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The electronics and data acquisition system for the DarkSide-50 veto detectors

The DarkSide collaboration

P. Agnes,[a] L. Agostino,[b] I.F.M. Albuquerque,[c,d] T. Alexander,[i] A.K. Alton,[g] K. Arisaka,[h] H.O. Back,[c,i] B. Baldin,[f] K. Biery,[f] G. Bonfini,[j] M. Bossa,[k,j] B. Bottino,[l,m] A. Brigatti,[n] J. Brodsky,[c] F. Budano,[o,p] S. Bussino,[o,p] M. Cadeddu,[q,r] M. Cadoni,[q,r] F. Calaprice,[c] N. Canci,[s,j] A. Candela,[j] H. Cao,[c] M. Cariello,[m] M. Carlini,[j] S. Catalanotti,[u,t] P. Cavalcante,[v,j] A. Chepurnov,[w] A.G. Cocco,[t] G. Covone,[u,t] L. Crippa,[x,n] D. D'Angelo,[x,n] M. D'Incecco,[j] S. Davini,[k,j,1] S. De Cecco,[b] M. De Deo,[j] M. De Vincenzi,[o,p] A. Derbin,[y] A. Devoto,[q,r] F. Di Eusanio,[c] G. Di Pietro,[j,n] E. Edkins,[z] A. Empl,[s] A. Fan,[h] G. Fiorillo,[u,t] K. Fomenko,[aa] G. Foster,[e,f] D. Franco,[a] F. Gabriele,[j] C. Galbiati,[c,n] C. Giganti,[b] A.M. Goretti,[j] F. Granato,[t,bb] L. Grandi,[cc] M. Gromov,[w] M. Guan,[dd] Y. Guardincerri,[f,cc] B.R. Hackett,[z] K.R. Herner,[f] E.V. Hungerford,[s] Aldo Ianni,[ee,j] Andrea Ianni,[c] I. James,[o,p] C. Jollet,[ff] K. Keeter,[gg] C.L. Kendziora,[f] V. Kobychev,[hh] G. Koh,[c] D. Korablev,[aa] G. Korga,[s,j] A. Kubankin,[ii] X. Li,[c] M. Lissia,[r] P. Lombardi,[n] S. Luitz,[jj] Y. Ma,[dd] I.N. Machulin,[kk,ll] A. Mandarano,[k,j] S.M. Mari,[o,p] J. Maricic,[z] L. Marini,[l,m] C.J. Martoff,[bb] A. Meregaglia,[ff] P.D. Meyers,[c] T. Miletic,[bb] R. Milincic,[z] D. Montanari,[f] A. Monte,[e] M. Montuschi,[j] M.E. Monzani,[jj] P. Mosteiro,[c] B.J. Mount,[gg] V.N. Muratova,[y] P. Musico,[m] J. Napolitano,[bb] A. Nelson,[c] S. Odrowski,[j] M. Orsini,[j] F. Ortica,[mm,nn] L. Pagani,[l,m,1] M. Pallavicini,[l,m] E. Pantic,[oo] S. Parmeggiano,[n] K. Pelczar,[pp] N. Pelliccia,[mm,nn] A. Pocar,[e,c] S. Pordes,[f] D.A. Pugachev,[kk,ll] H. Qian,[c] K. Randle,[e] G. Ranucci,[n] A. Razeto,[j,c] B. Reinhold,[z] A.L. Renshaw,[h,s] Q. Riffard,[a] A. Romani,[mm,nn] B. Rossi,[t,c] N. Rossi,[j] S.D. Rountree,[v] D. Sablone,[j] P. Saggese,[n] R. Saldanha,[cc] W. Sands,[c] S. Sangiorgio,[qq] C. Savarese,[k,j] E. Segreto,[rr] D.A. Semenov,[y] E. Shields,[c] P.N. Singh,[s] M.D. Skorokhvatov,[kk,ll] O. Smirnov,[aa] A. Sotnikov,[aa] C. Stanford,[c] Y. Suvorov,[h,j,kk] R. Tartaglia,[j] J. Tatarowicz,[bb] G. Testera,[m] A. Tonazzo,[a] P. Trinchese,[u] E.V. Unzhakov,[y] A. Vishneva,[aa] R.B. Vogelaar,[v] M. Wada,[c] S. Walker,[t,u] H. Wang,[h] Y. Wang,[dd,h,ss] A.W. Watson,[bb] S. Westerdale,[c] J. Wilhelmi,[bb] M.M. Wojcik,[pp] X. Xiang,[c] J. Xu,[c] C. Yang,[dd] J. Yoo,[f] S. Zavatarelli,[m] A. Zec,[e] W. Zhong,[dd] C. Zhu[c] and G. Zuzel[pp]

[1]Corresponding author.

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2016 JINST 11 P12007

[a] *APC, Université Paris Diderot, CNRS/IN2P3, CEA/Irfu, Obs de Paris, Sorbonne Paris Cité, 75205 Paris, France*
[b] *LPNHE Paris, Université Pierre et Marie Curie, Université Paris Diderot, CNRS/IN2P3, Paris 75252, France*
[c] *Department of Physics, Princeton University, Princeton, NJ 08544, U.S.A.*
[d] *Instituto de Física, Universitade de São Paulo, São Paulo 05508-090, Brazil*
[e] *Amherst Center for Fundamental Interactions and Department of Physics, University of Massachusetts, Amherst, MA 01003, U.S.A.*
[f] *Fermi National Accelerator Laboratory, Batavia, IL 60510, U.S.A.*
[g] *Department of Physics, Augustana University, Sioux Falls, SD 57197, U.S.A.*
[h] *Department of Physics and Astronomy, University of California, Los Angeles, CA 90095, U.S.A.*
[i] *Pacific Northwest National Laboratory, Richland, WA 99354, U.S.A.*
[j] *Laboratori Nazionali del Gran Sasso, Assergi AQ 67010, Italy*
[k] *Gran Sasso Science Institute, L'Aquila 67100, Italy*
[l] *Department of Physics, Università degli Studi, Genova 16146, Italy*
[m] *Istituto Nazionale di Fisica Nucleare, Sezione di Genova, Genova 16146, Italy*
[n] *Istituto Nazionale di Fisica Nucleare, Sezione di Milano, Milano 20133, Italy*
[o] *Istituto Nazionale di Fisica Nucleare, Sezione di Roma Tre, Roma 00146, Italy*
[p] *Department of Physics and Mathematics, Università degli Studi Roma Tre, Roma 00146, Italy*
[q] *Department of Physics, Università degli Studi, Cagliari 09042, Italy*
[r] *Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari, Cagliari 09042, Italy*
[s] *Department of Physics, University of Houston, Houston, TX 77204, U.S.A.*
[t] *Istituto Nazionale di Fisica Nucleare, Sezione di Napoli, Napoli 80126, Italy*
[u] *Department of Physics, Università degli Studi Federico II, Napoli 80126, Italy*
[v] *Department of Physics, Virginia Tech, Blacksburg, VA 24061, U.S.A.*
[w] *Skobeltsyn Institute of Nuclear Physics, Lomonosov Moscow State University, Moscow 119991, Russia*
[x] *Department of Physics, Università degli Studi, Milano 20133, Italy*
[y] *St. Petersburg Nuclear Physics Institute NRC Kurchatov Institute, Gatchina 188350, Russia*
[z] *Department of Physics and Astronomy, University of Hawai'i, Honolulu, HI 96822, HI*
[aa] *Joint Institute for Nuclear Research, Dubna 141980, Russia*
[bb] *Department of Physics, Temple University, Philadelphia, PA 19122, U.S.A.*
[cc] *Kavli Institute, Enrico Fermi Institute and Dept. of Physics, University of Chicago, Chicago, IL 60637, U.S.A.*
[dd] *Institute for High Energy Physics, Beijing 100049, China*
[ee] *Laboratorio Subterráneo de Canfranc, Canfranc Estación E-22880, Spain*
[ff] *IPHC,19 Université de Strasbourg, CNRS/IN2P3, Strasbourg 67037, France*
[gg] *School of Natural Sciences, Black Hills State University, Spearfish, SD 57799, U.S.A.*
[hh] *Institute for National Research, National Academy of Sciences of Ukraine, Kiev 03680, Ukraine*
[ii] *Radiation Physics Laboratory, Belgorod National Research University, Belgorod 308007, Russia*
[jj] *SLAC National Accelerator Laboratory, Menlo Park, CA 94025, U.S.A.*
[kk] *National Research Centre Kurchatov Institute, Moscow 123182, Russia*
[ll] *National Research Nuclear University MEPhI, Moscow 115409, Russia*
[mm] *Department of Chemistry, Biology and Biotechnology, Università degli Studi, Perugia 06123, Italy*
[nn] *Istituto Nazionale di Fisica Nucleare, Sezione di Perugia, Perugia 06123, Italy*

2016 JINST 11 P12007

[oo] *Department of Physics, University of California, Davis, CA 95616, U.S.A.*
[pp] *Smoluchowski Institute of Physics, Jagiellonian University, Krakow 30059, Poland*
[qq] *Lawrence Livermore National Laboratory, Livermore, CA 94550, U.S.A.*
[rr] *Institute of Physics Gleb Wataghin Universidade Estadual de Campinas, São Paulo 13083-859, Brazil*
[ss] *School of Physics, University of Chinese Academy of Sciences, Beijing 100049, China*

E-mail: stefano.davini@gssi.infn.it, luca.pagani@ge.infn.it

Abstract: DarkSide-50 is a detector for dark matter candidates in the form of weakly interacting massive particles. It utilizes a liquid argon time projection chamber for the inner main detector, surrounded by a liquid scintillator veto (LSV) and a water Cherenkov veto detector (WCV). The LSV and WCV act as the neutron and cosmogenic muon veto detectors for DarkSide-50. This paper describes the electronics and data acquisition system used for these two detectors. The system is made of a custom built front end electronics and commercial National Instruments high speed digitizers. The front end electronics, the DAQ, and the trigger system have been used to acquire data in the form of zero-suppressed waveform samples from the 110 PMTs of the LSV and the 80 PMTs of the WCV. The veto DAQ system has proven its performance and reliability. This electronics and DAQ system can be scaled and used as it is for the veto of the next generation DarkSide-20k detector.

Keywords: Front-end electronics for detector readout; Data acquisition concepts; Scintillators, scintillation and light emission processes (solid, gas and liquid scintillators); Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases)

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2016 JINST 11 P12007

Contents

2016 JINST 11 P12007

1 The DarkSide experiment

Many experimental results in cosmology and astrophysics provide evidence for the existence of a gravitationally-interacting, non-luminous dark matter. One of the candidates for dark matter are weakly interacting massive particles (WIMPs), neutral particles with mass $\sim$ 100 GeV and cross-section for interaction with nucleons in the range $\sim 10^{-45}$ cm^2 to $\sim 10^{-48}$ cm^2 that can be gravitationally bound inside our galaxy [1]. If WIMPs exist, they should occasionally interact with an atomic nucleus, causing the nucleus to recoil with kinetic energy less than 100 keV.

The DarkSide-50 experiment attempts to detect WIMP-induced nuclear recoils using a two-phase liquid argon time projection chamber (LAr-TPC), operated at the Gran Sasso National

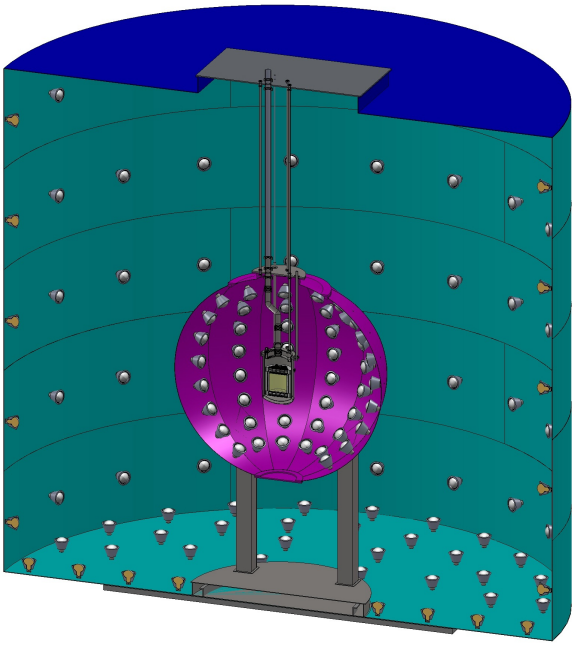

Figure 1. The DarkSide-50 experimental layout showing the mechanical scheme of the WCV, the LSV, and the LArTPC.

Laboratory (LNGS) in Italy. A WIMP search with an exposure of 1422(67) kg day using atmospheric argon (AAr) has been performed [2]. DarkSide-50 is now conducting a dark matter search with the LAr-TPC filled with underground argon (UAr), which contains a substantially reduced content of radioactive ^{39}Ar. The first WIMP search using UAr with an exposure of 2616(43) kg day is presented in [3].

A key feature of the DarkSide-50 design is its active veto system, composed of a liquid scintillator veto (LSV), serving as shielding and as anti-coincidence for radiogenic and cosmogenic neutrons, γ-rays, and cosmogenic muons, and a water Cherenkov veto (WCV), acting as passive shielding and as anti-coincidence for cosmogenic muons [4, 5]. Detailed information on the concept, development, installation, and performances of the DarkSide-50 veto detectors of DarkSide-50 can be found in [6]. Simulation results about the effectiveness of this veto systems are reported in [7, 8] and in the included references. This paper describes the electronics and data acquisition system (DAQ) of the active veto system of the DarkSide-50 experiment.

2 The DarkSide-50 veto detectors

The DarkSide-50 apparatus consists of three nested detectors (see figure 1). From the center outward, the three detectors are: the liquid argon TPC, which is described in detail in [2, 3], the LSV and the WCV. The LSV and WCV detectors constitute the active veto system of DarkSide-50 [6]. The DarkSide-50 detector system is located in the Hall C of LNGS at a depth of 3800 m.w.e., in close proximity and sharing many facilities with the solar neutrino detector Borexino [9–11]. In fact, the tank of the WCV is the same tank that was used for the prototype of the Borexino experiment [12].

2016 JINST 11 P12007

The electronics room for the DarkSide-50 veto detectors is located next to the electronics room of the Borexino experiment. Readout of the veto signals from the LSV and WCV are patched through the side of the WCV tank to the veto electronics room by cables $\sim$ 40 m in length, as described in detail in [6].

2.1 The LSV

The LSV detector is a 4 m diameter stainless steel sphere filled with 30 tonnes of boron-loaded liquid scintillator. The scintillator is a mixture of pseudocumene (PC) and trimethyl borate (TMB, $B(OCH_3)_3$), with 2, 5 diphenyloxazole (PPO) as fluor. The interior surface of the LSV sphere is covered with Lumirror diffusive reflecting sheets [13]. The LSV is instrumented with an array of 110 Hamamatsu R5912 8" PMTs [14], with low radioactivity glass bulbs and high-quantum-efficiency photocatodes (37 % average quantum efficiency (QE) at 408 nm). The phototube coverage of the LSV is $\sim$ 7%. The detailed description and characterisation of the LSV PMTs can be found in [6].

The LSV is designed to identify and veto neutrons which might enter or exit the LAr TPC. Neutrons thermalize by scattering on protons in the liquid scintillator and are efficiently captured by ^{10}B nuclei via two channels:

$$^{10}\mathrm{B} + \mathrm{n} \rightarrow {}^{7}\mathrm{Li} + \alpha \qquad 6.4\%$$
$$^{10}\mathrm{B} + \mathrm{n} \rightarrow {}^{7}\mathrm{Li}^{*} + \alpha, \quad {}^{7}\mathrm{Li}^{*} \rightarrow {}^{7}\mathrm{Li} + \gamma\ (478\,\mathrm{keV}) \qquad 93.6\%$$

Capture on ^{10}B proceeds to the ^{7}Li ground state with a branching ratios of 6.4%, producing a 1775 keV α particle, and to a ^{7}Li excited state with branching ratio 93.6%, producing a 1471 keV α particle and a 478 keV γ-ray. Neutrons can also capture on hydrogen, which causes the emission of a 2.2 MeV γ-ray.

The TMB contains natural boron with a 20 % natural abundance of ^{10}B which has a thermal neutron capture cross section of 3840 barn [7]. Loading TMB in the PC thus shortens the thermal neutron capture time. The thermal neutron capture time in a pure PC scintillator is $\sim$ 250 μs; it becomes $\sim$ 2 μs ($\sim$ 22 μs) in a 50% (5%) mixture of PC and TMB, as in the first (second) phase of DarkSide-50 [2, 3, 6].

Ionizing events in the LSV produce scintillation photons. These photons propagate inside the detector undergoing diffusive reflections on the Lumirror and the TPC cryostat until they are eventually detected by the PMTs. Due to the multiple reflections and low phototube coverage, the time distribution of the light signal extends up to 300 ns.

The information about the energy deposited in the LSV by a scintillation event is contained in the total charge collected by all PMTs within this time interval. The measured light yield in the LSV is $\sim$ 0.5 photoelectrons/keV (PE/keV) for β and γ-rays in the energy range from a few tens of keV up to a few MeV. The scintillation light produced by α particles is heavily reduced by scintillation quenching. In particular, the light output of the 1775 keV α from the neutron capture on ^{10}B has a β-equivalent energy of 50–60 keV, corresponding to 20–30 PE detected by the PMTs as measured in [6].

The PMTs work in the single photoelectron regime for scintillation events depositing less than $\sim$ 200 keV in the LSV, although the probability of having more than one photoelectron in a given PMT is not completely negligible, even for relatively low energy deposits. The signal due to a single photoelectron at the PMT output is a pulse with an amplitude of about 12 mV (on a 50 Ω load) and

2016 JINST 11 P12007

~20 ns total width. The PMTs are AC coupled and grounded at the cathode, so the meaningful part of the signal has negative polarity.

Scintillation events can happen anywhere in the volume of the LSV. Scintillation happening far from PMTs will deposit approximately the same fraction of light on each PMT in the detector, due to the multiple reflection of the light. However, this fraction can increase drastically for events happening near or directly in front of a PMT. Additionally, when a muon crosses the LSV, a huge scintillation signal is produced, corresponding to an energy deposit of $\sim$ 2 MeV per cm of scintillator traversed.

2.2 The WCV

The WCV is a cylindrical stainless steel tank, 11 m in diameter and 10 m high, filled with 1000 tonnes of ultra-pure water. To maximize the number of photons collected by the PMTs the internal surface of the tank is covered with reflecting Tyvek sheets. The WCV is instrumented along the floor and on the side of the cylindrical wall with an array of 80 ETL 9351 8" PMTs [12], with 27 % average QE at 420 nm. More information on the WCV can be found in [6].

The WCV serves two functions: it is a passive shield against external γ-rays and neutrons, and it is an active Cherenkov detector for muons crossing the LAr TPC or passing close enough to produce dangerous background events through the spallation of the various nuclei in the detectors.

When a muon crosses the WCV, a huge Cherenkov signal is produced. The signal is usually evenly distributed among all the PMTs because of the multiple reflections on the Tyvek and the low photocathode coverage. Due to the magnitude of the muon signal (larger than about 400 PE) and fast rise time (about 20 ns), muon events are easily distinguishable from noise events. Noise events are mainly due PMT pulses, from dark currents and from a small light leak in the WCV. For the WIMP dark matter search, we are interested in rejecting LAr TPC events that coincide with muon-like events in the WCV.

3 Requirements for the veto electronics and DAQ

Following very general considerations in the section above, we have designed a front end electronics and DAQ system that may work for LSV and WCV based vetoes for dark matter or neutrino detectors, according to the following requirements.

- *Single photoelectron detection with high efficiency and good time resolution*: the front-end (FE) and the digital electronics must be able to efficiently detect a signal as small as 0.25 PE with a time resolution better than 1 ns. This sub-PE threshold allows the detector to achieve high detection efficiency for very low energy events, including in particular the neutron capture signals on ^{10}B, or short tracks in the WCV. The good timing can be useful for eventual position and track reconstructions through time of flight techniques, following what has already been done, for example, by the Borexino experiment [9, 15];

- *Large dynamic range*: although most of the interesting events occur at low energy, it is important that the system performs well even when a huge signal appears in the scintillator, like the one generated by a muon or a muon-induced shower. It is difficult (and unnecessary in this case) to avoid saturating either the analogue amplifier of the ADCs, but it is important

2016 JINST 11 P12007

that the channel has a relatively short recovery time, so that muon-induced events, such as spallation neutrons, can be studied efficiently. We require that the vertical dynamics of the system can be as large as 7 PE and that the system be able to recover from a very large (×1000 or more) signal in less that 40 μs;

- *Synchronisation among channels*: it is important that the relative timing among hits collected by different PMTs (either in the LSV or in the WCV) is known and stable over the whole duration of a run, which typically continues for several hours. We require that the channels are synchronized within 1 ns, and that this synchronization is stable for at least 24 hours of continuos data taking;

- *Triggering capability and TPC synchronization*: the veto detectors are operated during TPC runs. Two independent modes should be possible: one in which the veto is triggered by the LAr TPC (regardless of the veto activity) and one in which the veto triggers on the LSV or WCV activity (regardless of the LAr TPC activity). TPC and veto events should be synchronized within at least 20 ns. The veto system should be able to trigger independently and the dead-time between two consecutive triggers should be virtually zero to avoid inefficiencies, particularly for correlated events.[1]

We have implemented these requirements in a system made of a custom built FE electronics and commercial National Instruments (NI) high speed digitizers, shown in figure 2. The same front-end modules (FEM) and digitizers are used for both channels of the both LSV and WCV of DarkSide-50. This electronics and DAQ system can be scaled and used as it is for the veto of the next generation DarkSide-20k detector.

4 Veto front-end electronics

The FE electronics for the DarkSide-50 LSV and WCV realize a set of functions that can be divided into analog and digital functions.

The FE analog functions are:

- due to the fact that LSV and WCV PMTs are AC coupled, FE must provide the high voltage and decouple the signals along a single cable;

- the PMT signals must be amplified by about a factor of 10 to achieve enough resolution on the single PE response (SER). The amplification must be at high bandwidth in order not to spoil the fast rise time of the SER (~ 3 ns);

- in order to have consistent dynamic range of the digitizers across the channels, the FE must provide programmable input offset compensation;

- a second non amplified output is very useful to extend the energy range of the detector;

[1] This paper describes the current implementation of these features. A project is in progress to implement trigger-less data taking of all PMT pulses with zero dead time and implementation of a pure software trigger. This new feature will be described in a separate paper.

2016 JINST 11 P12007

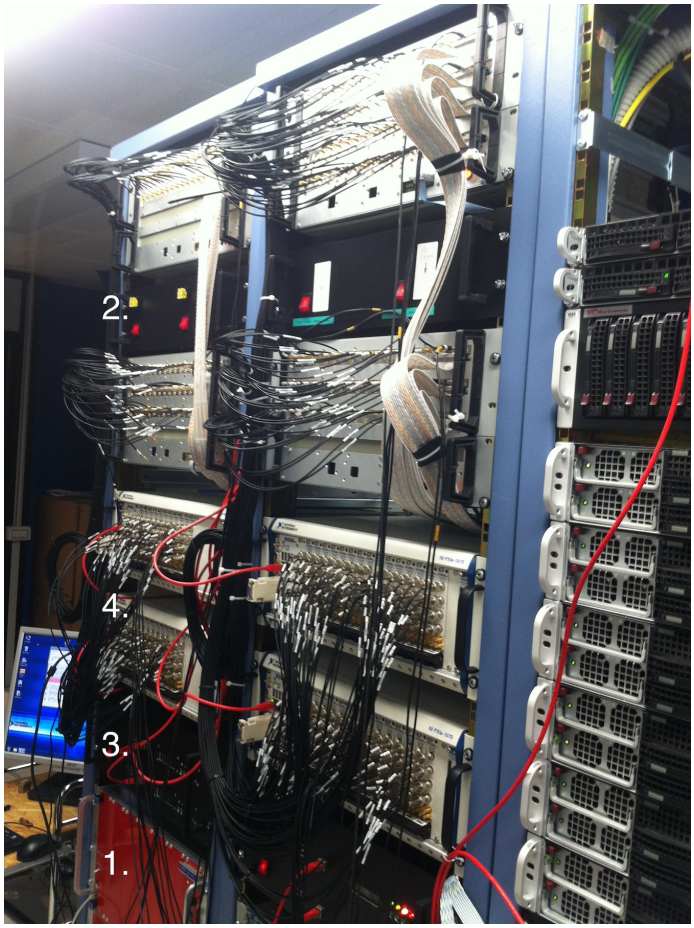

Figure 2. A picture showing the DarkSide-50 veto electronics in place. 1: the CAEN Mainframe (CAEN SY4527) for the CAEN HV boards (CAEN A1536); 2: the custom built front-end modules (FEM); 3: the custom built front-end digital board (FEDB); 4: the commercial National Instruments chassis (NI PXIe-1075) housing the National Instruments digitizers (NI PXIe-5162).

- easy scope inspection of the PMTs must be allowed through a second front panel output;
- a sum of the output of 16 channels is needed to build all channel sums for additional acquisition or analog trigger purposes;
- the possibility to distribute signals from a calibration input to all channels must be ensured.

The FE digital functions are:

- the signals must be discriminated on-board with programmable threshold to provide the digital signals used for the trigger and the monitor of the single PMT count rate. The discriminated signals are also fed to long range TDCs within the TPC acquisition process (see section 5.7).
- a monitor of the single PMT count rate must be provided;
- the LSV and the WCV trigger signals must be generated whenever a programmable number of channels in each sub-detector is firing within a time window of programmable duration;

2016 JINST 11 P12007

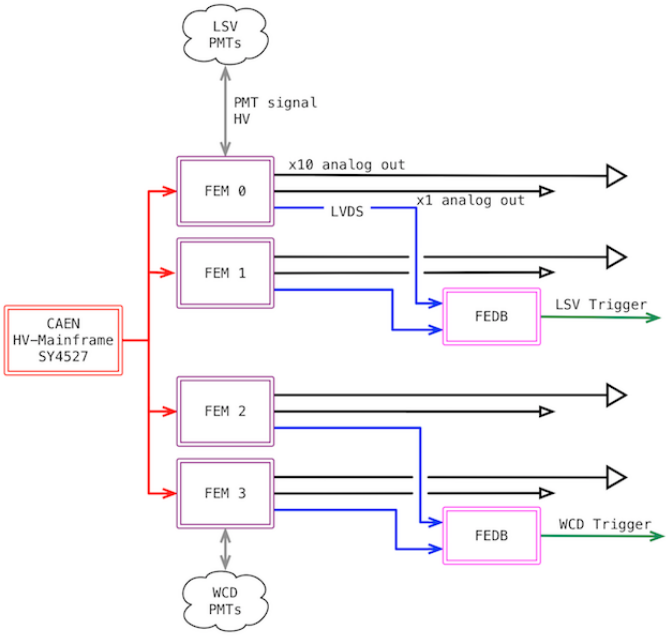

Figure 3. A block diagram of the front-end system of the DarkSide-50 veto.

- the run controller must be able to connect via TCP/IP to the FE in order to set parameters and to read single PMT count rate data;
- a local human interface with a display, buttons and LEDs is needed for prompt feedback on the system.

In order to fulfil these requirements we have designed a system composed of front end analogue boards (FEAB) and front end digital boards (FEDB). The system is composed of two identical modules for each sub-detector. Each 5U 19" module hosts up to four FEABs (i.e. up to 64 channels) and is mastered by a FEDB and features a dedicated linear power supply. A block diagram of the FE system is in figure 3.

4.1 Veto FEAB design

The FEABs were designed and implemented to provide the functionality expressed above with a high density of channels and low added noise. After simulations performed with PSPICE [16] and tests on a prototype, we came to the current configuration which houses 16 channels on each board, each with one input and three outputs. The final design has 200 μV_{rms} total output noise in its 230 MHz bandwidth at 20 dB gain setting.

A circuit diagram of the HV decoupling and amplification stage of the FEAB is shown in figure 4, while figure 5 shows the full FEAB circuit diagram. The two resistors R1 and R2 in figure 4 supply the high voltage to the PMT. The capacitor C1 (2.7 nF) acts as a high-pass filter, blocking the DC high voltage from the components of the board downstream. Due to this AC coupling, the downstream signal becomes bipolar. The time constant of the RC coupling is 135 ns.

2016 JINST 11 P12007

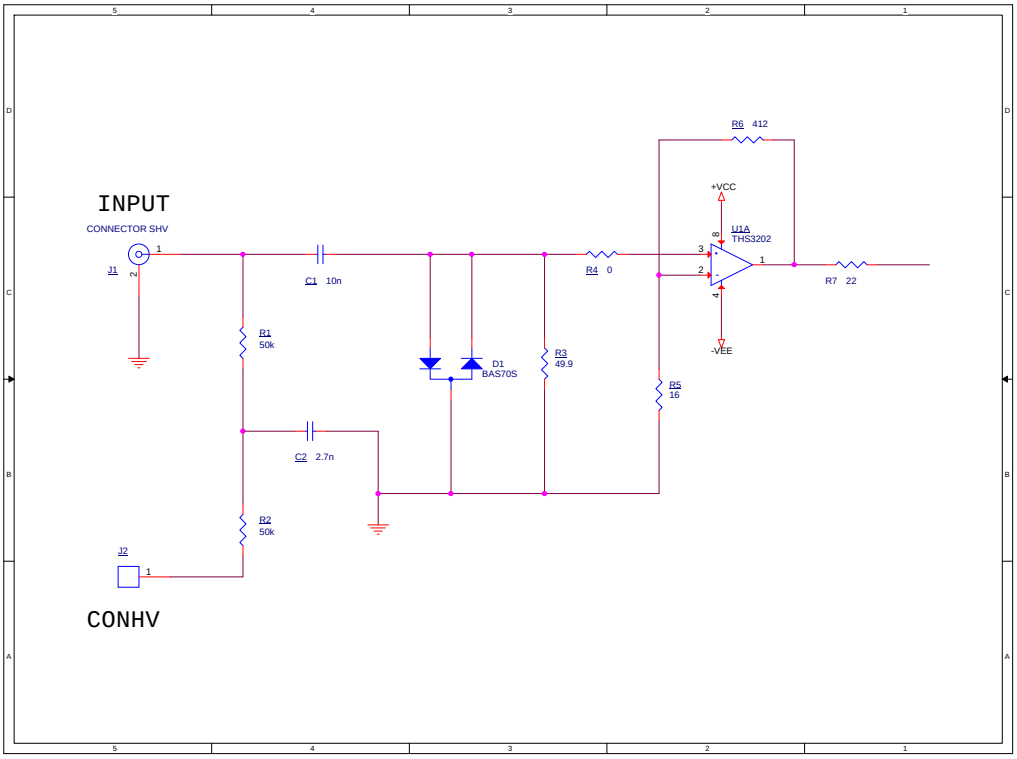

Figure 4. Circuit diagram of AC coupling and amplification in the FEAB.

The THS3201 (single) and THS3202 (double) fast current feedback operational amplifiers [17] whose gain bandwidth product is 1.8 GHz are mounted on the FEAB. The high gain bandwidth product was chosen upon the requirements on the time response described above. The signal is split into two branches, using the THS3202 for two gain ×10 paths and the THS3201 for a gain ×1 path. High-speed LMH6559 buffers [18] provide fan-outs to the ×10 output (given to the digitizers), the ×10 monitor output (oscilloscope probe), the discriminator, the offset regulation, and the adder output (sum of 16 channels). To host 16 channels in 1 PCB layout, we arranged 2 rows of 8 channels. FEAB features 8 PCB Layers, with a 274 × 274 mm footprint containing 2169 components on the top and bottom of the board.

On-board discrimination is implemented using the ADCMP567 [19], a dual ultrafast voltage comparator with differential PECL compatible output, followed by a buffer to send the digitized output (in LVDS standard) to the digital board. The threshold is set by the 8-bit DACs using the I^2C protocol.

The front panel top row alternates MCX and LEMO connectors for the ×10 outputs to be connected to digitisers and for scope inspections, respectively, while the bottom row features the MCX connectors for the ×1 outputs. The last two LEMO connectors on the left side of the panel are the calibration input and the sum output. The 34-pin connector yields LVDS discriminated outputs to the FEDB. The rear panel features 16 HV connectors where PMT cables are directly connected and a REDEL KAG.H22 multi-pin connector to the HV boards CAEN A1536 [20] housed in a CAEN Mainframe SY4527 [21].

2016 JINST 11 P12007

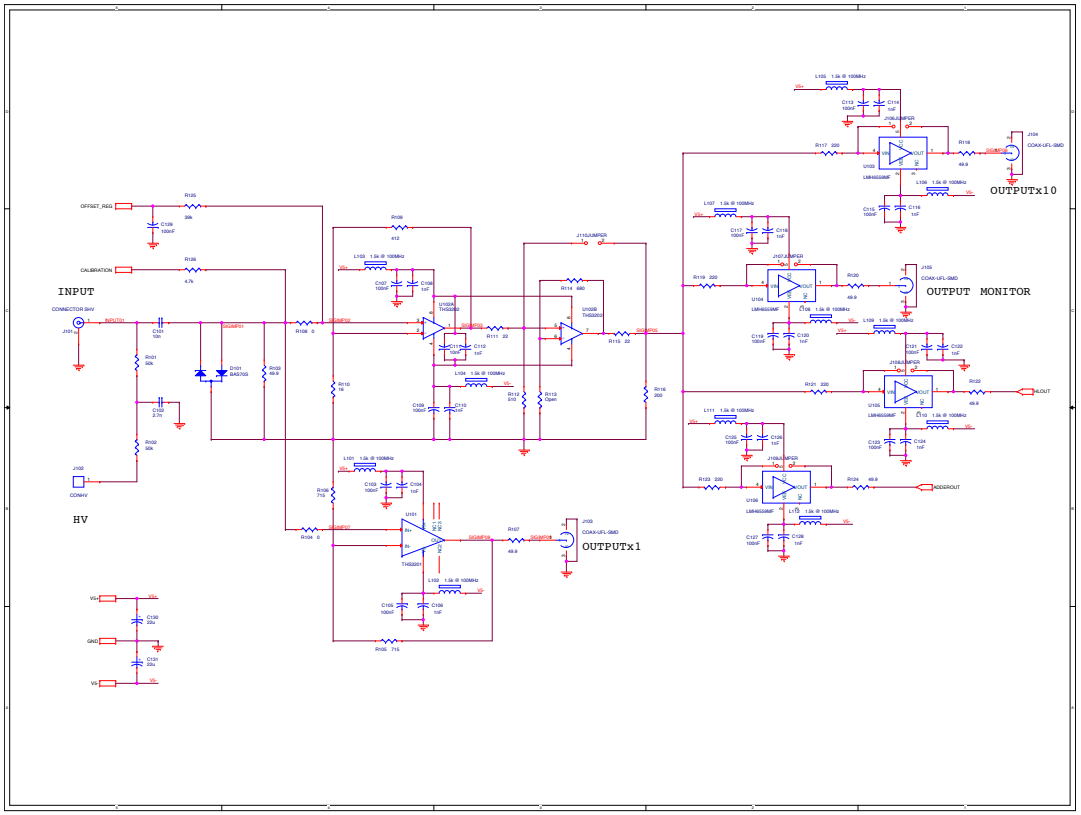

Figure 5. The full circuit diagram of the FEAB.

Special care has been devoted to minimize the noise originating from the power supplies. We avoided the use of switching power supplies and built a linear power supply able to deliver 15 A at the dual voltage, ±7.5 V, required for the FEAB modules.

4.2 Veto FEDB design

The FEDB handles the digital functions expressed above. It houses a Xilinx Spartan 6 FPGA [22] to perform the fast actions following the discriminator firing, namely trigger formation and the measurement of the single PMT rate. Slow control operations are implemented by a PIC32 micro-controller [23] mounted on its ethernet starter kit and interconnected to the FPGA. Both the FPGA firmware and the micro-controller program were developed specifically for DarkSide-50.

The FEDB houses a 100 MHz local clock issued by a quartz oscillator. The Xilinx Spartan 6 FPGA can operate on the local clock, however synchronization cannot be guaranteed in this way. For this reason, the FEDB hosts Micro Miniature MQ172 input connectors receiving a distributed clock signal.

The FPGA receives the 64 TTL logic inputs originated from the discriminators housed on the FEABs. The LVDS output of the FEAB are brought to a piggy-back board of the FEDB where they are duplicated to feed the TDC and then converted to single-ended TTL standard for the FPGA. At each clock cycle, the FPGA saves the status of the TTL lines and compares it with the previous one.

2016 JINST 11 P12007

4.2.1 FEDB single PMT rate function

At each clock cycle, if a transition from state 0 to state 1 is detected on a TTL input line, a 16-bit counter corresponding to that channel is incremented. Every 100 ms the 64 counters are copied to a cache and then reset. Whenever the user requests the counts for a channel the cached copy is provided. If a channel exceeds a programmable threshold N_{hot}, it is declared 'hot' (noisy). N_{hot} can be set in the 10–2550 kHz range. A front panel orange or red LED is lit if there is at least one or ten hot channels, respectively. If the user enables the specific functionality, the hot channels can also temporarily be excluded from the trigger while in the 'hot' condition.

The single PMT rate provided by the FEDB is used mainly for real time monitoring, in particular to detect abrupt spikes in the PMT rate, or channels with zero count rate, or drifts over a few hours time scale. A more accurate single PMT rate is also computed from the digitized waveforms, using a lower threshold and accepting pulses with shorter width, as described in section 5.4. However, this accurate computation requires running the full DAQ, storing the waveforms, and processing the data. The FEDB single PMT rate, although less accurate, is computed continuously and in real-time.

4.2.2 FEDB trigger function

In both the LSV and the WCV, FEDBs are daisy chained in a master slave configuration for triggering purpose, so that the generation of a trigger in the master is done on the full sub-detector rather than on just the 64 channels physically handled in the crate, while the trigger condition, evaluated in the slave, is ignored. Although two FEDBs are enough for DarkSide-50, the system is designed to scale up to larger detectors. In fact, each crate masters up to 4 slaves and more then two levels of cascading can be used.

In each FPGA, at each clock cycle, if a transition from state 0 to state 1 is detected on a TTL input line, a numeric flag for that channel is set to a programmable number N_{win}, unless the channel is disabled by the user (command set flag) or due to a high rate (see above). All flags different from zero are decremented at each clock transition. Each channel contributes to trigger formation for N_{win} clock cycles. At each transition, the number of flags different from zero is computed, stored in a 16 events FIFO and provided as a 10-bit sum output on an external connector along with a copy of the clock signal. The sum output is fed to the summed input present in the following module. Each FPGA samples the sum inputs (four are present for scalability) on the incoming clocks and adds them. The resulting record is added to sum of the internal channels retrieved from the FIFO with a programmable depth N_{del} (N_{del}=5 in our setup if running at 100 MHz). This mechanism ensures time alignment between the two crate stages by taking into account the cable length and the clock cycles needed in the master crate in order to sum the input signals from the preceding slave crates. Finally, the sum of all channels is compared to a programmable threshold N_{thr} eventually determining a trigger condition.

An internal prescale mechanism is also implemented to handle possible high trigger rates at low threshold. Upon meeting the trigger condition a down counter is decremented. A trigger is issued only when the counter reaches 0, after which it is reset. The counter value N_{pre} is programmable up 1024. The default value of 1 determines no prescale, with triggers being issued every time the condition is met.

2016 JINST 11 P12007

The duration of the trigger length is also handled via a programable down counter N_{len} in the 100 ns–25.5 μs range. While the trigger signal is on, the trigger condition is not checked, resulting in a self-vetoing behaviour. A yellow LED on the front panel is lit for 40 ms whenever a trigger is issued. The number of triggers is recorded with a dedicated counter, copied to a cache counter and reset every 100 ms. The content of the cached counter can be returned to the micro-controller upon request.

4.2.3 FE slow control functions

The FPGA is interfaced to the micro-controller via numerous I/O lines. A set/get command protocol is implemented with 16-bit data out (FPGA to micro-controller) and 10-bit data in (micro-controller to FPGA), plus a few control lines. The bus is mastered by the micro-controller and data are always polled. Commands are numerically coded in mirror tables between micro-controller and FPGA codes.

The micro-controller runs a single process which acquires an IP address from the LAN DCHP and acts as command interpreter by waiting for incoming socket connections on a specific port. In additions to the commands resolved by polling the FPGA, the micro-controller also communicates via I^2C to DACs for setting and reading back the channel input offset compensation (12-bit) and the discriminator thresholds (8-bit). The micro-controller also controls via I^2C an alphanumeric display mounted on the front panel (2 lines of 16 characters each). This is used to display single channel information (rate, threshold, offset, contribute-to-trigger-status) or trigger information (primary screen: rate, level, window length, prescale, secondary screen: trigger length, number of channels contributing, delay, status of automatic disabling). The command interpreter is interrupted by the timer every 500 ms to reread all displayed parameters and to refresh the screen. A green LED is toggled during this interrupt, obtaining a blinking "alive" monitor. Four buttons are read by interrupt request on the micro-controller which allow it to switch between single channel and trigger screens and to change the displayed channel.

5 Veto DAQ

A block diagram of the DAQ for the veto system of DarkSide-50 is displayed in figure 6. The analogue signals of all 190 PMTs in the veto are digitized and acquired using commercial NI PXIe digitizers after the amplification in the front-end stage. Waveform samples are acquired by the DAQ only when a trigger is received. The data readout code (ODAQ, outer detector DAQ) runs on each PXIe controller. When a trigger is received, ODAQ reads the waveforms from the digitizers and performs zero suppression. Four PXIe controllers are used, one for each PXIe chassis, in order to handle the 190 channels of the veto system. Each instance of ODAQ transmits the data fragment to the event builder PC via TCP/IP. The event builder application (ODB, outer detector builder) collects each data fragment from the four PXIe controllers and writes the event to disk.

The following sections describe the main features of the veto DAQ hardware, architecture and trigger.

2016 JINST 11 P12007

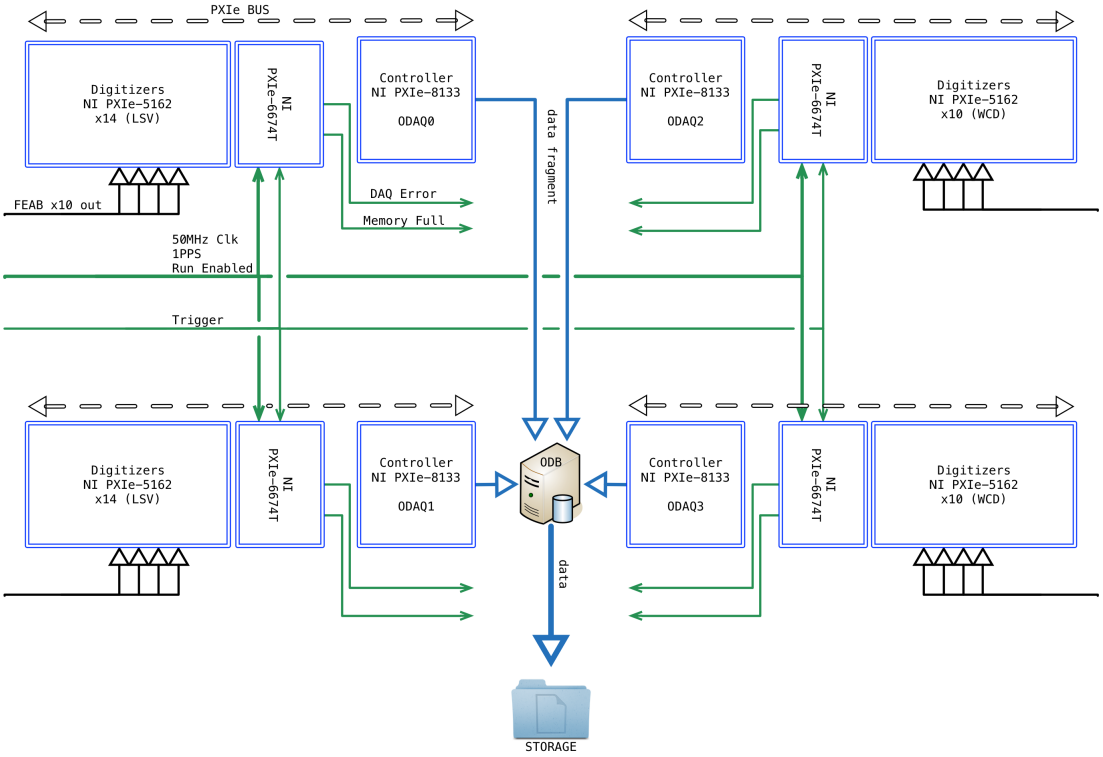

Figure 6. A block diagram of the DAQ system of the DarkSide-50 veto.

5.1 Veto DAQ design

The veto DAQ software system consists of two distinct applications: the acquisition-and-readout application ODAQ and the event builder application ODB. An instance of ODAQ runs on each of the 4 PXIe controllers. ODB runs on a devoted PC.

The DAQ of the DarkSide-50 veto has been designed to fulfil the set of requirements listed below:

- the system acquires data from 4 different PXIe chassis, preserving synchronization between each device in use;
- the DAQ system should be scalable (in principle) to any number of PXIe chassis;
- all DAQ applications are based on a state machine which correctly performs the necessary operations (e.g. initialize hardware, fetch data, stop acquisition, etc.);
- all DAQ applications should act as a server to listen for commands from the run controller (described in section 5.8), such as a request to start and stop data acquisition, communicating the system status, and provide the number of acquired events;
- the veto DAQ system should sustain an input data throughput (prior to zero suppression) up to 1 GB per second on each PXIe chassis;
- ODAQ must perform zero-suppression on the acquired waveform data;

2016 JINST 11 P12007

- ODAQ must provide host-target communication with the FPGA module, to retrieve the Trigger-ID and the timestamp of the events;
- all instances of ODAQ running on the 4 PXIe controllers can transmit data over a LAN to ODB;
- ODB must check the consistency of the timestamps of the events, then bundle zero-suppressed data from different chassis in a data fragment structure, which contains the timestamps and Trigger-ID of the event and the zero-suppressed waveforms;
- all DAQ applications should check CPU and memory usage in the machines running the DAQ, and gracefully make a transition to an error state if these exceed preset limits;
- ODAQ must periodically check the temperature of all digitizers and automatically shut them down to avoid potential thermal harm to the devices.

The most important requirement is the zero-suppression of the waveforms. Most of the samples in a 200 μs data acquisition window around a TPC trigger are just baseline (PMT pulses in fact represent just a few % of the data acquisition window). In order to avoid saturation of the bandwidth and excessive demand of storage, the DAQ must be able to select and keep only the samples needed to extract physical information on the event. The samples of interest are the ones both belonging to PMT pulses and in their neighbourhood (some samples before and after the pulse), which allow to compute the total amount of light collected in the vetoes, the time of the event with respect the LAr TPC scintillation, and an average baseline to better estimate the charge of the pulses.

Both ODAQ and ODB are written in LabVIEW [24] and conform to system design approach and documentation standards. We decided to use LabVIEW for the following reasons. It provides a natural integration with NI hardware, the availability of essential libraries, modules, and toolkits to develop a DAQ system (e.g. TCP/IP libraries) with a customizable user interface, high level design tools for multithreading and FPGA. This choice resulted in a fast development time with a small team of developers.

5.2 Veto DAQ hardware

The veto DAQ electronics provides digitized waveforms for each $\times$10 FE channels. It is organised in 4 PXIe chassis: 2 for the LSV and 2 for the WCV. Each chassis houses analog inputs for the waveform digitizers (56 for the LSV, 40 for the WCV) and digital TTL lines for the trigger and synchronization interface.

Each PXIe chassis (NI PXIe-1075 chassis [25]) is equipped with one NI PXIe-8133 controller [26], up to 14 digitizer boards NI PXIe-5162 [27], one NI PXIe-6674T timing and synchronization module [28] and one NI PXIe-7961R FlexRIO FPGA module [29].

The NI PXIe-8133 controller is a high-performance Intel Core i7-820QM processor-based embedded controller for use in PXI Express systems with 1.73 GHz base frequency, 3.06 GHz (single-core turbo) quad-core processor, and dual-channel 1333 MHz DDR3 memory. The PXIe controller is a true computer with Windows 7 OS. Each PXIe controller is equipped with two Gigabit Ethernet ports, used to transmit data to ODB and to receive commands from the run controller of the DarkSide-50 experiment.

2016 JINST 11 P12007

The waveform digitizers are NI PXIe-5162 modules. The sampling speed is 1.25 GSample per second (period 800 ps) and the resolution is 10-bit. Each sample is then 2 bytes in size. Each waveform digitizer module has 4 BNC input channels. The total on board memory is 1 GB (256 MB per channel). The input vertical ranges for each channel can be selected as 0.1, 0.2, 0.5, 1, 2 or 5 V peak to peak and the vertical offset can be regulated within the vertical range. The amplitude range is usually set between +0.1 V and −0.9 V, corresponding to a vertical range of 1 V with an offset of −0.40 V.

Trigger and synchronization functions are performed with NI PXIe-6674T timing modules, with one in each PXIe chassis. The timing module routes the clock and the trigger signals to the waveform digitizers and to the FPGA module in the PXIe chassis, allowing synchronization between all devices in the PXIe chassis. The timing module also routes the digital signals needed to generate timestamps to the PXIe-7961R FlexRIO FPGA module. The I/O connectors of the timing module are female SMA. The digital signal logic is TTL.

One NI PXIe-7961R FlexRIO FPGA module is used to generate the timestamp of each event using a 50 MHz reference clock common to the whole DarkSide-50 experiment, a 1 pulse per second (1PPS) signal received from the LNGS GPS, and a run enabled signal. This module also handles two digital lines to communicate DAQ errors and memory full signals.

5.3 DAQ software architecture and trigger

Each PXIe waveform digitizer module asynchronously and continuously samples the signals coming from the ×10 outputs of the FE modules. When a trigger is received, a block of samples around the trigger (the *acquisition window*) is stored in the digitizer memory buffer. The position of the trigger inside the acquisition window (the *trigger reference position*) is configurable, such that samples prior to the trigger can be stored. This allows the system to compensate for delays due to signal propagation and trigger generation. The acquisition windows and trigger reference positions used for data acquisition are described in section 5.5.

The trigger signal is received in the PXIe timing and synchronization module present in each PXIe chassis, to route the trigger condition to every PXIe digitizer in the PXIe chassis using the PXIe bus. This timing module also receives an external 50 MHz clock, the 1PPS signal, the run enable signal and the serial encoded Trigger-ID signal. The 50 MHz clock is used to synchronize the devices handled in the PXIe chassis to the main clock of the DarkSide-50 experiment. The digital lines are routed to the PXIe FlexRIO FPGA module that decodes the Trigger-ID and generates the timestamps to uniquely identify the event and correlate it with TPC triggers. More details on the FPGA logic, Trigger-ID, and timestamps are described in section 5.5.

Sample waveform data recorded by the PXIe digitizers are fetched asynchronously by the readout software ODAQ running on the PXIe controller. ODAQ waits for a configurable number of waveform data blocks (*number of records to fetch*) to be stored in the PXIe digitizer memory and readied to be fetched. When this condition is met, ODAQ starts fetching the records.

To reduce the size of waveform data, a zero-suppression algorithm is applied in ODAQ. The zero-suppression algorithm is described in section 5.4. Zero-suppressed data from the different PXIe digitizers in the same PXIe chassis are then bundled in a data fragment structure, which also contains the timestamp and the Trigger-ID of the event. Data fragments are then transmitted to ODB via TCP/IP, using the simple messaging reference library (STM) [30].

2016 JINST 11 P12007

During data acquisition, ODB collects data fragments from every PXIe chassis. For each trigger, the consistency of Trigger-IDs and timestamps of data fragments received from different PXIe chassis is checked, and a unique raw event with the pulses collected by all channels is written to disk. The raw file of the veto is a custom binary file which contains a header with all the information on the hardware and software configuration of the data acquisition, which is followed by the timestamp, Trigger-ID, and the zero-suppressed waveforms of each event.

ODB provides also an online monitor and event display. The trigger rate and the data transfer rate for each chassis are displayed. The user can also display, for the LSV and WCV, histograms of the number of PMTs with at least one pulse, the total number of pulses in a trigger, a waveform graph for a selected channel, and the summed waveform over all channels of the LSV and WCV.

5.4 Zero-suppression

The zero-suppression algorithm lets the user specify a threshold in amplitude, minimum width, and number of pre- and post-samples. When the waveform crosses the threshold and stays above threshold for the number of samples specified by the minimum width, the algorithm returns the entire waveform between both threshold crossings, including also the specified number of pre-samples before the first crossing and the specified number of post-samples after the final crossing. If the waveform goes below threshold and then back above before the specified number of post-samples have passed, the algorithm waits for the waveform to drop back below threshold and then starts counting post-samples starting from zero. Therefore, if two pulses appear on the same channel with overlapping zero-suppression windows, they are combined into one larger zero-suppressed pulse. The output of the zero-suppression algorithm is called the zero-suppressed waveform (or *pulse*, or zero-suppressed pulse). All the samples outside the zero-suppressed pulses are discarded.

During the first run of DarkSide-50, veto data were usually taken with a zero-suppression threshold of -30 mV (corresponding to ~ 0.25 PE), a minimum width of 3 samples (2.4 ns), and 20 ns worth of pre-samples and post-samples. Figure 7 shows a zero-suppressed waveform of a single photoelectron signal.

5.5 Veto trigger

There are 2 independent configurations for the input of triggers into the veto DAQ:

- *TPC trigger mode*: in this configuration the trigger signal of the veto is delivered only by the TPC DAQ. The length of the data acquisition window is usually set in a range from 70 to 200 μs in order to detect prompt and delayed physical events in the veto correlated to the LAr TPC;

- *Veto self-triggering mode*: in this configuration the input trigger of the DAQ is the logical "or" between the LSV and WCV triggers delivered by the FEDB (see section 4.2.2). The trigger rate is dominated by the LSV trigger rate and depends strongly on the LSV majority threshold. The length of the data acquisition window is usually set to 6.5 μs in order to acquire the whole scintillation signal, which has a duration of about 300 ns plus electronics overshoot, undershoot and afterpulses that naturally follows events with more than ~ 10 PE per channel.

The data used for the WIMP search are taken in TPC trigger mode.

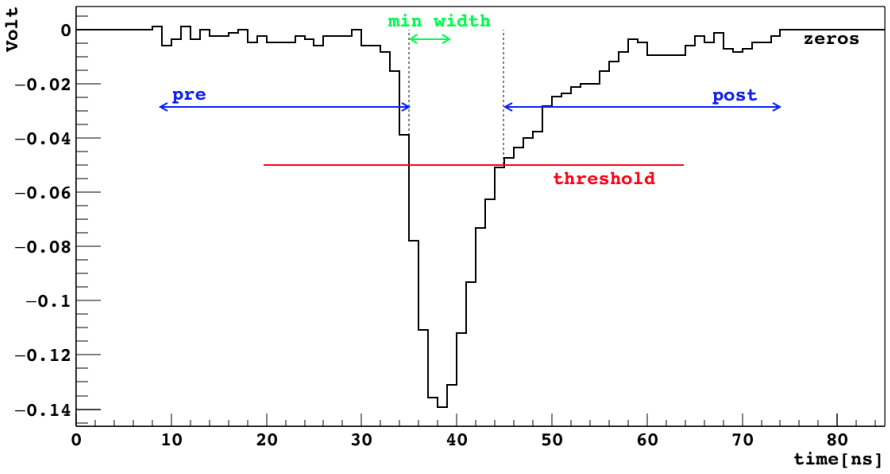

Figure 7. Zero suppressed waveform of a single photoelectron pulse. The red line represents the zero suppression threshold in amplitude (set to −0.5 mV in this example). The green line represents the minimum width, which refers to the minimum number of samples the waveform must stay above the threshold. The blue lines represent pre- and post-samples.

In the first phase of DarkSide-50, with a 50% mixture of PC and TMB in the LSV, the acquisition gate was set to 70 μs, of which 10.5 μs came prior to the trigger, and 59.5 μs after the trigger (corresponding to a reference position of 15%).

In the second phase of DarkSide-50, with mixture of PC (95%) and TMB (5%) in the LSV, the acquisition gate was set to 140 μs, of which 10.5 μs came prior to the trigger and 129.5 μs after the trigger. The acquisition gate was later extended to 200 μs, of which 10.5 μs came prior to the trigger and 189.5 μs after the trigger.

The data acquired during the calibration campaigns of DarkSide-50 were taken using both triggering modes. Information about the DAQ of the LAr TPC of DarkSide-50 can be found in [32].

The LAr TPC and veto systems can trigger independently, but a synchronization mechanism must be provided in order to correlate the LAr TPC events with veto signals. The two DAQ systems are physically displaced, therefore synchronization between the two systems is obtained through a high precision timestamp obtained from a common 50 MHz clock slaved to a 1PPS signal received from the LNGS GPS.

The trigger signal is delivered to each of the 4 PXIe timing modules and distributed to all the devices in the PXIe chassis through an internal bus. The PXIe timing modules also receive the 50 MHz clock, the 1PPS signal, and the run enable signal from the TPC DAQ. These signals are used to compute the timestamp of the event using three counters:

- the 1PPS counter which counts the number of seconds elapsed since the run enable signal was delivered (which correspond to the start of the run);
- the GPS fine time counter which counts the number of 50 MHz clock cycles elapsed since the run enable or the 1PPS signal (whichever comes last);
- the GPS one second counter which counts the number of 50 MHz clock cycles elapsed since the most recent 1PPS signal.

2016 JINST 11 P12007

The three counters are evaluated for every trigger received, then stored in a DMA FIFO of the PXIe FlexRIO FPGA and read asynchronously by ODAQ. These counters allow the system to compute the time of the trigger since the start of the run with a precision of 20 ns. The same timestamp is also computed in the TPC DAQ system, allowing physical events in the LAr TPC and the vetoes to be correlated with each other, even in veto self triggering mode.

In the TPC trigger mode, a 16-bit Trigger-ID is generated for each trigger by the TPC DAQ and serially encoded using a frequency modulation scheme. The Trigger-ID signal is acquired by the PXIe timing module and routed to the PXIe FlexRIO FPGA where it is decoded.

5.6 Communication and synchronization with the LAr TPC DAQ

The scheme in figure 8 describes the hardware communication between the TPC DAQ and the veto DAQ. Unless otherwise noted, signals in the block diagram are active high TTL, ECL or LVDS. The hardware connections between the TPC DAQ and the veto DAQ are based on optical links and FPGA units [29, 31]. The electrical-optical converters are VME V730-13 and V720-13 modules. The FPGA units are:

1. the TPC V1495 main trigger module located at the TPC electronics room;
2. a V1495 trigger module located at the veto electronics room;
3. a fanout V1495 module located at the veto electronics room;
4. the veto PXIe FlexRIO FPGA logic modules located in the PXIe crates, described above.

In what follows we focus on the communication between the TPC DAQ and triggering with the veto system. The details of the TPC DAQ and trigger are described in [32].

The TPC V1495 main trigger module, located at the TPC electronics room, generates the TPC triggers necessary to trigger the veto when running in TPC trigger mode. The trigger signal, the run enable signal, and a 16-bit Trigger-ID are transferred via optical link to the veto V1495 trigger module located at the veto electronics room. A 50 MHz clock signal is also sent from the TPC electronics room to the veto electronics room for synchronization of all veto and TPC DAQ devices to the same clock. The V1495s and the veto PXIe-6674T modules also receive the 1PPS signal. The logic inside veto V1495 trigger module decodes the Trigger ID and places it in an internal FIFO memory for the readout via the VME bus as a part of the TPC data stream. All VME FPGAs and electrical-optical converters are allocated in a VME crate.

Four copies of the trigger signal, the run enable signal, the Trigger-ID, the common 50 MHz clock, and the 1PPS signal are generated by the fanout V1495 module and delivered to each veto PXIe-6674T module in the four PXIe chassis. The PXIe-6674T handles the synchronization of any clock inside the PXIe chassis to the common 50 MHz clock, allowing the synchronization of all veto digitizers. The PXIe-6674T also routes the trigger signal to the digitizers through the PXIe bus, allowing for a synchronous trigger among all devices. Finally, the PXIe-6674T routes the trigger signal, the run enabled signal, the serially encoded Trigger-ID, and the 1PPS signal to the PXIe FlexRIO FPGA modules, which decodes the Trigger-ID and generates the timestamp, as described in section 5.5. The PXIe FlexRIO FPGA module has internal DMA memory which is used as a

2016 JINST 11 P12007

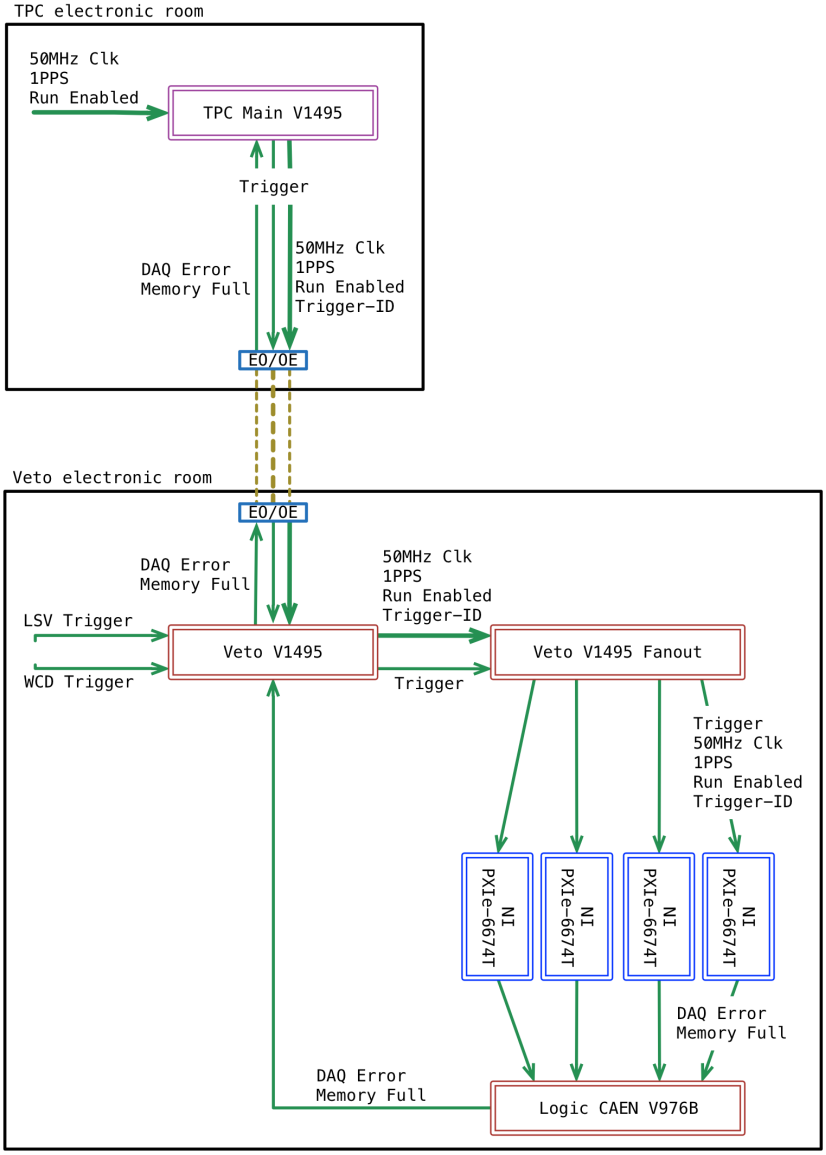

Figure 8. A block diagram showing the trigger connections between the TPC DAQ and the veto DAQ. EO means electrical to optical conversion.

FIFO to store Trigger-ID and timestamp counters for each incoming trigger. This memory is read out with each event in order to provide trigger markers for TPC and veto synchronization.

A Memory Full and a DAQ Error signal can be produced by each of the PXIe FlexRIO FPGA modules in the veto DAQ system in order to keep data readout rate at the maximum. This signal is sent to the TPC electronics to prevent generation of the TPC trigger (and associated veto triggers) when the veto DAQ is close to filling all available memory buffers. The logical "or" of the four Memory Full and DAQ Error signals is performed by a CAEN V976B logic module.

2016 JINST 11 P12007

5.7 Veto TDC

A secondary data stream for the veto system is implemented using TDCs. As described in section 4, one of the discriminated FEDB veto outputs from each channel is connected to a CAEN V1190 multi-hit 128 channel TDC [33]. The two V1190 modules are located in the veto electronics room and connect to the TPC V1495 trigger unit through the veto V1495 fanout logic unit. The trigger signal for the TDC modules is generated by the veto V1495 trigger module. The TDC DAQ software is built within the Fermi National Accelerator Laboratory's (Fermilab) *art* framework [34].

This secondary system does not replace the main veto readout but provides a back-up system. TDCs are only triggered by the TPC, even when the veto runs in self trigger mode, therefore each TPC trigger has direct mapping to the veto TDC data. Consequently, the TDC provides an independent data stream for the LSV and WCV, and is synchronized to the TPC trigger providing a cross-check on the efficiency of the ADC-based veto DAQ.

5.8 Run control

The veto DAQ and TPC DAQ systems are handled by a common run controller which is configured to permit different data acquisition modes:

- global runs, where the TPC and veto run at the same time (choosing either TPC trigger mode or veto self-trigger mode) and
- local runs, where the sub-detectors run independently.

The run controller application has been developed in LabVIEW, and conforms to LabVIEW coding and documentation standards. The run controller handles the communication to all DAQ devices and processes. Communication over ethernet with the TPC sub-systems is performed using the XML-RPC protocol, while communication with veto sub-systems is performed using the LabVIEW STM protocol. The run controller application has a graphical user interface that allows an operator to initialise or reset DAQ configurations, start and stop the data acquisition. The run controller supervises the data acquisition. When either the TPC or the veto DAQ display unusual behaviour or errors, data acquisition is automatically stopped. All DAQ sub-systems are then reset and re-initialized, and new run is automatically started. The run controller also logs the relevant parameters of each run to the experiment database.

6 Performance

DarkSide-50 began its first physics run in November 2013, with the veto electronics and DAQ system described above. The full DAQ system has been operational since then and can be remotely controlled. The DAQ system is constantly improved in performance, to maximize stability and introduce new features stemming from the requests from the experiment. The physics results obtained with DarkSide-50 are described in [2, 3]. The performances of the radiogenic neutron detection efficiency are described in [6]. The veto front end and DAQ system has shown to met the design goals for the physics of DarkSide-50. In particular, the LSV can easily detect the low energy signals of neutron captures on ^{10}B, allowing a very high neutron detection efficiency.

2016 JINST 11 P12007

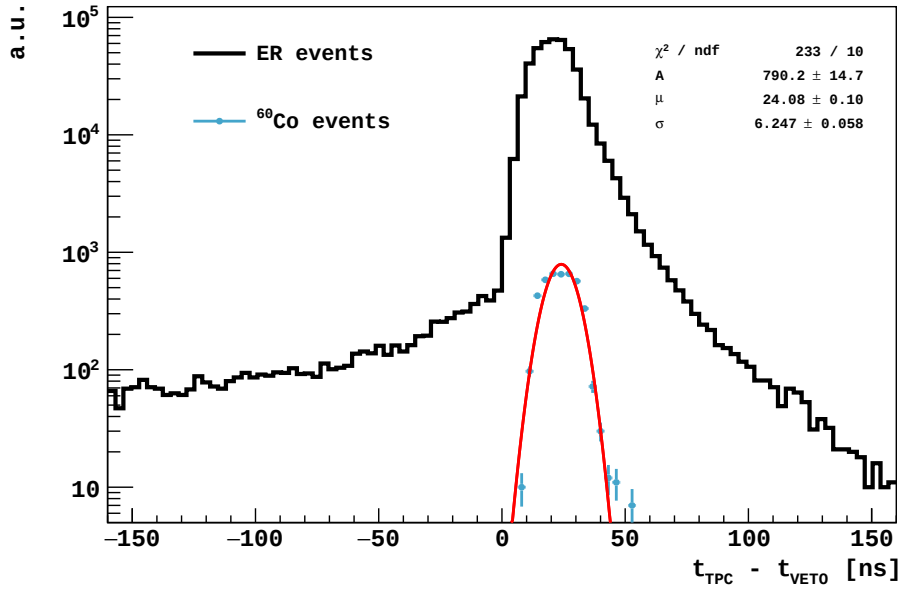

Figure 9. Time difference between the TPC event and the LSV event. The time difference is computed for two separate classes of events: electron recoil (ER) events from ^{241}AmBe (black line) calibration and ^{60}Co background (cyan dots). The events from ^{241}AmBe calibration are mainly due to the γ-ray emission from the decay of the excited state of $^{12}C^{*}$, which interact both in the LSV and in the TPC. The peak in the ER event is less narrow compared to the ^{60}Co events due to the higher pile-up rate and the complexity of the event in the ^{241}AmBe calibration. More information on the reconstruction and analysis algorithms used to identify the events can be found in [2, 6].

The veto data acquisition is stable with a maximum input data throughput of about 1 GByte per second on each PXIe chassis (each of the two LSV chassis acquire 55 channels and each of the two WCV chassis acquire 40 channels). We recall that trigger rate that the system can sustain depends on the the length of the acquisition window, but also on the background activity of the detector, since the system performs zero-suppression at DAQ software level. In the first phase of DarkSide-50, the LSV showed an unexpectedly high activity of the ^{14}C background (~150 kBq) in the TMB, whose feedstock was partly derived from modern carbon that has a much higher ^{14}C content than petroleum-derived [2, 6]. Despite the fact that during this initial period of data taking the ^{14}C activity was a factor ~ 500 higher than design goals, the veto DAQ was able to sustain the data throughput, allowing a duty cycle higher than 95% during WIMP search runs. The output data throughput of the veto in this phase, using an acquisition window of 70 μs, was ~ 200 kByte for each trigger, under a TPC trigger rate up to ~ 50 Hz.

After the first WIMP search run, the ^{14}C activity in the LSV was significantly reduced, from 150 kBq to 0.3 kBq. The TMB concentration in the LSV was also reduced, requiring longer acquisition windows following each TPC trigger in order to detect neutrons with high reliability [6]. In the current detector condition, the maximum trigger rate which allows a stable data aquisition with an acquisition window of 200 μs is ~ 16 Hz in TPC triggering mode. This is an order of magnitude more than the current LAr TPC trigger rate of ~ 1.5 Hz [3], ensuring high stability of the DAQ. The output data throughput in the current WIMP search mode, using an acquisition window

2016 JINST 11 P12007

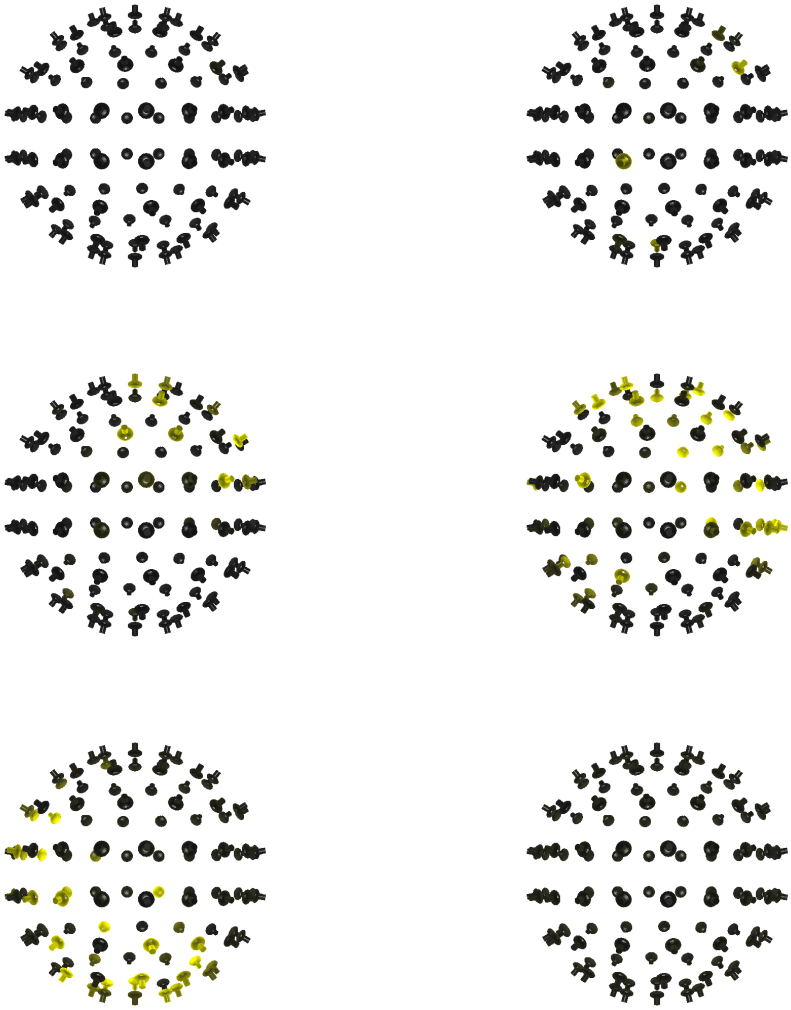

Figure 10. Event display of a muon crossing the LSV. The intensity of the color on the PMT is proportional to the waveform amplitude. The frames are sorted from then top to bottom. Each of the 6 frames is delayed of 8 ns with respect to the previous frame. More informations on the reconstruction algorithms used to generate this event display can be found in [2, 6].

of 200 μs, is $\sim$ 19 kByte for a complete LSV and WCV event triggered by the TPC. With the usual LAr TPC trigger rate the veto DAQ writes $\sim$ 2.5 GByte to disk per day (before bzip2 compression that decreases the size of the data by about a factor of 4). The veto electronics and DAQ system has also been used to acquire data during calibration campaigns with neutron and γ radioactive sources deployed in the LSV [35]. The system has shown to be stable during the calibration campaigns, with a data throughput higher of a factor $\sim$ 10. In particular, the veto DAQ system in TPC trigger mode has no need for trigger pre-scaling when a neutron source of $\sim$ 10 Bq is inserted in the LSV.

The synchronization between the LAr TPC and the LSV is checked and monitored using physical events that generate scintillation light at approximately the same time in both detectors, such as ^{60}Co decays, events from ^{241}AmBe calibration, and muons crossing the three detectors.

2016 JINST 11 P12007

^{60}Co, which can be found in the TPC stainless-steel cryostat, decays beta to an excited state of ^{60}Ni, which decays with the emission of two γ-rays with energies 1.17 MeV and 1.33 MeV respectively. The geometry of DarkSide-50 allows for one of the γ-rays to reach, and trigger, the LAr TPC, while the other produces scintillation light in the LSV. These events are used as benchmark to define the *prompt coincidence region* between the LAr TPC and the veto. A histogram of the time difference between TPC and LSV events is displayed in figure 9, where a peak is clearly visible. The synchronization between the LSV and the WCV is also checked and monitored using muon events which cross both detectors. The event display of a muon crossing the LSV and is displayed in figure 10.

The WCV has also met its design goals. In particular, the muon flux detected by the WCV is the same measured by Borexino [4, 6]. The probability of missing a muon crossing the WCV is negligible, as shown by an analysis of muons in coincidence in the three detectors.

7 Conclusions

This paper reports the description of the electronics and DAQ system developed for the veto detectors of the DarkSide-50 experiment. The DAQ involves data collection from a liquid scintillator veto and a water Cherenkov detector.

The front end electronics, the DAQ, and the trigger system discussed here have been used to acquire data in the form of zero-suppressed waveform samples from the 110 PMTs of the LSV and the 80 PMTs of the WCV. The synchronization between the veto DAQ and the TPC DAQ is also described.

The electronics and DAQ have been used since the start of the DarkSide-50 experimental phase to acquire data for dark matter runs and calibration campaigns with radioactive sources. It is foreseen to use the electronics and DAQ system described here throughout the remainder of DarkSide-50 operations. The veto DAQ system has proven its performance and reliability even with a background rate $\sim$ 500 time higher than the design goal. The Veto DAQ system has ensured stable data taking and allowed for a high duty cycle of data taking.

The DAQ described here is entirely based on LabVIEW. Any programming language could have been used to write the code, but the LabVIEW approach made it possible for a small team to quickly develop a high-throughput, fast-digitizer DAQ system with a large number of channels.

Because of the demonstrated performance and reliability, the whole electronics and DAQ system architecture of the DarkSide-50 veto detectors is scalable for the veto detectors of a multi-ton DarkSide experiment, such as the proposed DarkSide-20k detector.

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2016 JINST 11 P12007

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2016 JINST 11 P12007

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2016 JINST 11 P12007