UNIVERSIDADE ESTADUAL DE CAMPINAS
Faculdade de Engenharia Elétrica e de Computação

Fabio Kelm Pereira

Design of an Analog Reconfigurable Low-Pass Filter for Multistandard Radio

Projeto de um Filtro Analógico Reconfigurável Integrado para Radios Multi-standard

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Dissertation presented to the School of Electrical and Computer Engineering of the University of Campinas in partial fulfillment of the requirements for the degree of Master of Electrical Engineering, in the area of Electronics, Microelectronics and Optoelectronics.

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Supervisor: Prof. Dr. Gustavo Fraidenraich

Co-Supervisor: Prof. Dr. Eduardo Rodrigues de Lima

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Abstract

Some applications in communications have multiple bandwidths, requiring circuits with more flexibility in the radio receiver. When focusing on the bandwidth selection filter of the radios, a common solution for its flexibility is the use of a switch between passive components of the circuit. However, this alternative increases the number of elements if several frequency widths are necessary. More components lead to a bigger footprint area, which is undesired in the context of Integrated Circuits. This work proposes a reconfigurable, fully integrated Sixth Order Butterworth filter for these front-end receivers. To achieve this, the circuit uses a transistor-based structure to act as a voltage-controlled resistor, in the topology called MOSFET-C. The resulting circuit is simulated using a 65nm CMOS technology. It attains a footprint of 0.015 mm^2 and a frequency step of 1 MHz in filter selectivity while consuming $1,08mW$ of power. The designed filter is compared to State-of-the-Artworks, showing it can be used in multiple applications and configurations from 40 MHz down to 1 MHz channel bandwidth.

Keywords: Analog Filters, Multi-standard Radio, Reconfigurable Filter, Integrated Circuits.

Resumo

Algumas aplicações na área de comunicação utilizam múltiplos comprimentos de banda, e, portanto, necessitam de maior flexibilidade por parte do rádio de recepção. Se focarmos a atenção em filtros seletores de banda, uma das soluções comuns é o chaveamento entre elementos passivos diferentes, como capacitores e resistores. Essa alternativa, no entanto, aumenta o número de componentes. No contexto de Circuitos Integrados, isso tem como consequência uma área grande de silício, o que é indesejado dentro de um projeto. Esse trabalho propõe um Filtro totalmente integrado reconfigurável de sexta ordem do tipo Butterworth, projetado para esse tipo de rádios de recepção. O circuito proposto utiliza a chamada topologia MOSFET-C, usando uma estrutura a base de transistores para agir como resistores controlados por tensão. O circuito é simulado usando uma tecnologia 65nm CMOS. O resultado final tem uma área de 0.015 mm^2 e um consumo de potência de $1,08mW$, além de um passo de frequência de 1MHz. O projeto é comparado a outros circuitos no estado da arte, e pode ser usado em múltiplas aplicações com frequências entre 1MHz e 40MHz.

Palavras-chaves: Filtro Reconfigurável, Filtro Analógico, Radios Multi-standard, Circuitos Integrados.

"The good thing about science is that it's true whether or not you believe in it."
(Neil deGrasse Tyson)

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List of abbreviations and acronyms

RF	Radio Frequency
LPF	Low-Pass Filter
ABB	Analog Baseband
DVB-S2	Digital Video Broadcasting - Satellite - Second Generation
MAC	Media Access Control
LNA	Low-Noise Amplifier
LO	Local Oscillator
PVT	Process, Voltage, and Temperature
DRC	Device Rule Checking
LVS	Layout Versus Schematic
PEX	Parasitic Extraction
ETSI	European Telecommunications Standards Institute
WLAN	Wide-Local Area Network
PMOS	P-channel (positive) metal–oxide–semiconductor
NMOS	N-channel (negative) metal–oxide–semiconductor

List of symbols

Ω	Resistance
ϵ	Amplitude Error
k	Boltzmann Constant
ξ	Dampening Factor
η	Drain Junction and Miller multiplication effect
R	Resistor value
C	Capacitor value
L	Inductor value
M	MOS Transistor

Contents

1 Introduction

This dissertation comprises the work developed for the Master's degree in Microelectronics, and it is divided into five chapters. Chapter 1 is a brief introduction and literature review. Chapter 2 is an overview of the design choices and development of the circuit, as well as its chosen schematic form and preliminary results. Chapter 3 presents robustness analysis for the circuit considering statistical methods and worst-case analysis. Chapter 4 presents the physical design (layout) of the circuit, and some results after the parasitic extraction. Finally, chapter 5 draws some conclusions and future works.

1.1 Background and Motivation

Wireless communications have evolved to become part of our everyday use. From connecting people over large distances, allowing easy and quick access to knowledge, or help to monitor things from a safe distance, more and more devices communicate with each other, sometimes in an autonomous form.

In this greatly connected world, different standards were developed with specific applications in mind. This incurred in a plethora of different standard, most of them with so different characteristics from each other. This way, making the same radio being able to communicate using multiple standards is a challenge. And although it's possible to have multiple radios in the same system, this solution brings up other problems. Aside from the increase in cost and size, it can bring interference problems for multiple antennas or having to switch the same antenna to different radios.

In light of this challenge, Multi-standard Radios were thought off. Multi-standard Radios proposes a reconfigurable, programmable circuit that can change to receive and transmit signals on demand. This is relatively easy to accomplish in the digital domain, but rather intricate for the analog and RF Front-end.

Figure 1.1 shows a simplified diagram for a general front-end receiver with only one analog down-conversion. Usually, the front-end can be divided into the Radio Frequency (RF) part, composed by the Low-noise amplifier (LNA), Mixer, and Local Oscillator (LO); the lower frequency part, which can be at Baseband frequency (BB) or Intermediate frequency (IF), and is composed of filters, one or more variable gain amplifiers (VGA) and one analog to digital converter (ADC); and finally, the digital front-end, that is responsible for demodulation and further needed processing.

Working with Multi-standard Radio demands flexibility in design. RF circuits usually have more stringent constraints for their design, especially for noise and linearity.

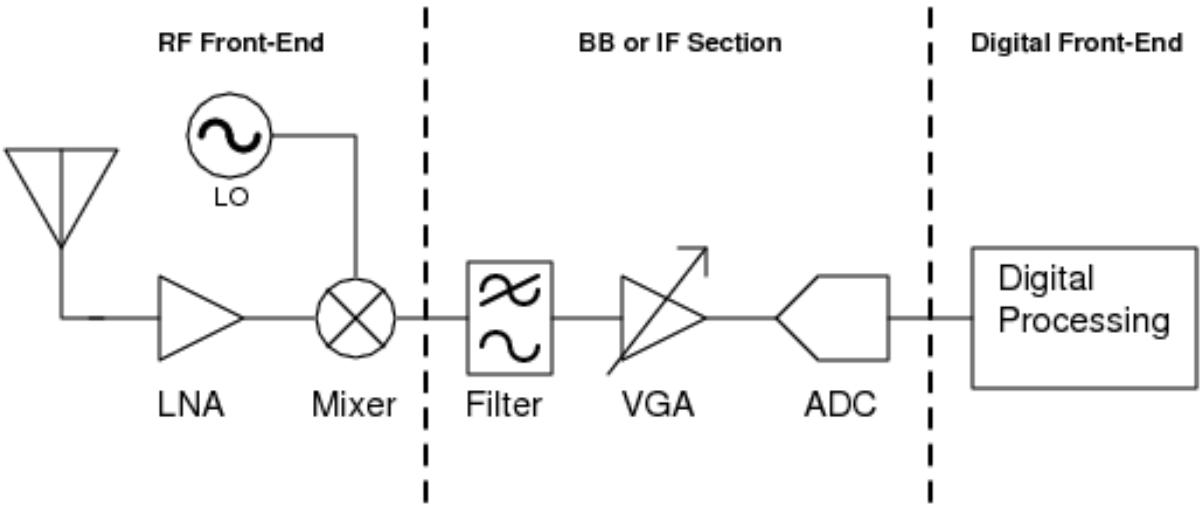

Figure 1.1 – Simplified diagram of a general Front-End receiver.

Adding multiple configurations makes the requirements even more difficult.

On the other hand, digital circuitry is a lot easier and faster to implement, and is usually the focus of Multi-Standard applications. This, however, comes with some caveats: first, digital filters with multiple coefficients are usually very large, occupying important silicon area in integrated designs; second, the added blocks usually means higher sample rates (i.e. higher frequency operation) on both the digital circuits and in the A/D Converter, which can both be harder to achieve and usually rises the power consumption of the blocks.

In order to make the design more efficient both in area and power, but keeping flexibility in the frequency domain, this work proposes the design of a finely configurable analog filter. The Filter is chosen because it has the function of removing, from the down-converted signal, the remaining information. The block is designed at lower frequencies rather than RF, making its requirements more relaxed. Since it's still in the analog domain, design can provide better power efficiency and more precision in the footprint.

1.2 Application and Circuit Specifications

To validate this circuit, the Digital Video Broadcasting - Satellite - Second Generation (DVB-S2) standard is chosen, whose specification can be seen in [1]. This standard has broader requirements for the analog front-end, with channels with different bandwidths. This means channels varying from 1 to 10 MHz in bandwidth or grouped together in up to 40MHz bandwidth. Considering that this multiplexing is made in the digital domain, the analog receiver must be able to adapt its bandwidth capability for all the possible options, making this an ideal test case for circuit reconfigurability. On further parts of this work, other Standards such as ETSI DVB-T ([2]) and IEEE 802.11n ([3]) are also cited and compared. This is, however, accomplished superficially, just to evaluate the multi-standard capability of the filter.

As previously stated, in the DVB-S2 Standard, there is not a defined bandwidth, but a range of possible frequencies, which vary from 1MHz to 40MHz. As we are using a ZIF receiver, the project of the filter frequency response must be evaluated in this range, and therefore it should be a Low-Pass Filter (LPF). The standard establishes the sensitivity of the receiver varying from -85dBm to -35dBm of input power, which for the receiver project is further improved from -90dBm to -25dBm.

Finally, although it could be interesting to have only one multi-functional block due to linearity and noise concerns, it is interesting to break down the block into multiple smaller blocks. This is shown in Figure 1.2. To avoid impedance matching problems, two buffers are added to the chain. This way, the mixer output load can be matched to the filter input impedance, and the Variable Gain Amplifier (VGA) input stage is isolated from the filter output. This block is necessary since the VGA changes the output load according to the gain configuration.

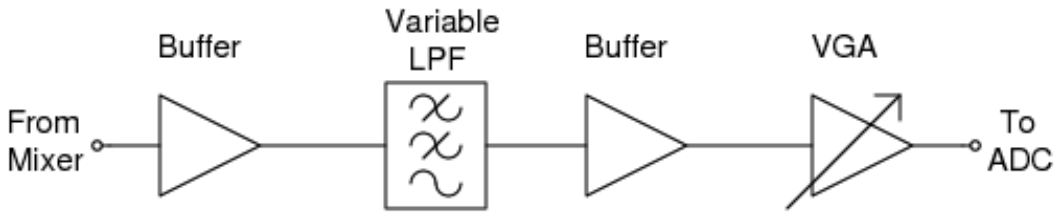

Figure 1.2 – Complete diagram for the Analog Baseband of the receiver.

The DVB-S2 standard allows to define the Noise Figure (NF) for the entire receiver chain. Using the Friis formula for noise as shown in Equation 1.1, it's possible to define that the baseband circuit must have a noise figure of $NF \leq 25dB$ at the narrowest frequency, i.e. $1MHz$. As the filter is one of the first blocks in the ABB chain, as can be seen in Figure 1.2, the best situation would be a NF close to this value.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \dots \tag{1.1}$$

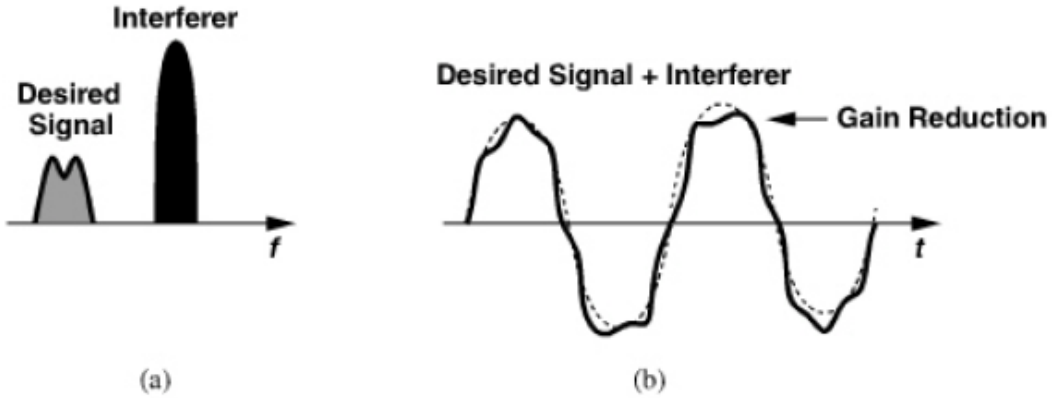

Figure 1.3 – General representation of a Interferer signal (a) and it's possible consequences to signal integrity (b). (adapted from [4])

Besides noise, the circuit must be capable of dealing with interference. Normally interference is dealt in two forms: i) either in the architecture level, by for example using specialized filtering like Surface Acoustic Wave (SAW) filters or topologies that neglect this kind of effect; and ii) by having high linearity, which guarantees that the circuits will still behave as expected even with high input signals. Figure 1.3 shows an example of an interferer signal.

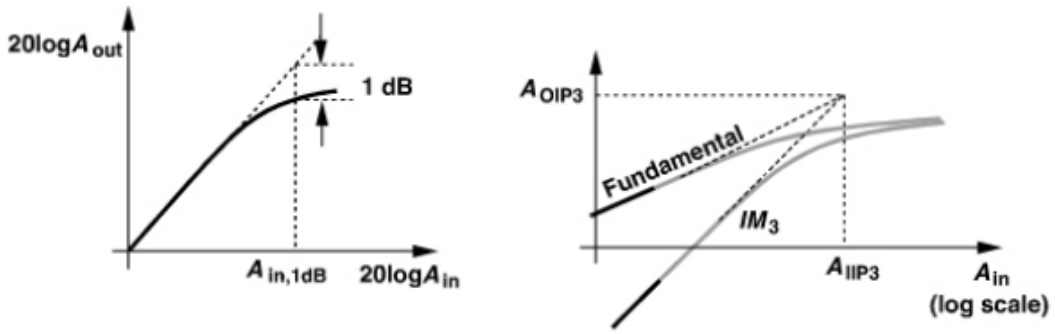

Figure 1.4 – General representation for two RF metrics: 1dB compression (right) and IIP3 (left). (adapted from [4])

For the linearity evaluation, two common metrics are the point of 1dB compression (P_{1dB}) and the Input-referred third-order intercept point (IIP_3). A graphical representation of both is shown in Figure 1.4. For the P_{1dB}, it's considered the point where the correlation Signal-in between Signal-out deviates by 1dB of the expected linear value. This usually happens because of the saturation of a non-linear component, like the supply limitation that saturates the output of an amplifier. Similarly, the IIP_3 uses a linear extrapolation. However, it compares the signal on both the fundamental and third

harmonic, and evaluates the theoretical cross point of these curves. In theory, from this point onward, the signal would be corrupted by the third harmonic frequency, and your signal would become indistinguishable from it. Realistically, the non-linear effects deviate the curve and change this point, but we still use the extrapolated value as the metrics for it.

For the filter, these values are derived from the chain like the noise figure, even using something similar to Equation 1.1. But, contrary to what happens with noise, the most important block is the ADC. It's the input capacity of the block that defines how the conditioning circuits should deliver the signal. For this project, we have the following specifications: $P_{1dB} \geq -10dBm$; and $IIP3 \geq 0dBm$.

1.3 Literature Review

As it is well known, a filter is a circuit that operates changing the frequency spectrum of a signal, as commented in [5]. Therefore, we can understand a filter by looking at how signals with different frequencies will behave and what is the resulting signal at the output of the system. Figure 1.5 shows a basic example to illustrate this definition.

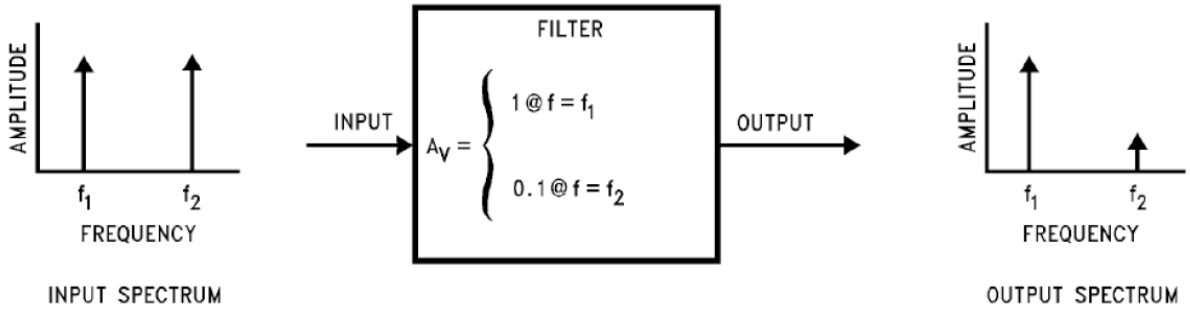

Figure 1.5 – General representation for a electronic filter. (adapted from [5])

Continuous-time filters are a type of circuit that operates in the continuous time-domain, with an analog level voltage response. This means they don't need a clock or sampling frequency to operate, like discrete-time filters; and theirs output levels aren't restricted, represented by 1s and 0s, like a digital filter, as discussed in [6]. Continuous-time filters can be represented using Laplace domain expressions, like:

$$H_f(s) = \frac{a_0 + a_1 \cdot s + a_2 \cdot s^2 + \dots}{b_0 + b_1 \cdot s + b_2 \cdot s^2 + \dots} \tag{1.2}$$

where the coefficients a_m are used to define the m zeroes, and the coefficients b_n are used to define the n poles. More specifically, these poles and zeroes help determine the shape of the frequency response. For this reason, is typical in filter design to use the components that allocate them in proper places, achieving the desired frequency response. Two usual concepts of filter design used are the pass-band, a region of the spectrum that is unaltered by the filter; and the stop-band, a region that is attenuated by the filter. We use this abstraction to create a "mask" of ideal frequency response, and try to design a filter with poles and zeroes that match this graph.

$$H(s) = \frac{s-a}{s-b}, a > b \tag{1.3a}$$

$$H(s) = \frac{(s-a_1)\cdot(s-a_2)}{(s-b_1)\cdot(s-b_2)}, \quad a_2 > b_2 > b_1 > a_1 \tag{1.3b}$$

$$H(s) = \frac{s-c}{s-d}, d > c \tag{1.3c}$$

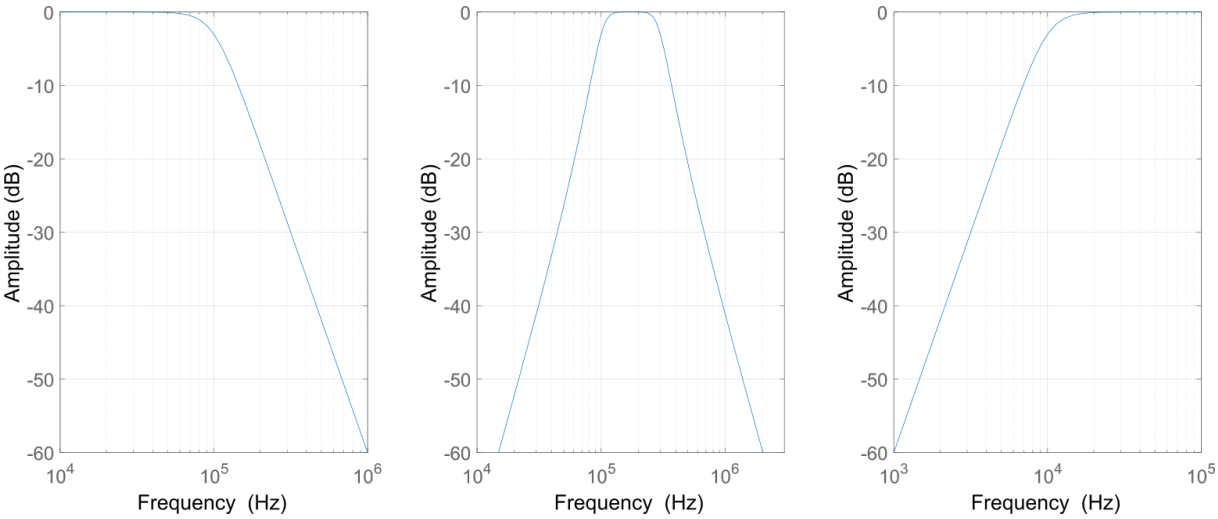

Figure 1.6 – Different types of filters and their frequency response. Equations 1.3a, 1.3b, 1.3c represent, respectively, the three figures.

Figure 1.6 shows this mask approach, and their equations are represented in Equations 1.3. The filters shown in Figure 1.6 are the low-pass filter, band-pass filter, and high-pass filter, respectively, with the equations for each curve in the same order. These three are some of the most common types of electronic filters. The type of filter to be used in a radio receiver is dictated by the architecture and position in the signal chain. For example, a Direct Conversion receiver, also called Homodyne receiver, uses generally a Low-pass filter in the processing of the signal in the Baseband frequency f_0. In contrast, a Low-IF architecture, which is a kind of Heterodyne receiver, uses a Band-pass filter since the desired signal is in the frequency f_{IF}. This correlation between receiver architecture and the type of filters needed is shown in various works of literature, like in [4].

Comparing the ideal mask used for a filter with the images in Figure 1.6, it's possible to see that they are different, especially in the transition between the Pass-band and the Stop-band. This happens because making a sudden transition is unrealistic. For this reason, mathematical approximations can be made to try to fit the frequency-domain equation to a specific mask. Some of the more famous ones are the Butterworth approximation, the Bessel approximation, the Chebyshev approximation, and the Elliptic approximation. Figure 1.7 shows an example of the same filter, with $f_c = 10kHz$, designed using different mathematical approximations.

The Butterworth approximation is defined by the maximal flat pass-band. This means there is no frequency ripple, and the response is more linear across the pass frequencies of the filter. This is achieved by having the poles directly in the desired cutoff frequency. However, because of that approach, the frequency roll-off is directly related to the number of poles, being 20dB/octave per pole. This means that, for a higher selectivity filter, a Butterworth approximation needs more poles than the others. The step response of the filter in the time-domain has noticeable overshoot, which can be undesirable depending

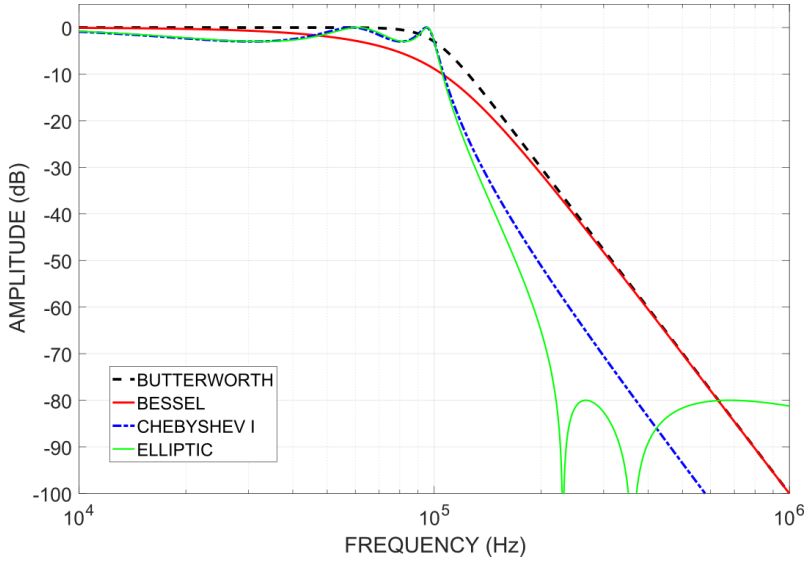

Figure 1.7 – Comparison of the same Low-Pass filter using different approximations: Butterworth, Bessel, Chebyshev, and Elliptic approximations.

on the application. This technique is named after Stephen Butterworth and his 1930 paper "On the theory of filter amplifiers"[7].

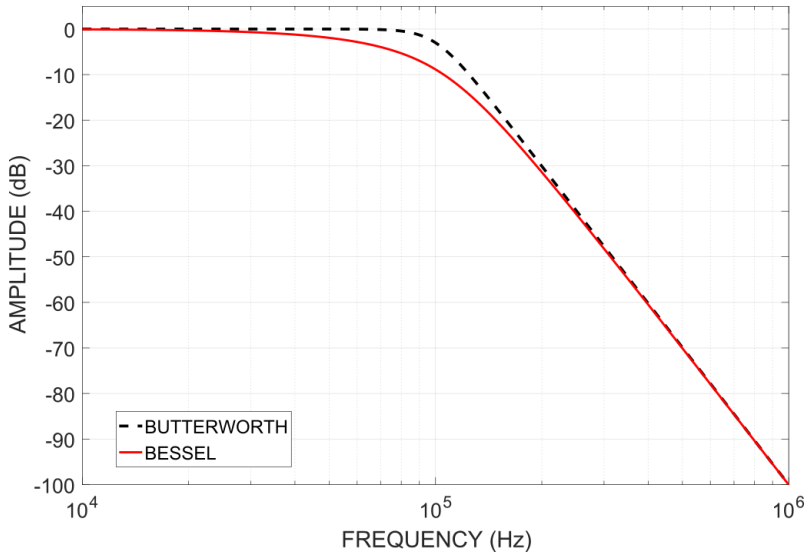

Figure 1.8 – Comparison of the same Low-Pass filter using different approximations: Butterworth and Bessel.

The Bessel approximation considers the time domain response of the filter, focusing on reducing the overshoot in the step response of the filter and minimizing group delay. A Bessel design usually works with a dampening factor $\xi \geq 0,707$, which means, in a 2° order system, that two different real poles exist. This increases stability and reduces overshoot. It however affects the roll-off curve decreasing the selectivity when compared to other approximations with the same order, as can be seen in Figure 1.8.

The Chebyshev approximation tries to achieve a steeper roll-off, and therefore more selectivity, with a lower order filter. Looking at Figure 1.7, the f_{3dB} is the same but

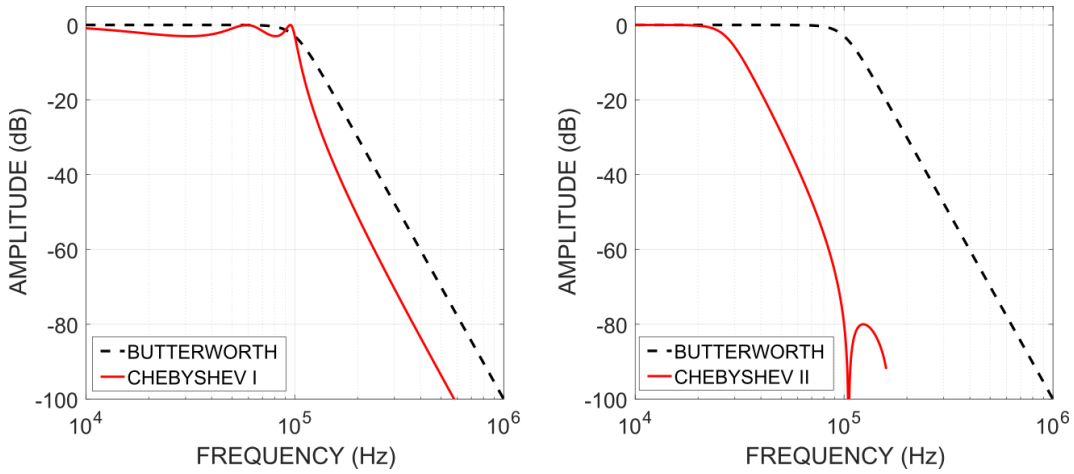

Figure 1.9 – Comparison of the same Low-Pass filter using different approximations: the same Butterworth compared to two different Chebyshev types.

the linear descend begins early in comparison to the other two filters. This is possible using the Chebyshev polynomials in determining the poles of the filter. However, the approach introduces ripples in the frequency response of the filter, which then needs to be considered in the design. Usually, by defining the maximum desired ripple peak, it's possible to calculate the equivalent Chebyshev polynomial. . This technique name comes from Pafnuty Chebyshev, who proposed the original mathematical polynomial function used in it.

The frequency-domain ripple can also be designed to be in the pass-band or the stop-band of the filter, which is usually the criteria to differentiate Chebyshev filters. Type I, also called only the Chebyshev filter, has the ripple in the pass-band; while Type II, also called reverse-Chebyshev filter, has the ripple in the stop-band of the filter. The Type II Chebyshev approximation also is fairly inaccurate in the cutoff frequency. Figure 1.9 shows the two different types, each compared to an equivalent Butterworth approximated filter.

The Elliptic Approximation is like a combination of both types of Chebyshev, focusing on minimizing the transition between Pass-band and Stop-band. This way, for the same order, the Elliptic filter will always have higher selectivity than another type of filter. This can be seen in Figure 1.10, where an Elliptic approximated filter is compared to two Chebyshev approximations. However, one downside to this filter is the presence of a ripple on both bands. This increases the complexity of the function and, later, of the circuit needed to achieve it, as the maximum ripple on both bands must also be specified.

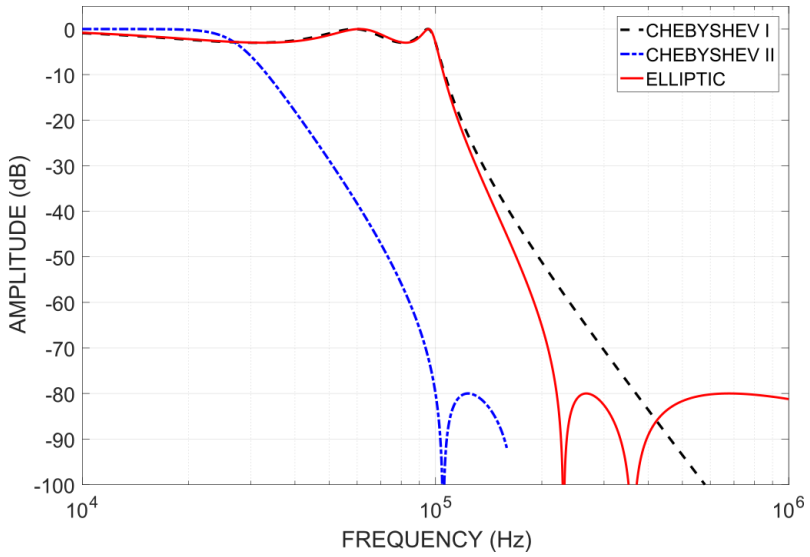

Figure 1.10 – Comparison of the same Low-Pass filter using three different approximations: Elliptic and Chebyshev Types I and II.

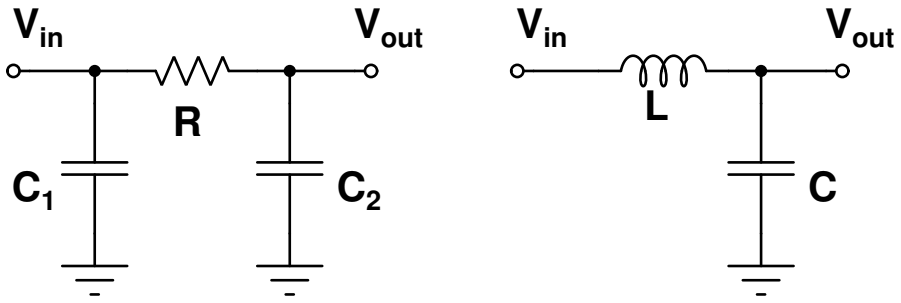

Figure 1.11 – Example of two 2° order passive filters: RC and LC.

Once the approximation is performed and the desired function $H(s)$ is known, the next step in the Electronic filter design is to translate this into components that can represent this function in the s domain. A traditional approach to this is to use simple resistors, capacitors, and inductors in a passive array, as these components have different frequency responses. This is a very simple and straightforward way, as you can choose values for the passive array and match the desired transfer function. Passive filters usually are called by what components they have: RC for resistors and capacitors, LC for inductors and capacitors, and so on. Figure 1.11 show two example of such filters. However, passive filters usually have an attenuation to the voltage signal. Also, in the context of integrated circuits (IC), these passive components can have downsides: inductors are too large and usually have too many parasites currents, limiting their equivalent quality factor; resistors have a great process variability, which means that applications using this device might need a complex calibration process.

An interesting approach that can be similar to a passive array, is the use of MOSFET-C. This approach uses the linear region, also called the Triode region of a transistor as a way of emulating the behaviour of a resistor. This is interesting since you

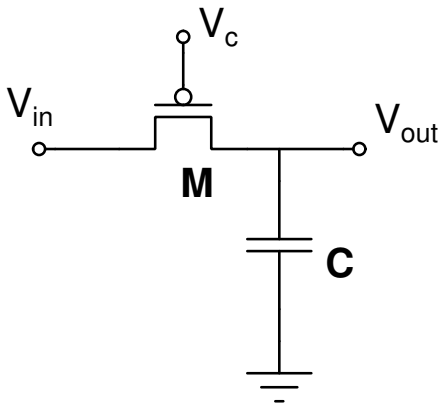

Figure 1.12 – Example of a 1st order low-pass filter, implemented using a MOSFET-C topology.

can design this in a similar way to a RC filter with direct allocating poles. The difference is that, in the linear region, the transistor transconductance varies linearly with the applied gate voltage. This allows the value of the equivalent resistance to change, moving the pole according to the voltage gate V_c. Figure 1.12 shows an example of a 1st order low-pass MOSFET-C filter.

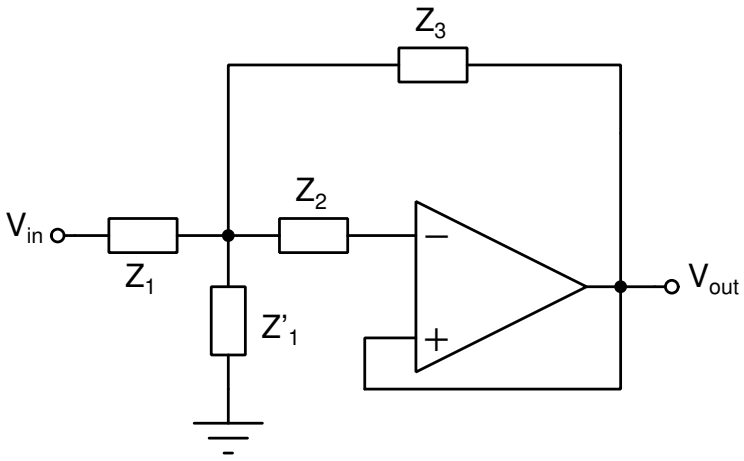

Figure 1.13 – Model of a Sallen-Key biquad cell.

Another alternative to passive component arrays is an Active Filter, which uses active components like amplifiers to improve voltage gain in the pass-band and linearity. The most common use of these filters is with circuits called biquadratic, or biquads for short. One of the most common topologies for biquads is the Sallen-Key approach, for which an example can be seen in Figure1.13. This biquad filter can achieve the desired 2 main poles using only one amplifier and a feedback network of passive components. It also utilizes the amplifier in a buffer configuration, which is good to guarantee the driving capability and a no-gain approach ($0dB$). The main drawback of this topology is the sensitivity to parasitic capacitance, especially in the input nodes. This can change the position of the poles and lead to a change in the desired frequency response.

This and the other active filter topologies discussed can be found in many works of the literature, like in [8].

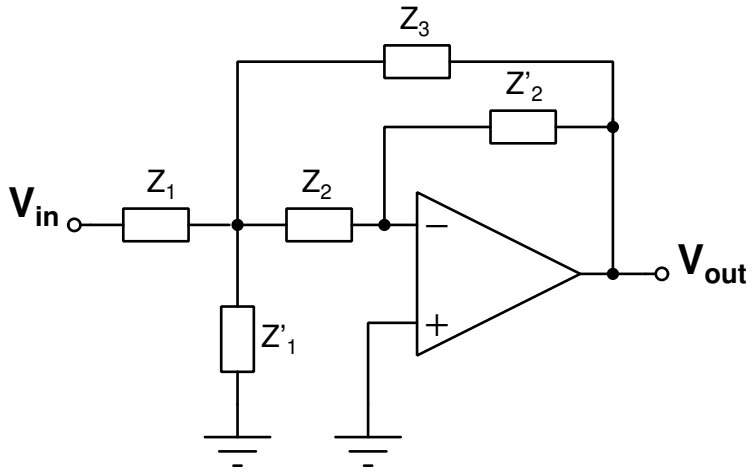

Figure 1.14 – Model of a Rauch biquad cell.

Another common type of biquad cell that uses a single amplifier is the Rauch model, which can be seen in Figure 1.14. This amplifier does not work as a buffer. Instead, it uses the amplifier in an inverted configuration and with a reference to the ground. This way, having this amplifier with a $0dB$ gain means trying to get the node "-" as close to the ground as possible. Any other desired gain value may come from the difference between the voltage in this node and ground, and it will be amplified by the closed-loop DC gain of the amplifier and the impedances Z_2 and Z_2'. Like the Sallen-Key topology, the Rauch is susceptible to parasitic capacitance, although in a lower degree.

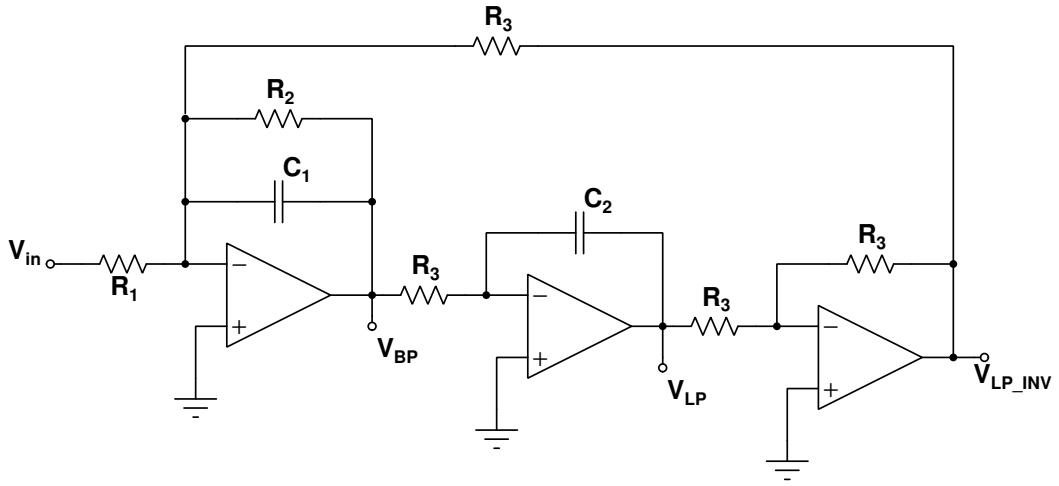

Figure 1.15 – Example of a Thomas-Tow biquad cell.

Both the Sallen-Key and Rauch topologies are usually more focused on power efficiency since they utilize only one active element to achieve the 2 poles of the biquad. This however makes them susceptible to parasitic capacitors in specific nodes. One of the alternatives to mitigate this is to use the amplifier to define both poles. The Tow-Thomas

biquad, as can be seen in the example of Figure 1.15, is one of such filter topologies. This filter topology also has the benefit of having the amplification in two or more different stages. That can be useful for designing one stage for gain, and another as buffering for driving the desired output load. This is especially true for the single-end version as shown in Figure 1.15, in which the last amplifier works to invert the signal. In a fully differential application, this last amplifier is typically excluded, and instead, the output lines are crossed. Its main disadvantage is the great number of components, which can be especially troublesome in IC applications with restricted silicon area. Also, since this topology needs more than one amplifier, it usually consumes more current than an equivalent Sallen-Key or Rauch biquad.

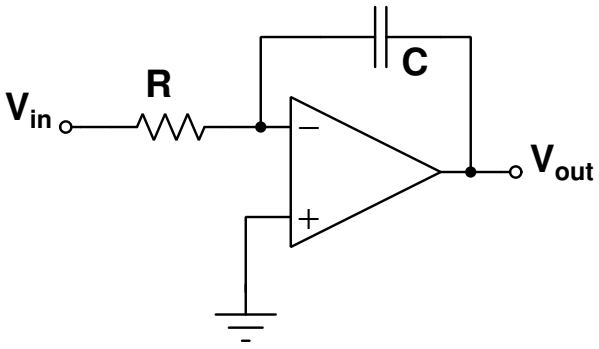

Figure 1.16 – Example of a 1^{st} low-pass Active-RC filter.

Besides the biquads, which are integrator circuits with 2 poles, other types of filters can utilize active elements to allocate poles and zeros for filters. The two most common are the Active-RC and the Gm-C filters. The first one was, in fact, a part of the Rauch biquad previously explained. This can be easily seen by comparing Figures 1.14 and 1.16. Like in a passive filter, the pole is defined by the passive elements, R and C, but the operational amplifier (opamp) design can help prevent the signal attenuation that would happen with the passive filter. This topology also is sensible to parasitic capacitance, especially in the output node (V_{out}). It is usually implemented together with a biquad to achieve an odd-ordered filter, like 3^{rd} of 5^{th} order.

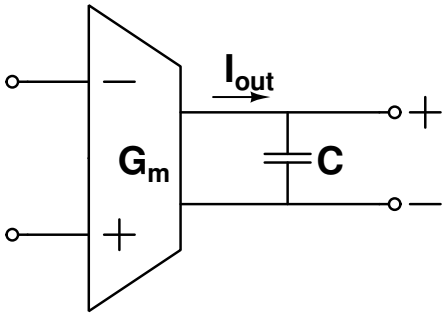

Figure 1.17 – Example of a 1^{st} low-pass Gm-C filter.

The other common topology, Gm-C, uses the transconductance of a transistor

to drive a capacitive load. This can be implemented, for example, using an Operational Transconductance Amplifier (OTA) with a fixed capacitance load. This kind of filter is interesting for using a current-driven element, like the OTA, which usually doesn't have a problem when driving low-impedance loads. It's also easier to design OTA than Opamps, which can be interesting in IC applications. This device can, however, have multiple and larger components, and in some cases have higher current consumption.

As previously said, all these topologies are circuits that can have the same behaviour as a desired filter approximation in the frequency domain. This means that, during the design process, the topology transfer function must match the approximation chosen. To demonstrate this, consider the following:

$$H(s) = -\frac{1}{s \cdot R \cdot C} \tag{1.4}$$

Equation (1.4) shows the transfer function of the ideal Active-RC filter seen in Figure 1.16. R is the resistance and C is the capacitance of the circuit. This is the equation that must be matched to a 1st order Chebyshev low-pass functions:

$$|H(s)|^2 = \frac{1}{1 + \epsilon^2 \cdot (C_n(s))^2 \cdot s/\omega_c} \tag{1.5}$$

where ϵ is the maximum tolerated ripple in dB; ω_c is the desired cutoff frequency in rad/s, and $C_n(s)$ is the Chebyshev polynomial of order n. The first two parameters are defined in the project of the filter, according to the application. The last one is directly tied to the desired filter order, as more parts of the polynomial will increase the number of poles of $H(s)$. By matching Equations 1.4 and 1.5, the resulting values of R and C lead to the desired Chebyshev response. Further details can be found on multiple works, such as [9].

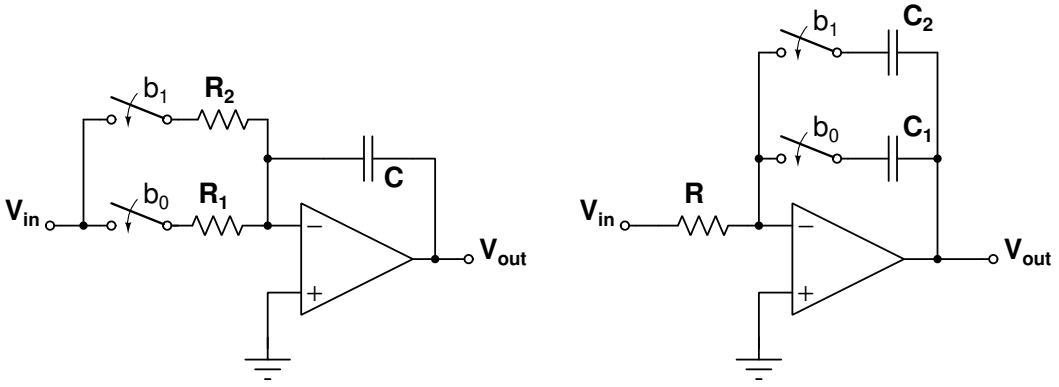

Figure 1.18 – Example of two 1^{st} low-pass Active-RC filters, with variable cutoff frequency; the first varies the resistance in the loop, and the other varies the capacitance.

Therefore, a direct relation between the cutoff frequency f_c (or ω_c) and the passive components of the nets can be established. So, if the filter application needs more

than one frequency configuration, it is possible to change the values of either R or C to change the poles of the filter. Figure 1.18 shows two possible designs using this principle. Using, for example, a single bit b, the filter can alternate between states b_0 and b_1, that can be, for example, the two bandwidth frequencies of $20MHz$ and $40MHz$ of an 802.11n (Wi-Fi 4) radio [3].

It's important to notice that, although in frequency response the variation of the values of the resistance or capacitance might see the same, this may not be the case when considering other factors. For this specific circuit, changing the value of R can change the perceived Z_{in} of the filter, which can be significant for the previous circuit in the chain. Also, changing the value of C will change the Z_{out}, which can impact both the matching with the next circuit in the chain and the amplifier of the circuit in both driving capability and stability.

This approach of switching between different passive elements is very common, as this represents a more straightforward way of design: changing the values directly changes the position of the pole, so if all the other effects are considered, it's just a matter of calculating the desired capacitance/resistance. But, as commented, these solutions may have changed the characteristics of the circuit in an undesired way. They can also get bulky very quickly, or be more susceptible to variations in temperature and/or in the fabrication process. For some topologies, however, there are alternatives to this method.

The MOSFET-C topology, as shown in Figure 1.12, uses a voltage V_c to change the characteristics of the transistor M in the Triode region. Using the MOS transistor equation for this region:

$$I_d = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{gs} - V_t)V_{ds} - V_{gs}^2] \tag{1.6}$$

It's possible to establish a direct relationship between the voltage and current in the transistor, which is equivalent to a resistor. This way, changing the voltage difference between gate and source (V_{gs}), V_cr in the circuit of the figure, it is possible to vary the equivalent resistance and, therefore, to change the cutoff frequency.

Besides these two options, the Gm-C filter also uses the transistor as an element for defining the poles of the filter. Similar to Equation (1.6), if we consider the transistors in the OTA of a GM-C filter like in Figure 1.17, we can define the transconductance as:

$$g_m = \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_t) \tag{1.7}$$

This is very similar to the equation of the transistor in the saturated region:

$$I_d = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 \tag{1.8}$$

This allows establishing a relation between the drain current I_d and the transconductance g_m, which is defined as:

$$\frac{g_m}{I_d} = \frac{2}{(V_{gs} - V_t)} \tag{1.9}$$

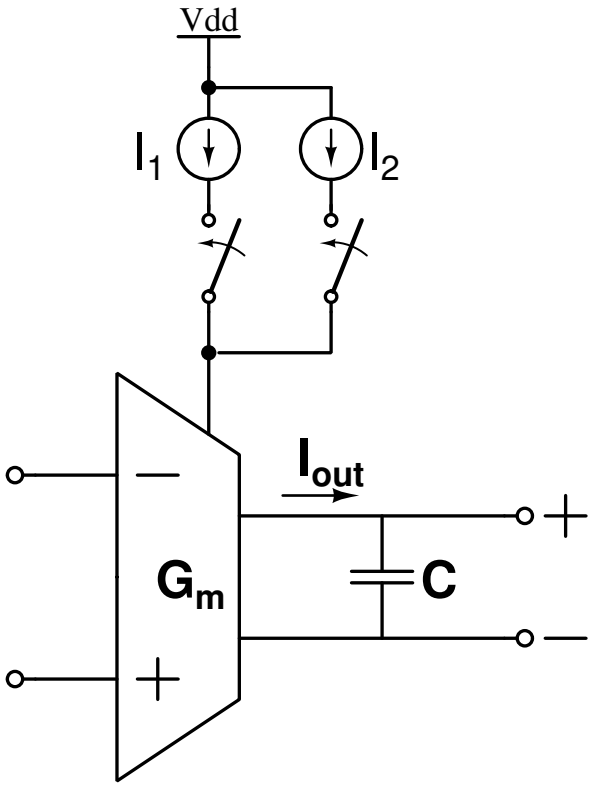

Figure 1.19 – Example of a 1^{st} low-pass Gm-C filter with variable cutoff frequency by varying its bias current.

Therefore, using Equations (1.7), (1.8) and (1.9), we can see that, for a fixed value of gate voltage V_{gs}, the value of the transconductance is directly proportional to the current. Using a circuit like the one in Figure 1.19, we can change the current fed to the circuit of the OTA and, therefore, change its equivalent transconductance and the pole it defines.

These three techniques have been the focus of some studies on how to design variable analog filters. In [10], which is one of the main books on this subject, it is compiled a series of works about this area. There are some works, like [11], about the transconductor of a Gm-C type filter, with a variable OTA cell, also called Variable Transconductance Amplifiers (VTA). Works like [12] investigates traditional approach of having switchable passive components in the network. They try to mitigate power and offer more gain/drive flexibility, by jumping stages when needed.

Some innovation comes from [13], with an approach that seems to mix some of the previous works. Using a fixed Active-RC filter, but varying the current feed of the output stage to change the position of the pole of the integrator. Another different approach comes from [14]. It uses a GmC type filter that also changes the amplifier transconductance, but it does so using by changing the polarization of stacks in a folded cascade topology.

2 Schematics Design

Considering the project parameters developed in section 1.2 and the theory presented in section 1.3, we can now make choices in the filter design. This will define the circuit's overall format, what components will be used and how we can get the desired frequency response. After that, we define the overall circuit parameters and the amplifier circuit design. With all the parts of the circuit design, we use a simulator to input these values and check whether the results are as expected.

2.1 Topology Definition

As seen in Section 1.3, the traditional approach for filter design is the cascade of multiple identical cells per the desired order. Therefore it's only needed to design the base cell, called a biquadratic cell. This name comes from the fact the circuit adds two real poles to the system transfer function, and you choose your components to define these poles in a frequency response graph. It's also of our interest to use active filters. As seen in Section 1.2, since we have to use a 6th order or higher filter, building all the stages with passive filters can lead to excessive attenuation.

Looking now to the biquad cell, choosing what topology helps to determine which parameters will be available for the design later. Considering the mains topologies of Section 1.3, we can choices between Sallen-key, Rauch, or Thomas-Tow. The first two use a combination of a passive and an active section to determine the 2 poles. This helps the design shrink in size and have lower power consumption, but can offer challenges with sensitivity to parasitics and drive speed. On the other hand, the Thomas-Tow usually has a bigger area footprint and consumes more power, as you need 2 or 3 amplifiers for the circuit.

Since reducing area is a priority, we prefer the two first circuits. While choosing between Sallen-Key and Rauch, the latter is chosen for being more sensitive to the amplifier operation. A diagram for the single-ended model of the Rauch biquad can be seen in Figure 2.1.

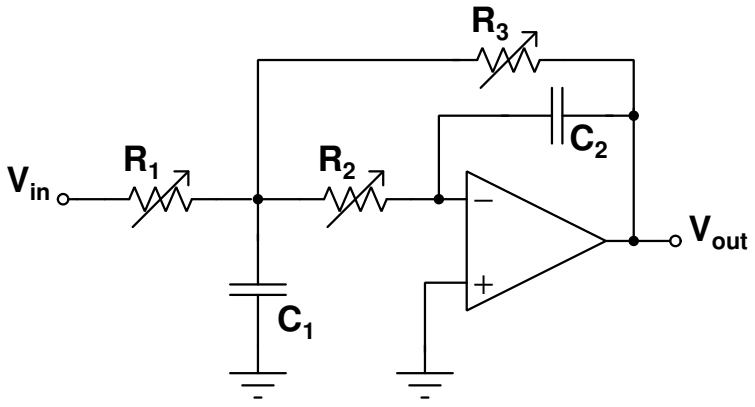

Figure 2.1 – Example of a Low-pass filter implemented using a Rauch topology.

2.2 Circuit parameters calculation

With the topology defined, we can begin the design process by using the frequency response. This allows us to match the frequency of f_{3dB} to the desired value for the project. The Laplace domain transfer function using the Rauch topology [8], can be written as

$$H_{LP}(s) = \frac{1}{R_1 \cdot R_2 \cdot C_1 \cdot C_2 \cdot s^2 + C_2 \cdot (R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3}) \cdot s + \frac{R_1}{R_3}} \tag{2.1}$$

where the values of R and C are according to the model shown in Figure 2.1. For simplicity of design, we make all the resistances and capacitances proportional to fixed values, i.e.

$$\begin{aligned} R_1, R_2, R_3 &\propto R, \\ C_1, C_2, &\propto C, \end{aligned} \tag{2.2}$$

As any frequency ripples are undesired for our application, we need to apply the Butterworth criteria for maximum flatness in the pass-band section of the filter. Therefore, we find:

$$\begin{aligned} C_1 &= 2 \cdot C_2 \\ R_2 = 2 \cdot R_1 &= 2 \cdot R_3 \end{aligned} \tag{2.3}$$

where R and C are now arbitrary values that we can choose based on the project specifications. Let's now consider that, to minimize our design footprint area, we can choose to use only one value of C, changing only the value of R. With these considerations, the transfer function defined by (2.1) can now be used to find the value of the cutoff frequency as seen below:

$$H(s) = \frac{1}{(1 + s \cdot R \cdot C)^2}, \qquad f_c = \frac{1}{4 \cdot \pi \cdot \sqrt{2} \cdot R \cdot C}; \tag{2.4}$$

Using Equation (2.4) and a fixed value of capacitance, we can find the values of resistance as:

$$C = 120fF, \quad R_{eq} = 11,7k\Omega \quad @40MHz \quad R_{eq} = 496,9k\Omega \quad @1MHz \tag{2.5}$$

As can be seen, these values are significantly far from each other. This means that the number of resistors would be high. Even if we were to use multiple capacitors, the area penalty for this kind of solution is too high. To circunvent this problem, we use the approach of a MOSFET-C type filter, where the resistor is substituted by a triode polarized transistor. This allows us to make the following equivalence:

$$R_{eq} = \frac{V_{SD}}{I_d} = \frac{L}{W} \cdot \frac{1}{\mu C_{ox} \cdot (V_g - V_t)} \tag{2.6}$$

were μ,C_{ox} and V_t are parameters of the transistor, defined by it's technology and it's polarization [15]; V_g, W and L are values that can be defined by design, so as to match R_{eq} to our desired values of R found in Equation (2.5). Since the width (W) and length (L) of the transistor cannot be changed after fabrication, our control variable is the MOS Gate Voltage (V_g), which we will call Control Voltage V_c. Therefore, we can simplify the equation to:

$$R_{eq} = K_1 + K_2 \cdot \frac{1}{V_g}, \qquad K_1 = \frac{L}{W} \cdot \frac{1}{\mu \dot{C}_{ox} \cdot V_t}, \qquad K_2 = \frac{L}{W} \cdot \frac{1}{\mu \dot{C}_{ox}}, \tag{2.7}$$

where there is a linear relationship between the resistance and the control voltage, as long as the constants K_1 and K_2 are defined.

To better control the gate voltage, the linear scale is substituted by a step-ladder scale. This allows for the integration with a more simple and reliable system, like a DAC ladder output or a precision resistor ladder that can be implemented after validation. For

this approximation, it's important to consider a step that allows for the 1MHz frequency tuning.

Evaluating other DACs in commercial solutions, we chose the value of 5mV steps in a full-scale voltage of 0.6V, which is the core voltage of our technology. This gives more flexibility in the future for either an internal (SoC) or external solution. With a 5mV step and a 0.6V full-scale, we have a 7-bit ladder across the range, with about 128 possibilities. This is more than the 40 needed re-configurations, but if we think on the work of a lookup reference table for the frequencies after calibration, this solution is more appealing. It will also be useful in the future when we discuss robustness and calibration steps. For the schematic-only analysis, using a range from 1MHz to 40MHz and step of 1MHz; we find an equivalent range from 45mV to 320mV.

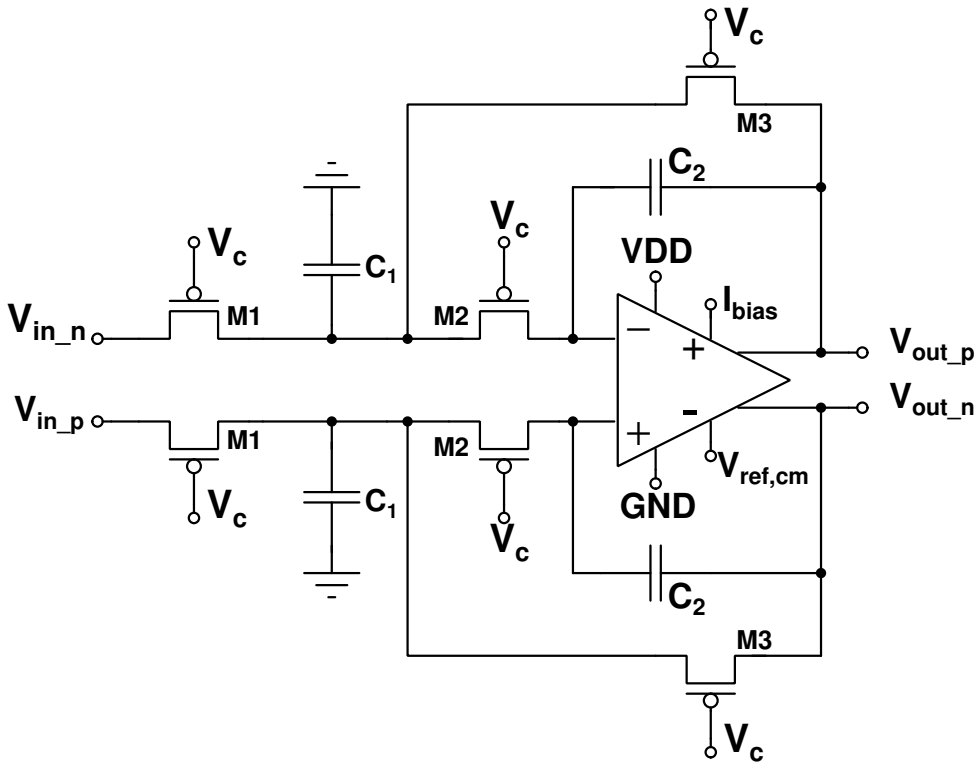

Figure 2.2 – Schematic of the implemented solution using a 2nd Order block (Biquad cell).

Figure 2.2 shows the implementation of the Rauch Biquad topology in the proposed MOSFET-C configurations. The design is made fully-differential, to reduce even-numbered harmonics and following other blocks in the receiver chain. The next step now should be to design the Amplifier. To meet the goal of low power and low footprint, the circuit should be the simplest possible. It must, however, meet certain requirements:

- Must maintain a 600mV DC level in single-end operation, maximizing dynamic range.
- The cutoff frequency of the amplifier must be higher than that of the filter.

- The circuit should be able to drive the load of the passive components.
- The circuit should be stable across the frequency range.

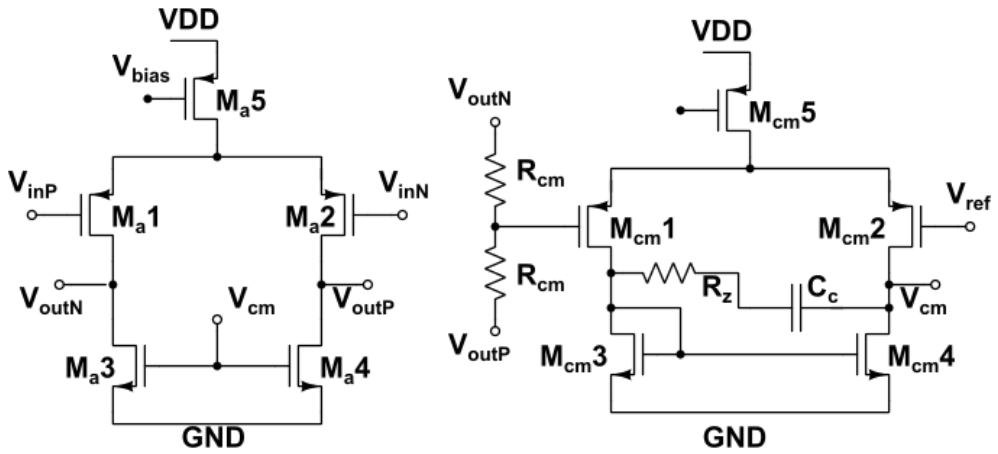

Figure 2.3 – Schematic of the amplifier utilized in the biquad cell

With this in mind, a single-stage amplifier is designed to meet these requirements, as shown in Figure 2.3. The Amplifier has an expected gain of 20dB, which is not high but is enough, and a cutoff frequency around 60MHz. Also, as a single-stage amplifier, it's always stable and has a compact footprint. The topology utilized is a simple common-source, with a Common-mode Feedback (CMFB) amplifier regulating the load in the main amplifier.

After the conclusion of this step, we can begin integrating the circuit in schematics level and simulate the circuit, to verify if the results are coherent. The final dimensions used with the TSMC 65nm CMOS LP MS/RF ®can be seen in Table 2.1.

Table 2.1 – Dimensions and values for the Proposed Circuit

Device	Dimension
$M1$, $M3$	0.95/0.2 μm
$M2$	1.9/0.2 μm
M_a1, M_a2	12/0.1 μm
M_a3, M_a4	4/0.1 μm
$M_{cm}1$, $M_{cm}2$	12/0.1 μm
$M_{cm}3$, $M_{cm}4$	4/0.1 μm
R_{cm}	50 $k\Omega$
R_z	1.2 $k\Omega$
C_c	300 fF
C_1	120 fF
C_2	240 fF

2.3 Test-bench and Schematics Results

In this section, we present the testbenches developed for evaluation of the circuit, as well as the results for them. All the simulations have been performed using the software Cadence® Virtuoso® Analog Design Environment (ADE) and Schematics Editor, alongside TSMC 65nm Low-Power CMOS technology. The results presented are plotted using MATLAB® R2015-b. All these simulation tools are licensed to Eldorado Research Institute.

It's important to comment that the voltages, V_{cm} and V_{ctrl}, as well as the supply voltage and ground, are all external, provided by a test board to the IC through a wire bond. Although these are all DC signals and should have a minimal impact by this configuration, the parasitic model shown in Figure 2.4 is used with values for the capacitance and resistance taken from the datasheet files. Using these values, the wire-bond inductance is given by $L_{wb} = 4nH$, using the model of a single wire over a ground plane. This model is reproduced using ideal components in the simulation environment.

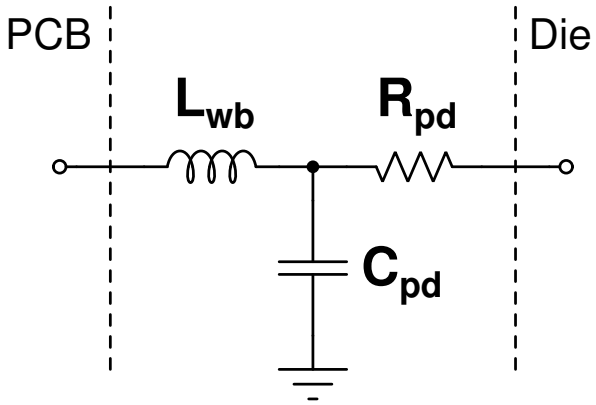

Figure 2.4 – Circuit model employed for the PAD, IO circuity and Wire-bond of the IC.

2.3.1 Amplifier Simulated Results

The first testbench presented applies to the amplifier used in the biquads. Figure 2.5 shows the testbench developed for it. The load capacitance $C_L = 200pF$ is calculated to include both the feedback loop capacitance, the next stage, plus a small margin for parasitic capacitance. The main evaluated features for this testbench are:

- Stability and cutoff frequency, using AC evaluations and Bode diagram;
- DC performance for the CMFB circuitry, as well as polarization for the transistors of the amplifier;
- overall qualitative transient response.

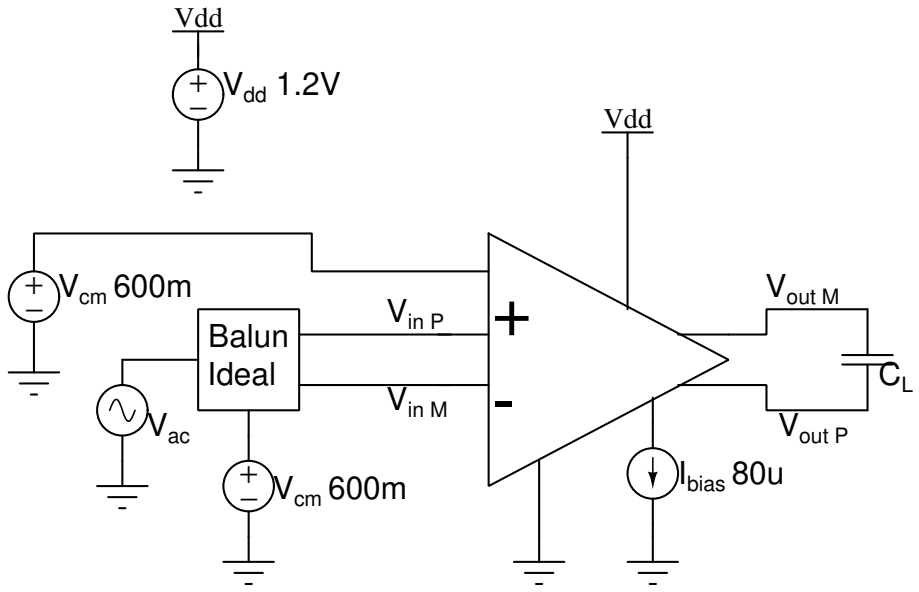

Figure 2.5 – Testbench for the individual amplifier used in the biquad circuit.

The results for this testbench can be seen in Figures 2.6 and 2.7, while the numerical values can be seen in Table 2.2. As previously stated, the single-stage amplifier is always stable, so the value for Phase Margin is expected to be above 90°. The tradeoff in this amplifier design is the frequency of 3 dB, DC Gain, and power. Having a higher gain would require a two-stage amplifier, and this would require a typical Miller compensation or another approach for stabilization, and this approach severely reduces the cutoff frequency.

Table 2.2 – Evaluation of the biquad amplifier

Metric	Value	Unit
f_{3dB}	43.3	MHz
Phase Marg.	97	° (deg.)
DC Gain	17.2	dB
DC Current	290	μA

2.3.2 Performance of Simulated Results

The filter is evaluated directly using the 6^{th} Order configuration, with the 3 biquads in cascade. Integrated with the circuit is also a series of MOS-based current mirrors, to reproduce the reference current to each amplifier. The load capacitance is $C_L = 100f$, as calculated for the subsequent block. Figure 2.8 shows the general schematic for this testbench. The main evaluated feature here is the AC performance, specifically the frequency response and cutoff frequency. As the last one, the transient signal and DC output level are also evaluated.

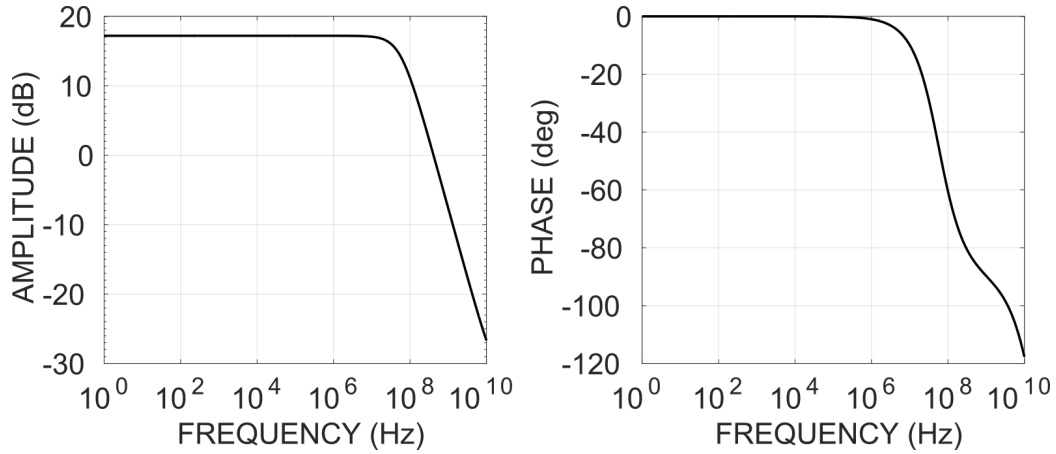

Figure 2.6 – Frequency Response for the amplifier designed for the biquad circuit.

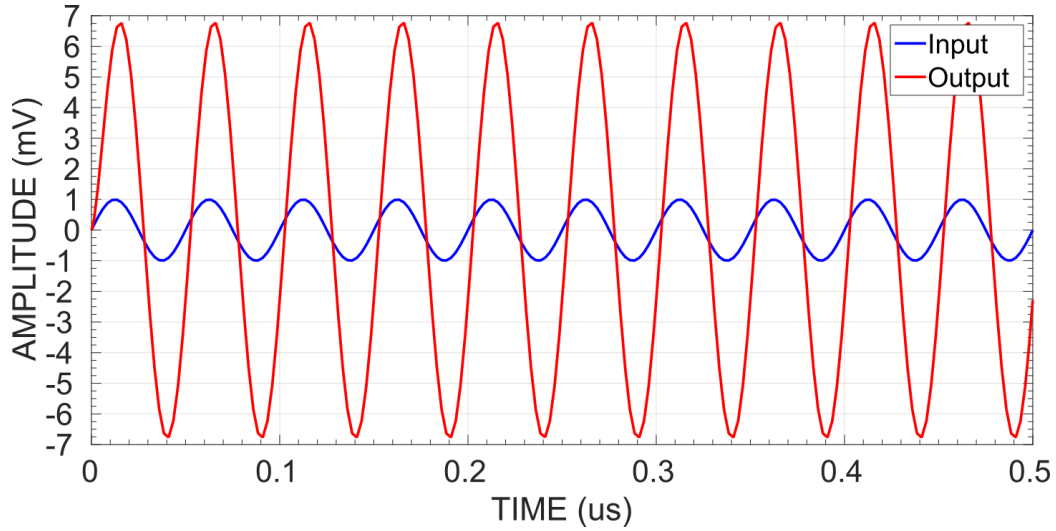

Figure 2.7 – Time domain response for the amplifier designed for the biquad circuit, using a 20MHz sinusoidal signal.

As can be seen in Figure 2.9, the filter frequency response is coherent to the Butterworth criteria, maintaining a flat frequency response on all the pass-band. We can also see the gate control voltage is inversely proportional to the cutoff frequency, as expected since we are using PMOS transistors for the MOSFET-C design. One consequence of the amplifier choice is a noticeable attenuation in the pass-band of the filter, which can achieve levels close to -16dB. However, since the filter has a high enough selectivity (36db/Octave), this issue can be compensated through the gain chain following the filter. Figure 2.10 shows the time domain response, with a wave composed of a 20MHz signal and a 100MHz interferer in the input of the filter. We can see that although the main component is attenuated, the interferer is completely removed from the signal, as desired by a 6^{th} order LP filter.

Finally, as a way to evaluate the filter capability for reconfiguration, we evaluate Figure 2.11. This curve is made by sweeping the control voltage V_c and evaluating, for each, the correspondent cutoff frequency f_{3dB}. This sweep is similar to the DAC ladder

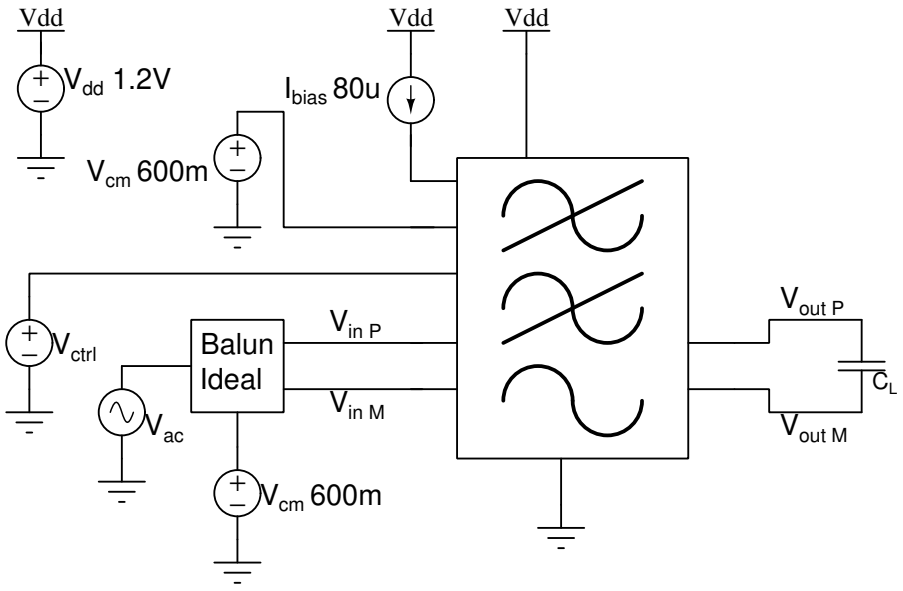

Figure 2.8 – Testbench for performance analysis of the complete filter, with the three stages in cascade.

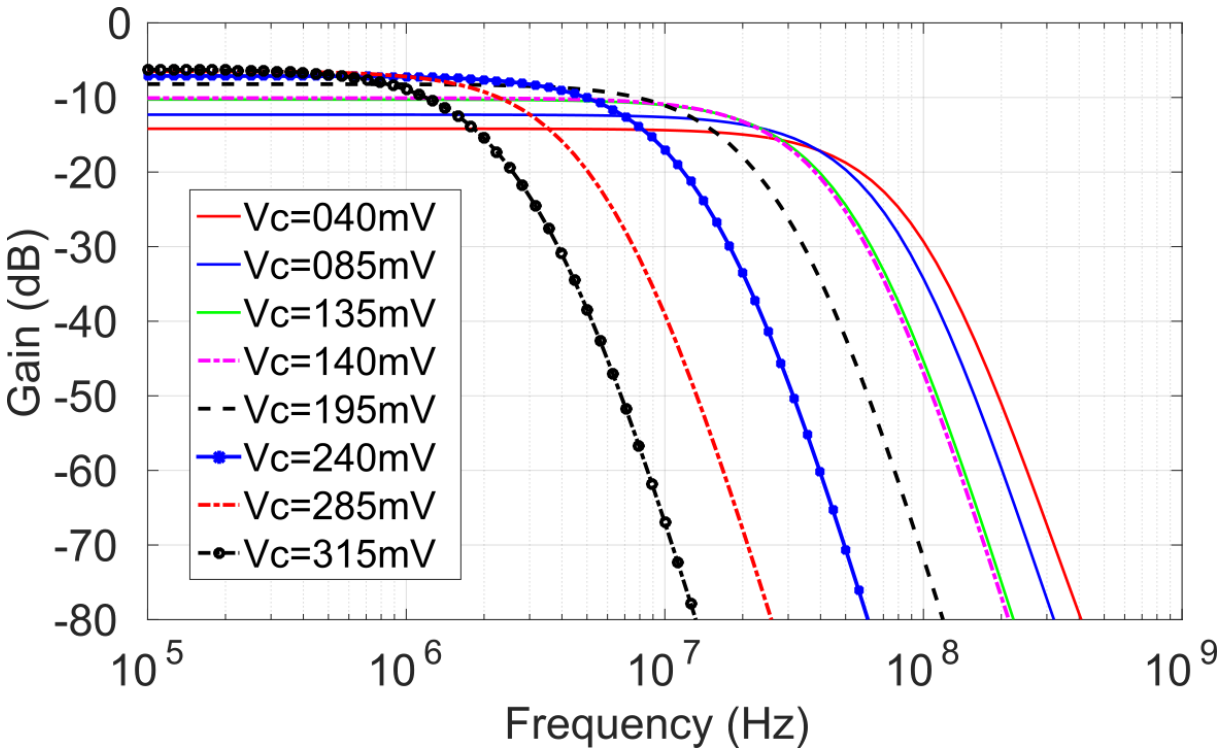

Figure 2.9 – Filter response for different control voltages, varying from 1MHz to 40MHz cutoff frequency.

output cited early in Section 2.2. We can see that, as expected, the frequency behaviour is very similar to a PMOS I_d vs V_g curve, which can be seen in multiple works like [16]. As we are using the transistor conductivity to determine the cutoff frequency, this is what we desired. It's important to notice, however, that the curve has a non-linearity after around 200mV, where the transistor stops operating in the Triode state and starts entering sub-Threshold. This isn't considered a problem for two reasons: first, the linear region

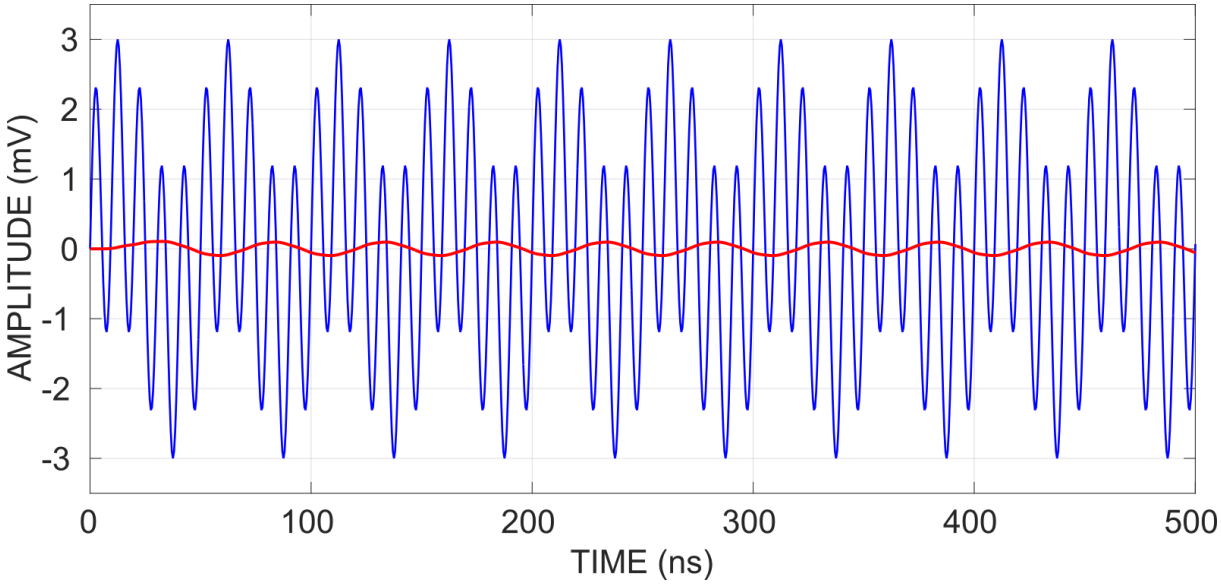

Figure 2.10 – Filter time domain response, filtering a modulated signal.

already covers most of the desired frequency range; second, the non-linearity makes the transistor less sensible to changes, and therefore an increase in the number of steps is enough to achieve desired frequencies.

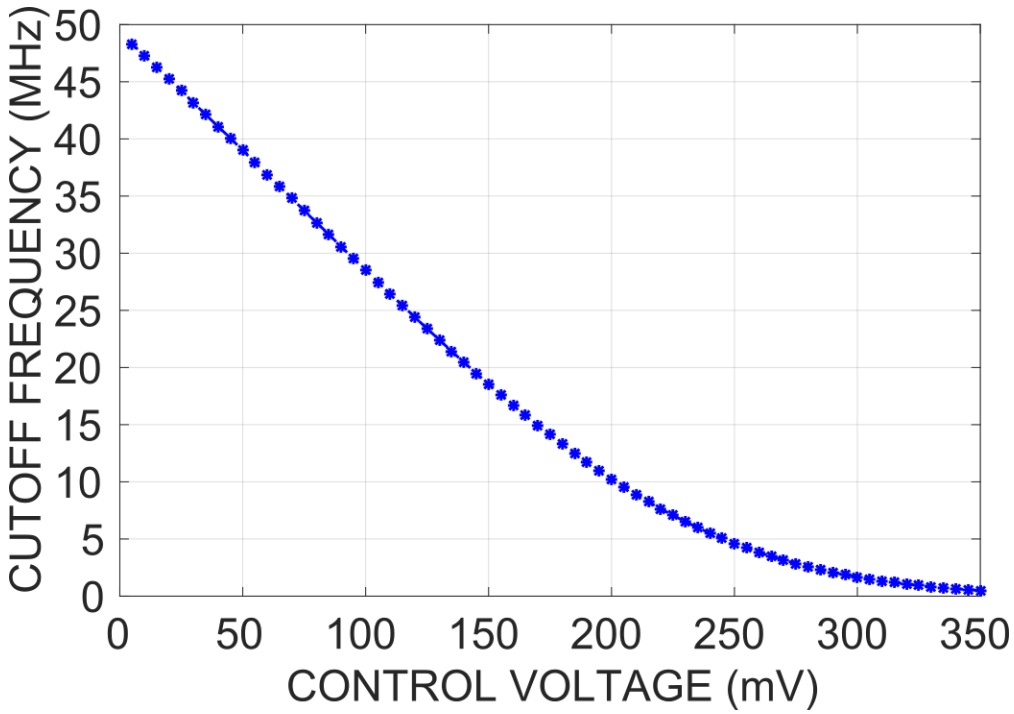

Figure 2.11 – Curve for the filter cutoff frequency versus control voltage, which defines the filter reconfigurability.

2.3.3 RF Metrics

Finally, the last testbench is to evaluate RF metrics, demonstrated in Figure 2.12. It's very similar to the previous one, but the ideal AC source is changed to a Port

with a defined R_{in}. This input impedance is an important factor for these metrics, and its value is defined by the circuit before the filter. In a direct testbench, this value is defined by the measuring components; but in a receiver chain, this is defined by the preceding block, the Mixer. In this case, the value is $R_{in} = 1.3k\Omega$.

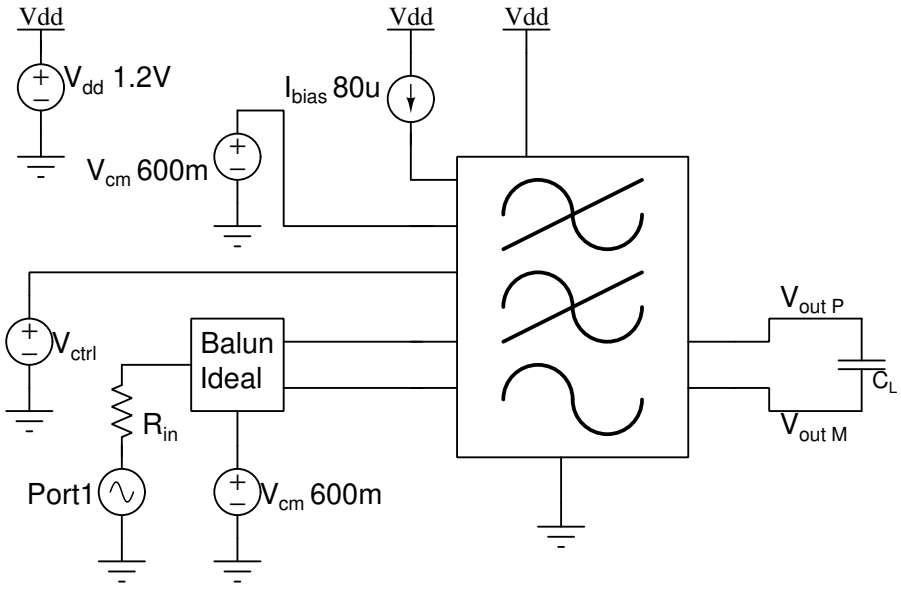

Figure 2.12 – Testbench for RF metrics evaluation of the complete filter, with the three stages in cascade.

It's also important to note that, as it was explained briefly in Section 1.2, the filter is generally very sensitive to impedance matching and coupling with other circuits. Therefore, the value of R_{in} is set by the output impedance of the buffer, used to match that of the filter with the small value, i.e., the performance for a cutoff frequency of 40MHz. With this value in mind, the curves simulated with the testbench can be seen in Figure 2.13 and 2.14. Both the noise and compression performance are better than the previously specified value. The specific number will be compared to other works for further evaluation.

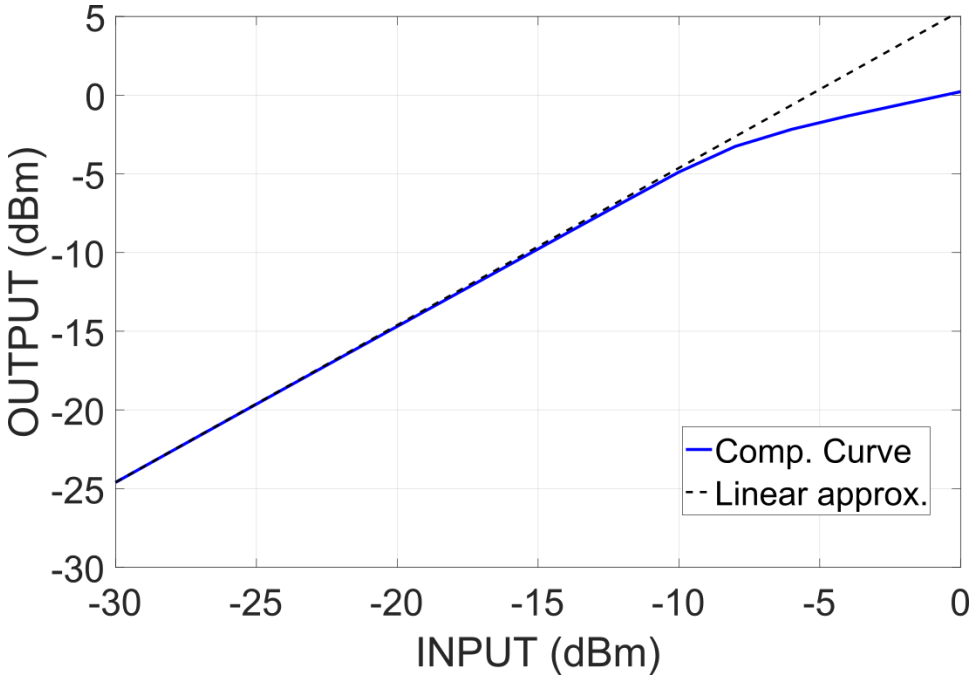

Figure 2.13 – Curve for the 1dB compression point

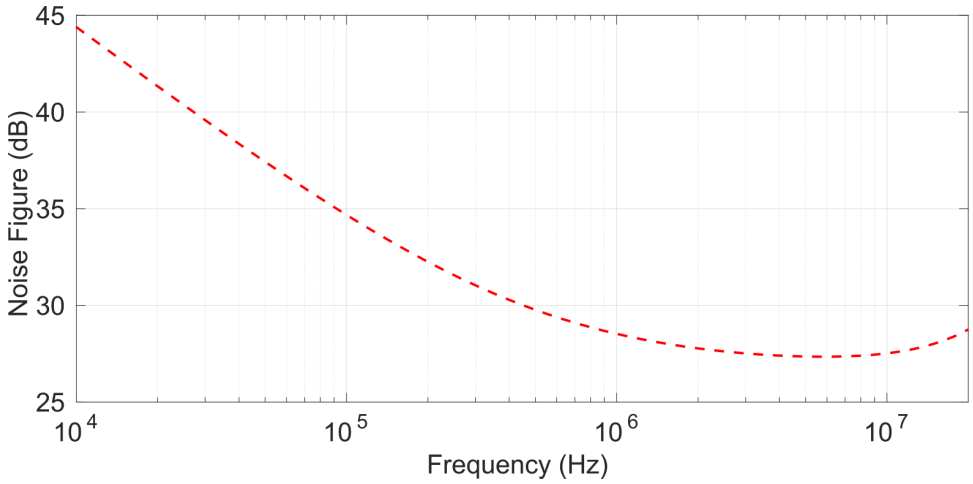

Figure 2.14 – Curve for filter noise figure.

3 Robustness Analysis

With the circuit topology defined and implemented in a chosen technology, the next step, in the design process for an analog integrated circuit, is the evaluation of the robustness. All circuits can change their behaviour depending on the conditions, and it's important in the design cycle to try and preview these variations. This can happen by either having a calibration step or by using more robust structures to minimize variations. This chapter will cover the two more common robustness analyses utilized in CMOS Analog IC design in two separate sections. The first one is the "Process, Variation and Temperature" (PVT) analysis, in which the circuit is subjected through the variation of each of these separately and then combined to investigate the worst-case scenario. The second one is the Monte Carlo Analysis, where statistical analysis is performed based on possible variations in the fabrication process.

It's important to choose what variables should be evaluated with the robustness analysis. Although going through all the specifications would be ideal, some of these are incompatible even on a simulator level. For example, to evaluate the compression 1dB point we need to make a sweep of variables and that's not compatible with the Monte Carlo analysis. For this work, we focus on the reconfigurability of the circuit and will use Figure 2.11 as a baseline guide for evaluating the filter frequency behaviour. The DC gain will also be seen in some stages as a cross-check, although not as thoroughly analyzed.

3.1 PVT Analysis

For the first robustness analysis, we will evaluate the three variables for common behaviour variation in CMOS circuits. The interaction between these variables can either compensate or intensify certain effects. For this reason, we will first investigate each effect separately.

For the first one, the process variation influence is shown in Figure 3.1. The CMOS process has some different stages for ion deposition, and depending on the time dedicated to these stages you can get different conductivity for either NMOS or PMOS transistors. These variations are signed by "s" for **slow** and "f" for **fast**. As the filter cutoff frequency is directly related to this parameter, we can observe a very severe variation in the filter response curve. The "Proc. tt" curve is the same as Figure 2.11 and is the "nominal" value for this analysis.

Although the variation in the curve is significant, further evaluation of Figure 3.1 shows that this variation do not occur on the linear part of the curve, therefore the desired principle of having at least 1MHz change in cutoff frequency per voltage step is

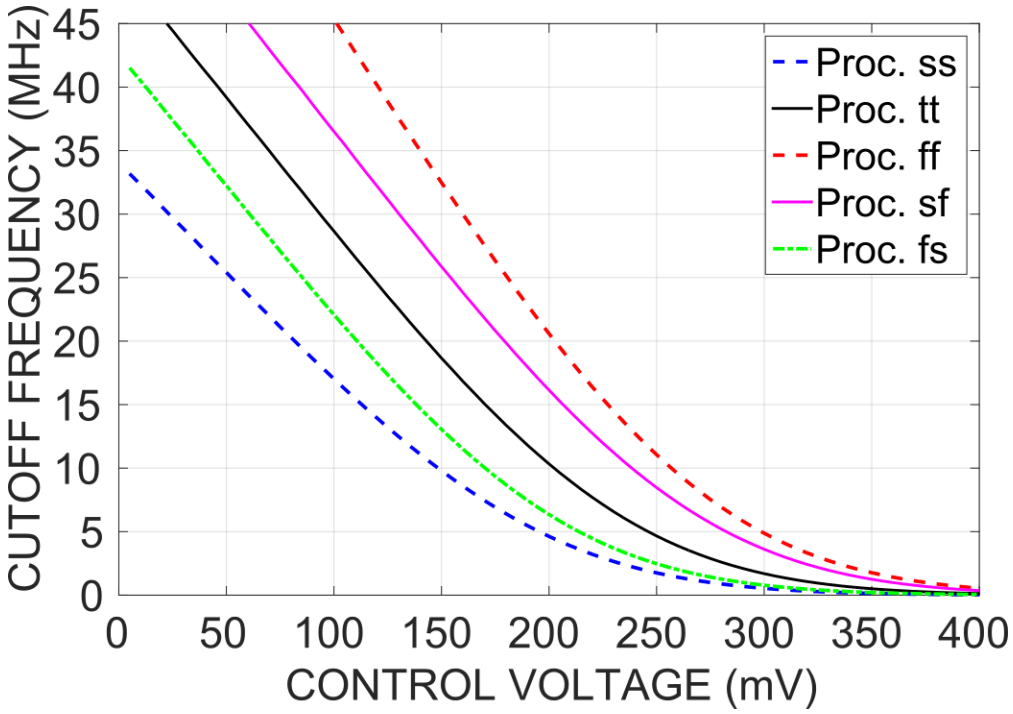

Figure 3.1 – Filter frequency response for different control voltages, analyzed according to CMOS Process variation.

still valid. Since the process variation only happens once, during fabrication, we can design the circuit to account for this variation. The results presented here and the values for table 2.1 already consider this. The maximum desired frequency of 40MHz is not achieved in all the cases, but as we shall investigate this in further analysis, this may not be statistically significant.

In the following, we evaluate the circuit response to voltage variation. A real test bench with a supply voltage set to $V_{DD} = 1.2V$ can be seen by the circuit as only $V_{DD} = 1.1V$, and therefore its behaviour will change.

Figure 3.2 shows that the cutoff frequency variations are very small. This is expected since the cutoff frequency isn't dependent on the supply voltage, as can be seen in Equation (2.4). These small variations, therefore, come from the changes in the amplifier. Table 3.1 show the variations for to the individual amplifier of the basic biquad cell. Specifically looking at the Gain Bandwidth Product (GBW), it is possible to observe that the value for both voltage variations is very similar. This is in accordance with the changes in Figure 3.2. As this variation doesn't affect the circuit significantly, we consider that this doesn't need a dedicated solution for correction.

Finally, we evaluate the temperature variation. There are several possible operating temperatures, but for this work, we followed the Extended Commercial Range defined by Renesas Electronics Corporation [17], which currently produces similar DVB-S2 and other RF tuners. The standard varies from $-20°C$ to $85°C$. Figure 3.3 shows the temperature variation for this range while considering standard operation at $27°C$.

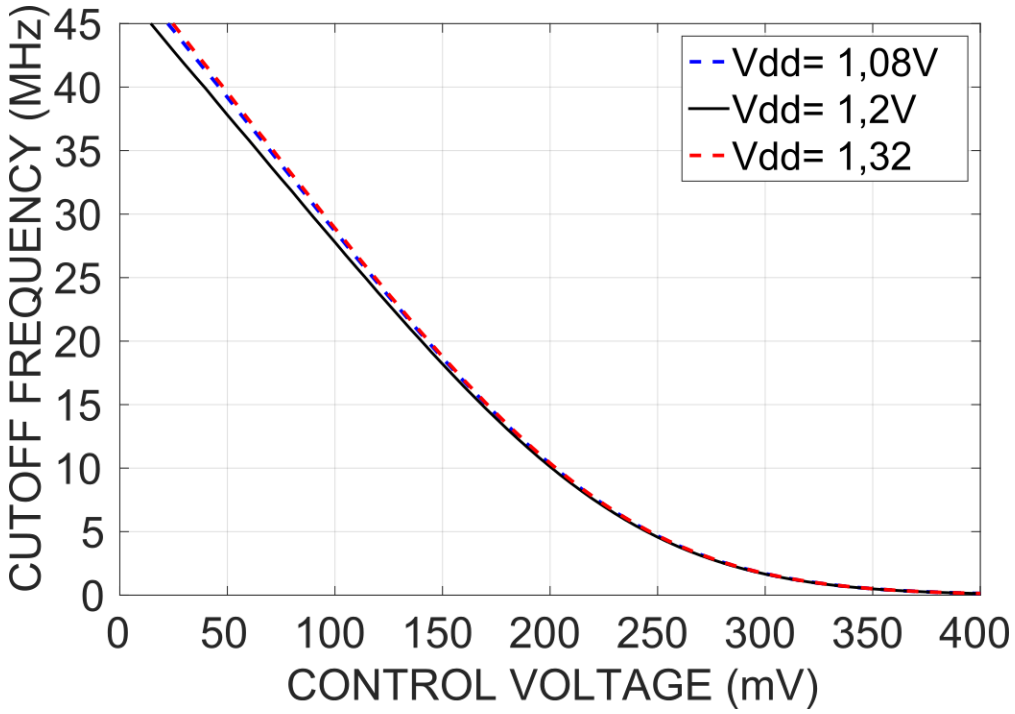

Figure 3.2 – Filter frequency response versus control voltages for different values of Supply Voltage.

Table 3.1 – Voltage Variation analysis in the biquad amplifier

Supply Volt.(V)	1,08	1.2	1.32
f_{3dB}(MHz)	30.6	43.4	48.5
DC Gain(dB)	16.3	17.2	17.4
GBW(MHz)	312.2	356.4	322.2

The curve shows a significant variation in the linear portion, which can be harmful. This is expected since the temperature change affects the transistor conductivity. To solve this, one possible solution is to adjust the voltage to compensate it, i.e. having the control voltage with a specific temperature-dependent relationship. Evaluating the variation in the linear coefficients of the curve, we can make the following approximation $T_c = 2.5m°C/V$. With these corrections, the resulting curve is shown in Figure 3.4. Evaluating the slope of these curves, it is possible to observe that the slope varies between $5.1mV/MHz$ and $4.45mV/MHz$, which is a lot closer to the desired values.

Finally, we evaluate the combination for these effects, and the results are presented in Figure 3.5. Here also we can see that the effects are similar to the curve subject to displacement on the X-axis, very similar to the effect due to Process variation. In fact, if we analyze the combined effect of Voltage and Temperature in different Processes, we see that this variation isn't as pronounced. Therefore, with the appropriate calibration of the circuit for each process, the response curve should be very similar across the remaining variables. This will be further explored in section 3.3, but a general view can be

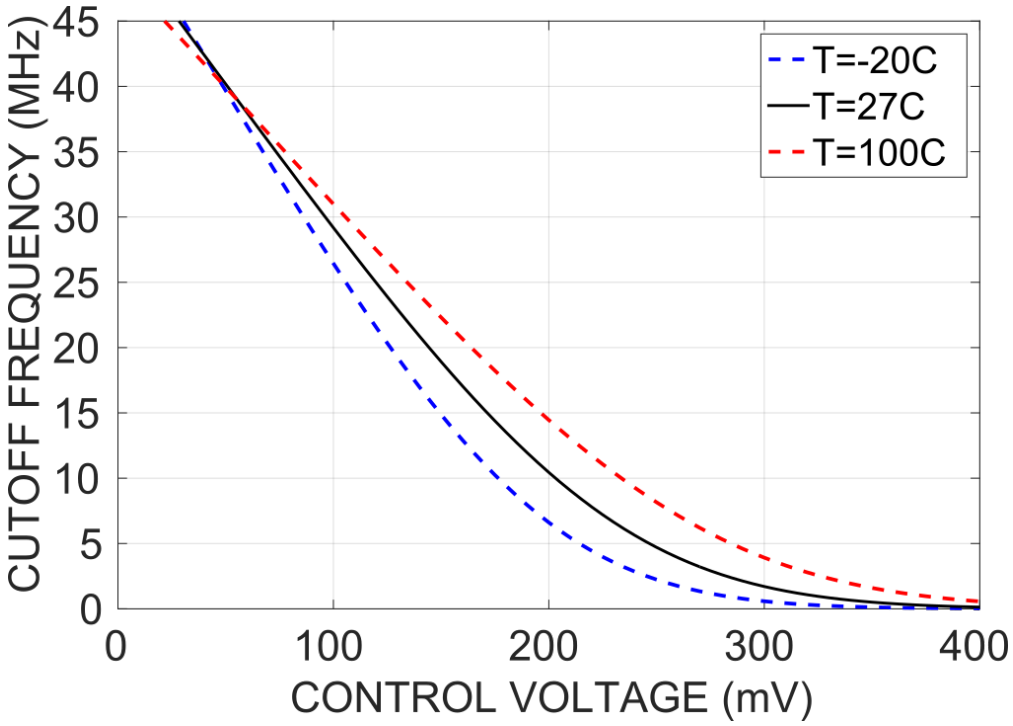

Figure 3.3 – Filter frequency response for different control voltages, analyzed according to Temperature variation.

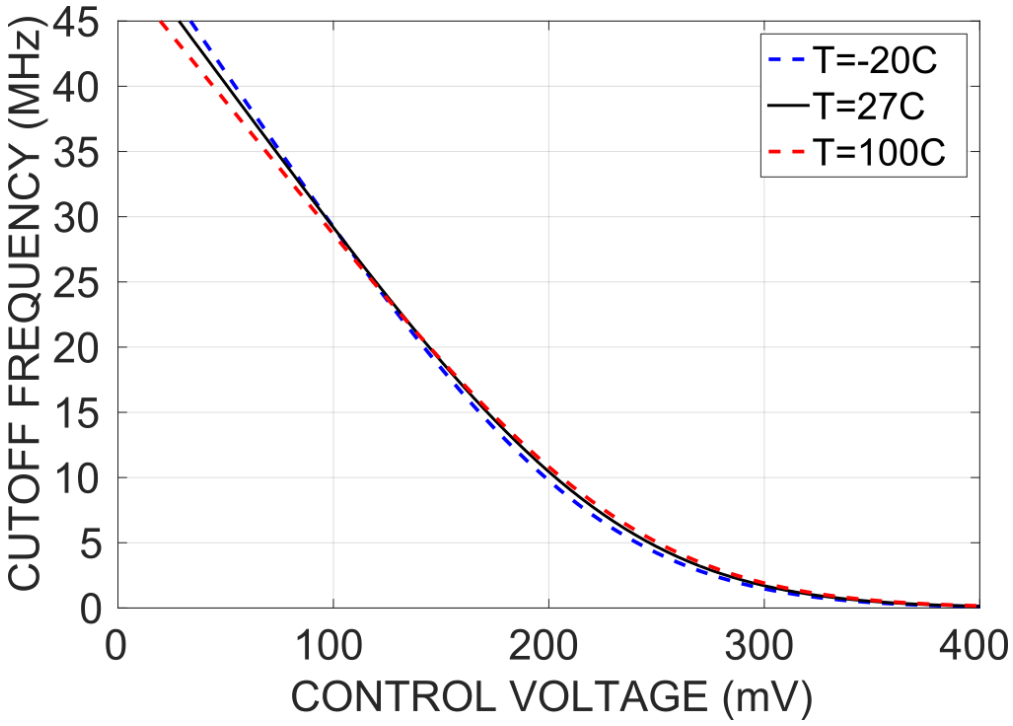

Figure 3.4 – Filter frequency response for a temperature-dependant voltage source.

seen in Figure 3.6. This is the curve for 3 voltages values for each one of the 3 different temperatures.

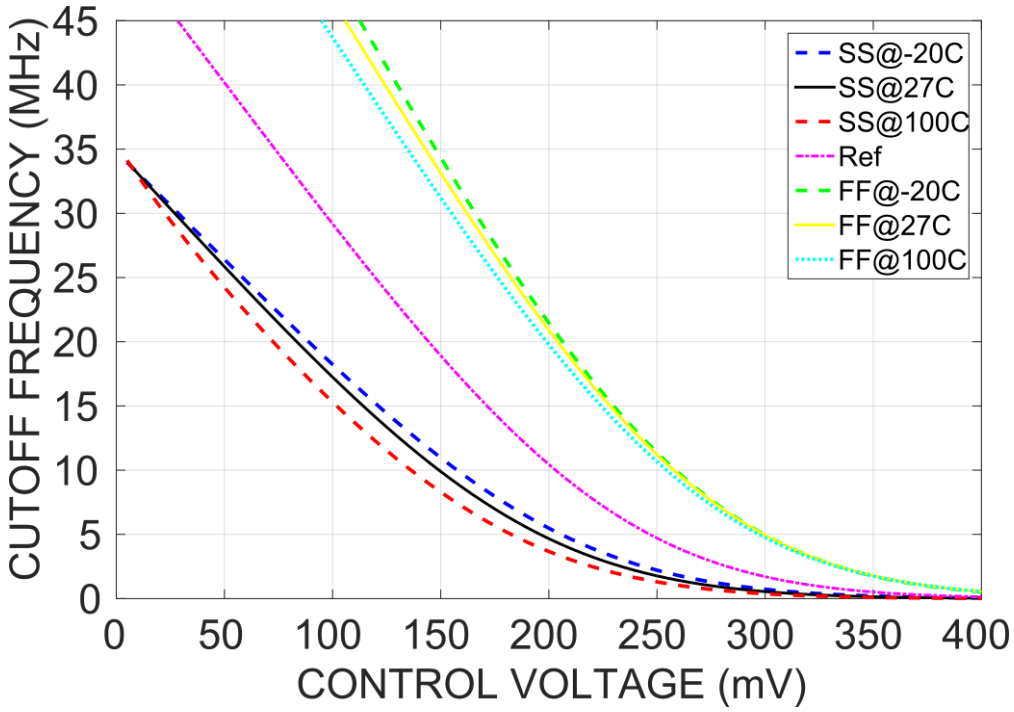

Figure 3.5 – Filter frequency response for different control voltages, for all PVT.

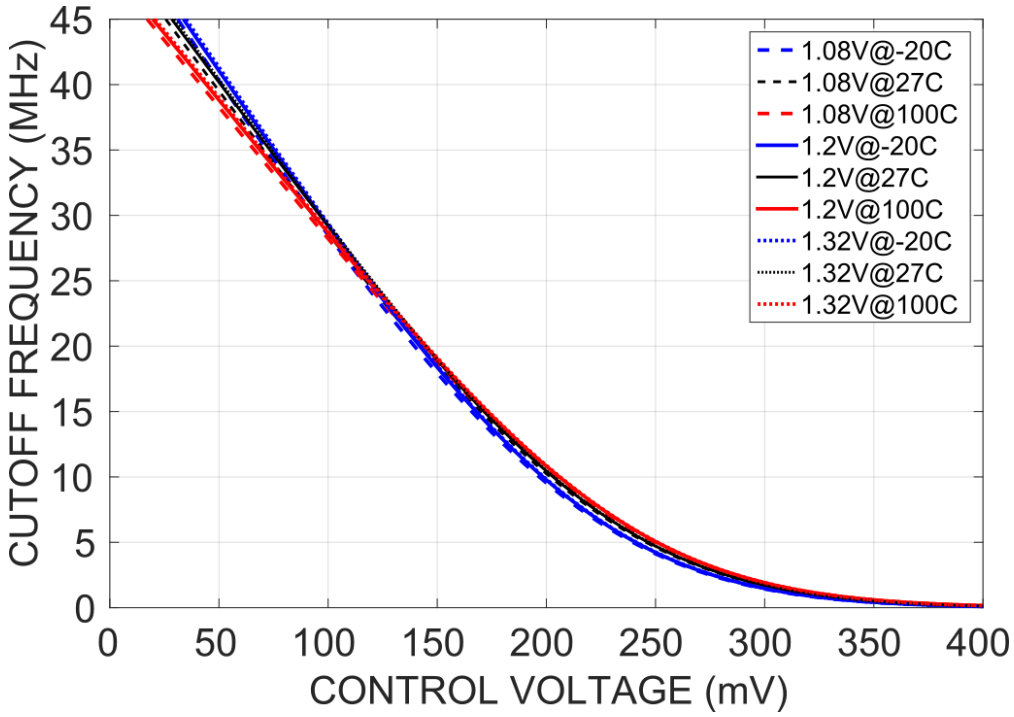

Figure 3.6 – Filter frequency response for different control voltages, for just VT.

3.2 Monte Carlo Analysis

The PVT analysis gives a general view of what may be the worst case for the design during Fabrication. However, these only show the extreme values for variations and may not cover different process variations that may compensate for one another. For this reason, the Monte Carlos analysis is an important tool to understand the statistical

distribution of results and variations your design may have.

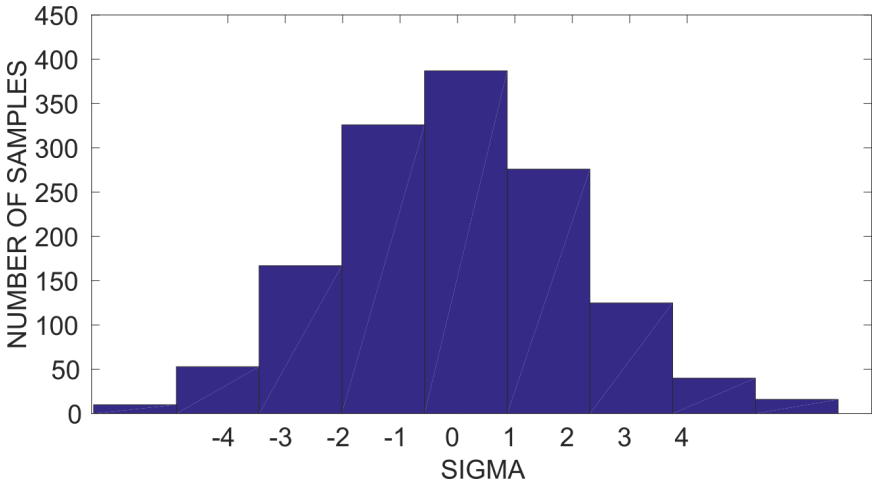

Figure 3.7 – Histogram for the F3dB with V_c at 0mV .

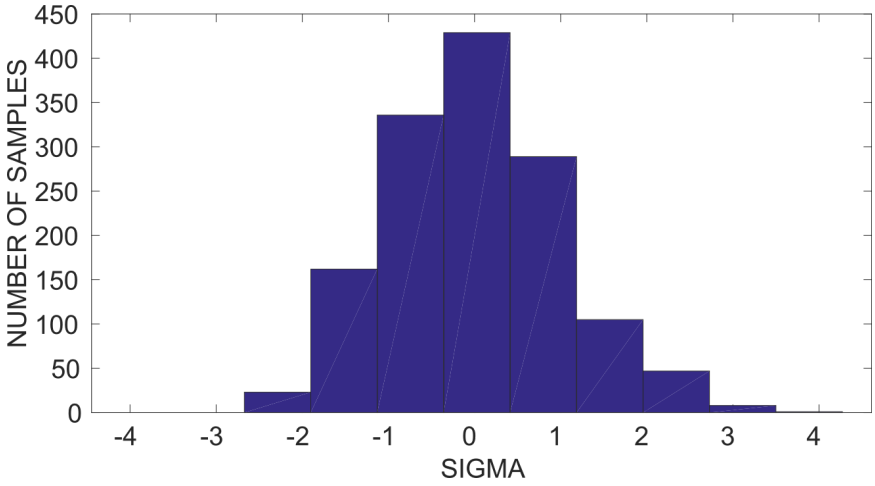

Figure 3.8 – Histogram for the F3dB with V_c at 195mV.

For the evaluation of the filter, the main curve is evaluated performing a sweep of the variable V_c. This is incompatible with the Monte Carlo Analysis, and therefore an alternative is needed. To solve this, we evaluate three points of the curve, save the worst-case MC state, and use it to run a sweep. This allows observing if the curves are very different for the multiple process variations and observe whether the conclusion for these points can be extended to other operations points. Figures 3.7 and 3.8 show the histogram for 2 different points of operation of the filter. Both analyses were run with 1400 samples, and both curves use $\sigma = 2.2MHz$ and a mean value of $f = 49.1MHz$ and $f = 9.8MHz$, respectively.

As it can be seen, the two histograms are different in distribution if we evaluate both curves for the same σ. This happens because the MOS transistor is less susceptible to the effects of process variations in the sub-threshold region than in the linear/triode region, and at $V_c = 195mV$ the PMOS is already near transit to sub-threshold region. In

fact, if we evaluate the number of samples that can achieve at least $f_c = 40MHz$ using $V_c = 0mV$, 98% of them are compliant with this criteria. Moreover, it's possible to extract the worst-case corners and run a sweep for the V_c curves. By doing so, we can evaluate how the desired reconfiguration capability varies in a worst-case scenario. Figures 3.9 and 3.10 show these curves.

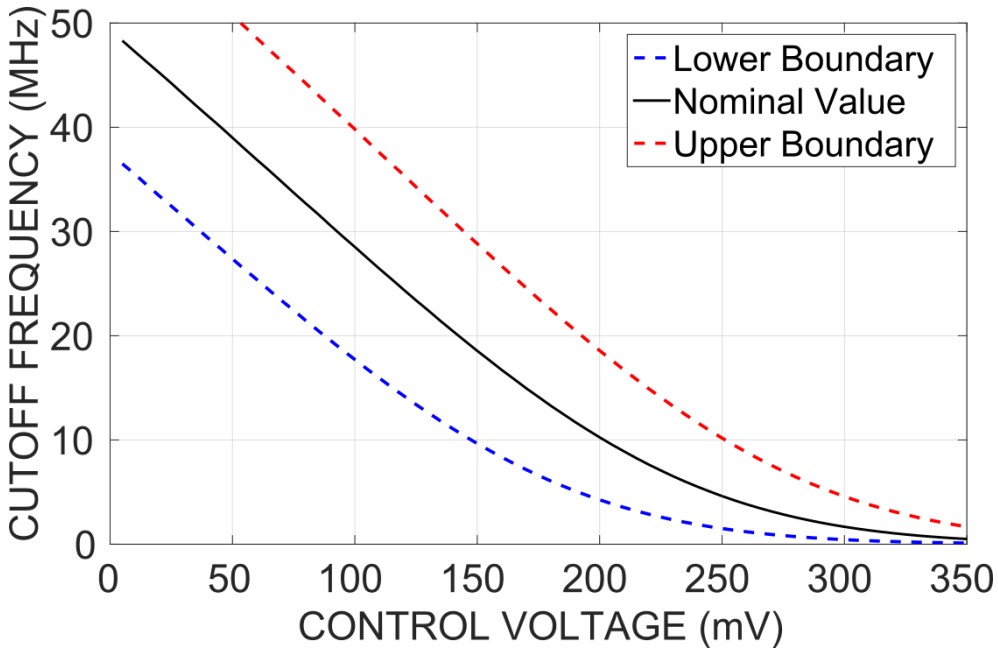

Figure 3.9 – Filter frequency response for different control voltages considering the variation related in Figure 3.7

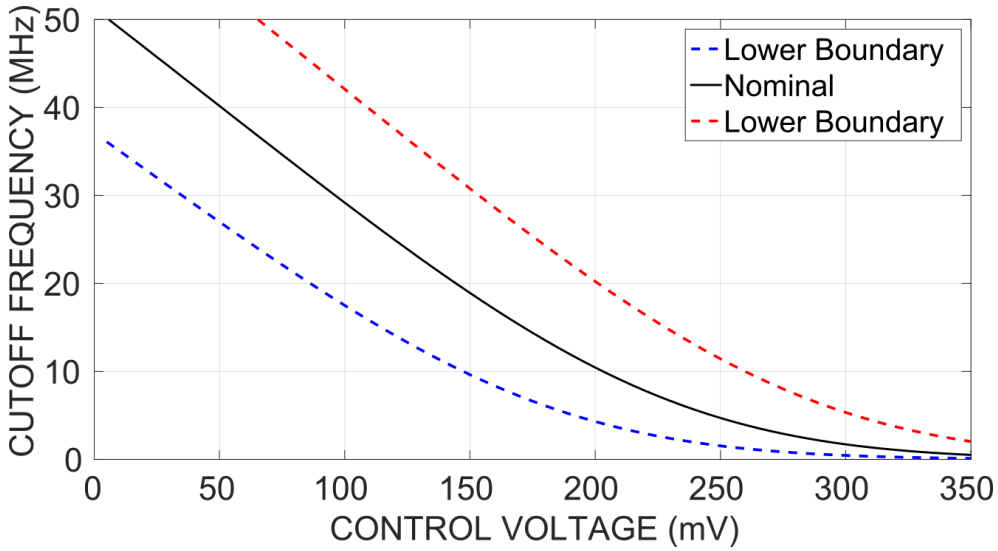

Figure 3.10 – Filter frequency response for different control voltages considering the variation related in Figure 3.8

Observing Figures 3.9 and 3.10, we see that both are very similar in both the angle for the linear portion, the point of inflection where the Transistor changes from the linear region, and the values of the maximum cutoff frequency achievable by the filter.

This means that, despite the apparent difference in operation points, an analysis made to one point in the circuit should behave in a similar way for another point. This is important as a way for us to avoid having to make statistical analysis for each possible value of V_c, allowing for the extrapolation of the results in a worst-case like that at $V_c = 0mV$.

3.3 Robustness Evaluation and Calibration

As it can be seen in some figures of this very chapter, most of the variations in the frequency response of the filter results in an "offset type" change in the desired frequency control curve. This means that the desired selectivity of 1MHz or less in each voltage step is maintained, and we only need to change the correspondence between the step value and the desired frequency.

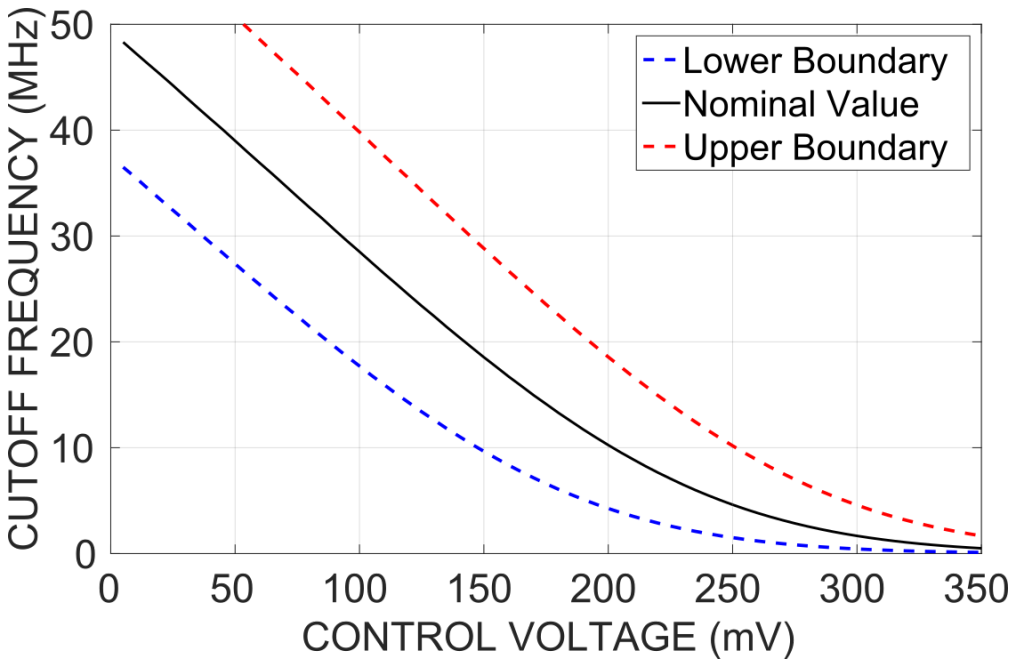

Figure 3.11 – Filter frequency response for different control voltages, analyzed in the variation points of the Monte Carlo analysis.

By choosing three values of voltage V_c, and evaluating the filter frequency cutoff, we can evaluate where the initial point of the curve begins and whether the curve steep is still the desired one. Then, we only need to offset the appropriate bit-combination in the default values, and the filter can have a correct table of correspondence for each of the desired 41 possible frequencies. This procedure has the advantage of saving on area, making the calibration process more direct, non-destructive, and easily automated.

Now for the remaining variations of Voltage and temperature, the results show that they have a small influence on changing this control curve behaviour and therefore, further valuations would be needed when the circuit is fabricated and multiple samples are tested. For now, the design is ready for moving on to the next phase: Physical Design and Parasitic Extraction Evaluation.

4 Physical Design and Parasitic Extracted Results

Assuming that the circuit is proper adjusted for robustness, the next step on the Analog Design Flow is to begin the Physical Design phase, also called the Layout Phase. In this stage, the models utilized in the schematics will be correlated to the 2D drawing provided by the Foundry for the appropriate process. These shapes and drawings are equivalent to multiple mask layers, that are later used by the Foundry during sequences of etching and deposition of materials [18].

It's during this phase that more effects are included in our analysis, especially with the effect of Parasitic resistors and capacitors; as well as the importance of transistor distribution along with the layout to avoid mismatching of components. Section 4.1 will discuss strategies from the literature and what was used in the proposed design. Section 4.2 will show the results after using the parasitic extraction tool, and compare these results with the previous ones. Section 4.3 shows the final results for this work in comparison to other filter designs in literature, contrasting parameters like power, area footprint, frequency range, and others.

Another important factor to consider is matching components. Devices in the CMOS process suffer from 2-D effects on both the lithography and deposition processes. This means it's best to use multiple unit-size devices than a larger, single one [6]. Most of the design is made with this in mind, having values of width in the transistors that are easily dividable by 2 or 4. In the same way, capacitors and resistors are arranged in arrays to try to balance these effects in the circuit.

4.1 Physical Design Strategy

Figure 4.1 shows the layout of a single biquad cell. The layout is divided into the amplifier and the feedback network, both made separated and integrated into a single cell biquad. The Feedback network has a horizontal symmetry, to avoid unbalancing between each of the differential sides. Both capacitors and transistors are interdigitated to improve mismatch robustness. The amplifier is separated according to the type of transistors: PMOS and NMOS are grouped and put in a cross-coupled configuration between themselves; the same is done for both resistors of the CMFB circuit, while the capacitors aren't matched because they are more tolerant to process variations. Finally, signal and power paths are made to minimize the length and to maintain a balance between the 2 differential signals, avoid coupling capacitance and minimize the increase in the capacitive load of the

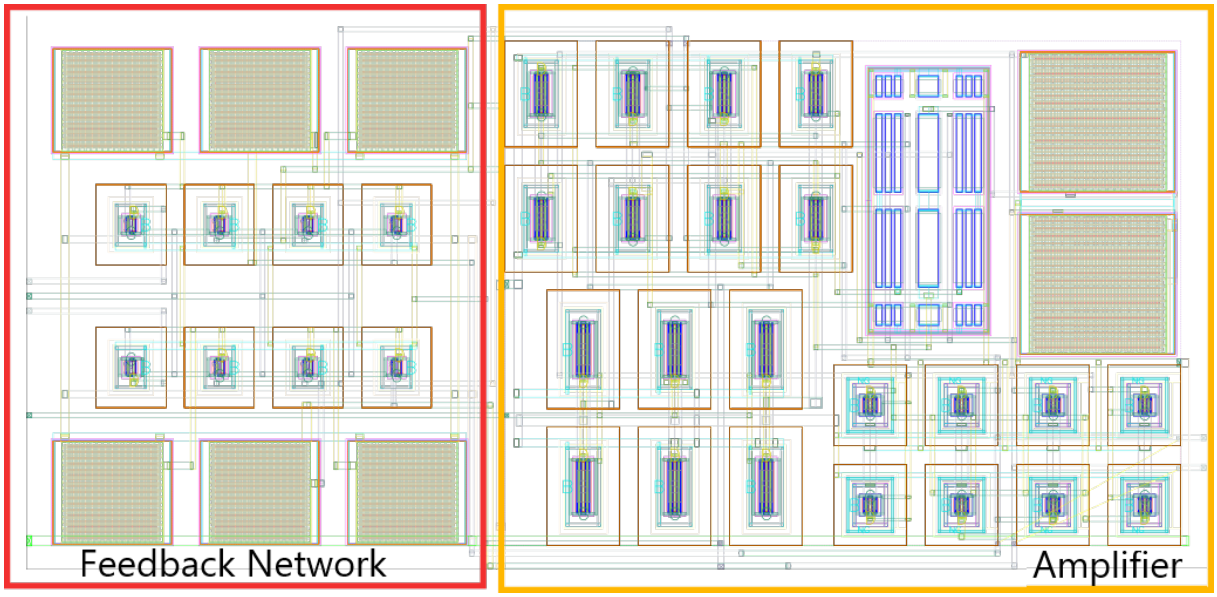

Figure 4.1 – Layout of the proposed biquad cell; measurement is in μm.

amplifier.

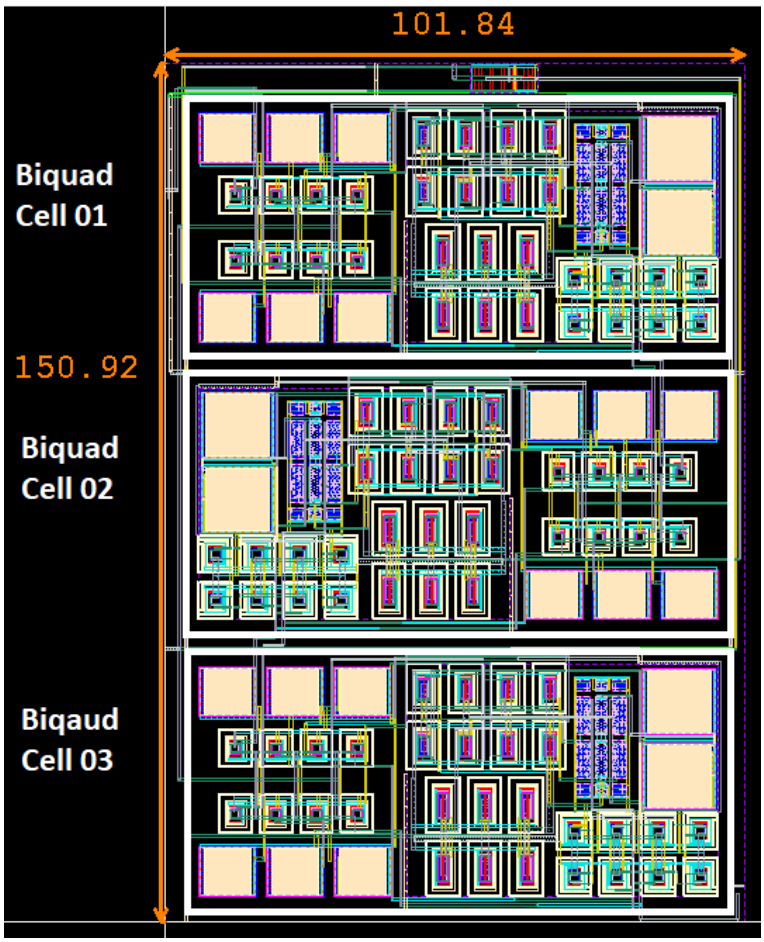

Figure 4.2 – First layout of the proposed filter, with all three cells and complete routing; measurement is in μm.

After the biquad is placed in a floor-plan and the paths are established, we

can construct between both parts. Here, form-factor and signal path length are the more important parts, and therefore the priority is to get the smaller signal path with the better form possible to the top. Since there is still no design for the top block, the parts are arranged as shown in Figure 4.2. The biquads are stacked, with the one in the middle mirrored to minimize the signal path. A single, small current distribution block is put in the top, generating a reference current I_{bias} for all the amplifiers. The signal enters in the top left, and exits at the bottom left. It's also important to notice the blocks are interdigitated between themselves, which should minimize mismatch.

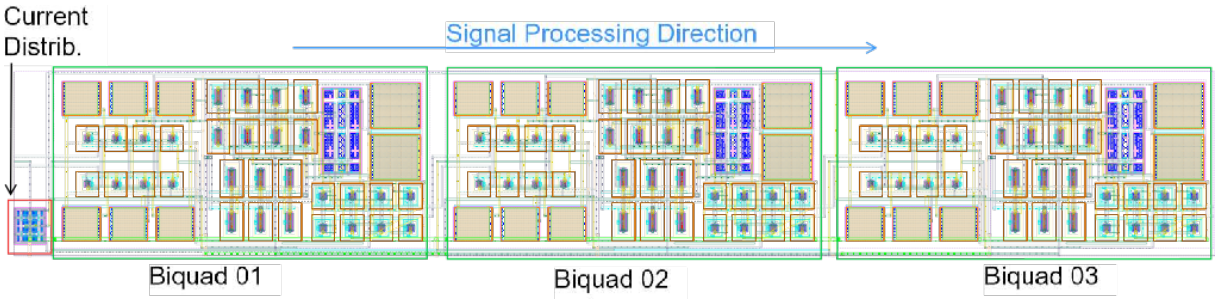

Figure 4.3 – Final layout of the proposed filter, with all three cells and complete routing; measurement is in μm.

Once that this layout was performed, some important block positions were altered in the top design, and therefore the filter layout has changed to better suit the new geometry. Figure 4.3 shows the final version of the filter. This layout is a single strip, which is not good for mismatch variations. It is, however, very central in the top configuration, so it should be less affected by mismatch when seen from the die perspective. Again a separate current distributor generates the reference currents for each amplifier. This design also has multiple lanes due to its long nature. The performance is similar to the other layout, and the area is even slightly smaller, passing from 0.015 mm^2 to 0.014 mm^2.

4.2 Parasitic extractions results and corrections

After each step of the layout is finished, the completed block is extracted using the Calibre PEX® tools in the Virtuoso® Layout Environment. After that, the same testbenches are used for evaluation, and the results are compared between the schematic model versus the extracted parasitic model.

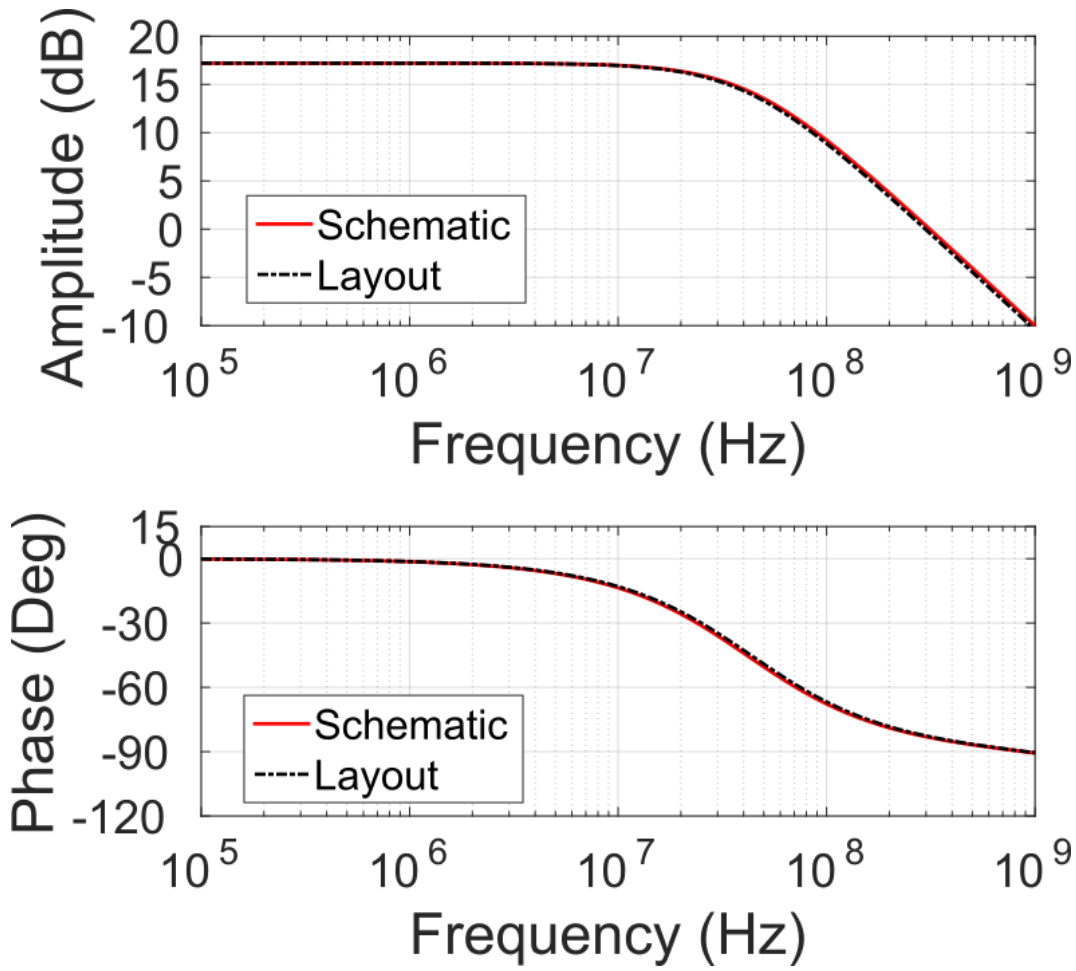

Figure 4.4 – Frequency response for the biquad amplifier, comparing schematic model versus parasitic extracted model.

Figure 4.4 shows the frequency response of the amplifier, comparing the post-layout version with the original schematics one. The main difference is the reduction of the DC Gain and the Phase margin. This happens because the parasitic capacitance and resistance on the branches change the output load of the amplifier, impacting its performance. We can see in the image that these values are very close, as the curves are identical.

Figure 4.5 shows the frequency response graph. Note that the difference is more significant in magnitude. Due to additional resistors and capacitors, the poles of the system are moved, and new zeros are created thanks to the capacitive coupling of the differential signals. Since they are very small, the effects can be seen above $200MHz$,

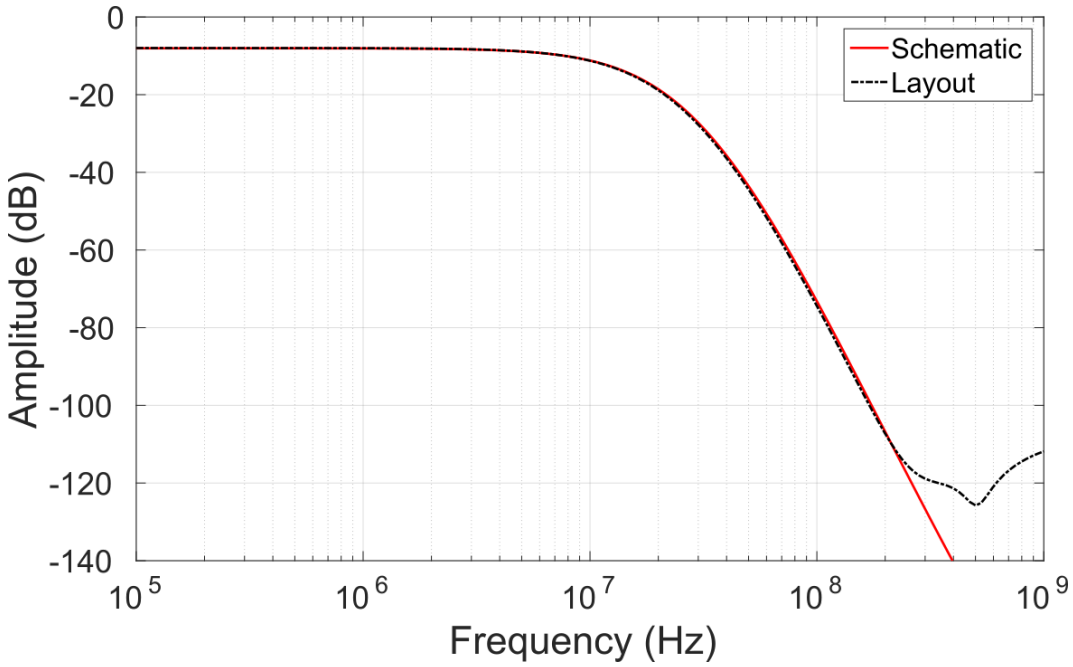

Figure 4.5 – Frequency response of the 6th order filter, comparing schematic model vs parasitic extracted model.

which is already on the desired stop band of the designed filter, and therefore is not a performance issue.

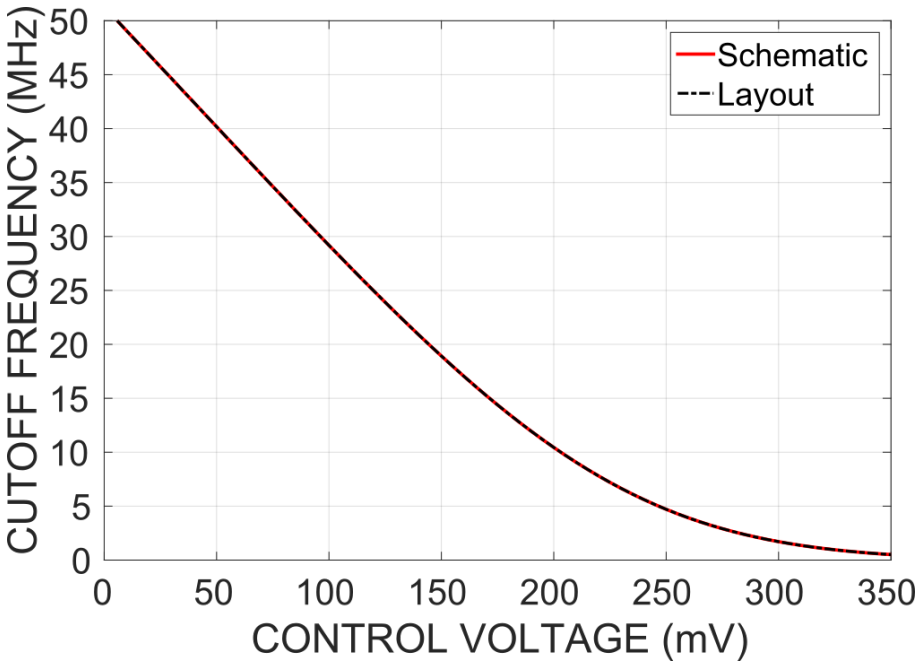

Figure 4.6 – Cutoff frequency versus control voltage curve of the filter, comparing schematic model versus parasitic extracted model.

Figure 4.6 shows the frequency behavior versus control voltage, the curve used in this work to evaluate the reconfigurability performance of this circuit. We can see that there is no significant difference between the two curves as expected, according to Figure 4.5. The position of the main poles, which are defined by the biquad feedback loop, doesn't

change with the parasitic resistors and capacitors. Therefore, as long as the poles made by these parasitic components aren't dominant, the layout won't affect this aspect of the circuit performance. This is important in IC design since a wider metal way has lower equivalent resistance, but higher capacitance. This trade-off, although not critical in our use case, can limit the performance of some filters.

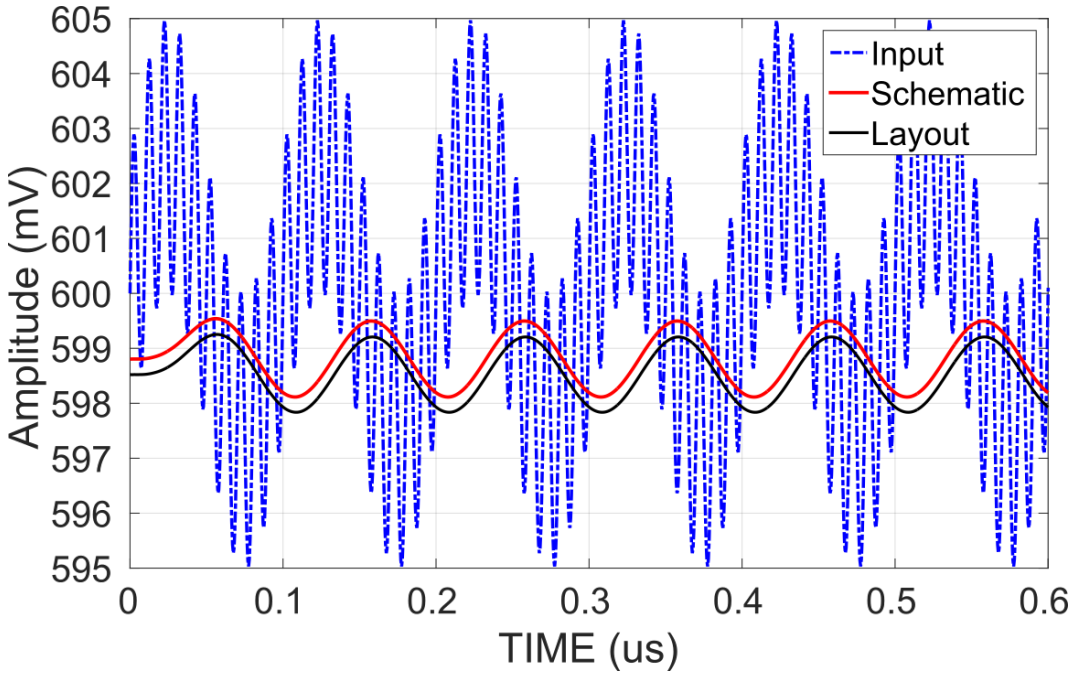

Figure 4.7 – Time domain response of the filter, comparing schematic model versus parasitic extracted model.

Finally, due to changes in loads, especially the resistive loads and the amplifier output capacitive load, there is a small deviation in the DC value of the output. As shown in Figure 4.7, this value is easily corrected by small adjustments in the transistors of the CMFB output circuit. This way, using a standard *tt* process at $27°C$ leads to a circuit with a DC level close to $600mV$.

4.3 Comparisons to previous works

Once that the final layout is established and the parasitic extraction included in the simulation, we consider the results of the simulations very close to the measured circuit. We compare our results to other works in the literature in Table 4.1. This allows the evaluation of how close our performance is to other multi-standard circuits already developed near our operation range.

Table 4.1 – Result comparison between Filters in Literature.

Ref.	**Tech**	**Filter Type**	**Order**	**VDD**	**Freq. Range**	**Power**	**Area**
Unit	-	-	ABS	V	MHz	mW	(mm^2)
This Work	65nm	MOSFET -C	6	1.2	1-40	1.1	0.014
[19]	130nm	g_m-RC	4	1.2	1.45-3.6 / 5.87-19.44	3.4 / 14.2	0.9
[12]	65nm	RC	2 - 8	1.2	0.5-22	1.72-9.6	0.8
[11]	180nm	g_m-C	2	1.8	0.2-20	0.95-3.81	0.013
[13]	180nm	RC	6	1.8	7.1-20.3	0.47	0.21
[20]	180nm	g_m-C	6	1.8	1.5-12	10/15	0.83
[21]	250nm*	g_m-C	3	2.5	0.05-2.2	2.5-7.3	0.48

*this technology is SiGe instead of CMOS.

Comparing this work with the others in Table 4.1, the results in area reduction are very promising. Only one work is around the same footprint, but its frequency range is more limited, its power consumption higher and it's of a lower order, although it's in a larger node. When compared with other works, we see the frequency range is considerably higher, with one of the smallest power consumption and with higher order than average, which indicates a higher selectivity. Since most of these works don't specify the frequency steps and the possible number of configurations, it's difficult to make a fair comparison.

Note that, except for one work ([11]), all other works in Table 4.1 are measured results, and ours is simulated. As it is well known final measured results can be very different from simulated ones.

5 Conclusions

As stated, the challenge of building flexible analog blocks for front-end radios becomes especially important in satellite communications, as there are fewer restrictions in the channel bandwidth for these types of systems. However, the more common approach of switching between components has the compromise of adding a lot of components, which translates to an increase in the area needed for an Integrated Circuit implementation. The approach of using a polarized transistor in the wide-band frequency area allows for a more flexible design that can also be calibrated without the need for any additional structures, further saving the area for the circuit.

Looking at the results for the proposed circuits, they are generally on par with other published works. Power consumption is better compared to other filters, especially when observed at the higher operating frequencies. It also has the smallest footprint compared to other works, except for one that uses a single biquad [11], while this work has 3. This means that we get triple the selectivity in the desired pass-band for almost the same area. Also, the small area combined with the flexibility for many different configurations gives it the capability to be used for multiple radio applications. The main difference to these woks is the lack of a measure after fabrication, which should be addressed in the future.

Table 5.1 – Compatible Standards for the proposed circuit.

Standard Name	**Freq. Range**	**Modulation Schemes**
DVB-S2[1]	1-20 MHz	BPSK, QPSK, 8-PSK, 16-QAM or 64-QAM.
802.11n[3]	20/40 MHz	OFDM, BPSK, QPSK, 16-QAM or 64-QAM.
DVB-H[2]	5-8 MHz	OFDM, BPSK, QPSK, 8-PSK.
LTE [22]	1.4-20 MHz	OFDM, QPSK, 16-QAM, 64-QAM, 256-QAM.

Table 5.1 shows some wide-band standards which have frequency and noise inside our evaluated circuit. This indicates that, if used in an according to front-end receiver chain, the circuit presented in this work can perform well for these applications, as long as it is properly calibrated and the proper reference values are established for the control voltage V_c.

Therefore, the proposed solution of exchanging multiple devices for a polarized transistor allowed for a small, fully integrated analog filter that gives the versatility of use to the front-end analog radio. The circuit could even be used in other wide-band applications as long as they are on their frequency range and minimum bandwidth.

The next steps for this work include the measured results from a fabricated

chip to validate the results. This is expected to happen in near future, together with other circuits in the project by Eldorado Research Institute. Full integration with other analog blocks and a digital modem for functional analysis is also planned, and it was already done at a schematic level. The baseband circuitry is already in layout, with the filter as shown in Figure 4.3. It's possible a version of the previous layout, shown in Figure 4.2, will also be fabricated in a test mode. This provides an opportunity to evaluate the impact of different layout strategies on the proposed circuit. Finally, since the filter and baseband circuitry can be independently evaluated, it's possible to test a fabricated version with real-world signals from different standards, like the ones from Table 5.1; as to evaluate the direct performance of this circuit in a real-world multi-standard scenario.

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Annex

ANNEX A – Publication ICECS 2019

The Paper *A Small-Reconfigurable Low-Pass Filter for Analog Front-End Receivers* was presented in the International Conference on Electronics Circuits and System at Genova, Italy, from the 27th to the 29th of November of 2019. This publication is available at IEEEXplore.

A Small-Reconfigurable Low-Pass Filter for Analog Front-End Receivers

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***Abstract*—Some applications in communications have multiple bandwidths, requiring circuits with more flexibility in the radio receiver. This work proposes a reconfigurable, fully integrated Sixth Order Butterworth filter for these front-end receivers. To achieve this, the circuit uses a transistor-based structure to act as a voltage-controlled resistor. The resulting circuit is simulated using a 65nm CMOS technology. It attains a footprint of $0.015mm^2$ and a frequency step of 1 MHz in filter selectivity. The designed filter is compared to State-of-the-Art works, proving it can be used in multiple applications and configurations from 40 MHz down to 1 MHz channel bandwidth.**

I. Introduction

In the context of terrestrial wireless communication, usually, each protocol establishes a standard with a fixed bandwidth. In contrast, for satellite communication, each one can work on different channel bandwidth, as these systems are more limited by other variables, like transmission power. This characteristic poses a challenge to receiver design, as they need a higher degree of flexibility for signal reception. It is especially difficult for analog radios, as they are more sensitive to variations, like those in process and temperature. Some solutions have been proposed for building flexible analog blocks, for example in Software Defined Radio (SDR) [1]. Most of them rely on using multiple components for each desired frequency response. However, they have an issue: when the number of different configurations increases, the number of components also increases. This impacts the footprint of the block, which is more critical for Integrated Circuits, as each chip is desired to have a smaller silicon area.

An alternative to achieve this flexibility without the area penalty is the use of MOS transistors in the triode region. This device has a linear response to different voltages applied in the gate, acting as a voltage-controlled resistor. This allows for a single device to work as multiple resistors, as long as you have controlled voltage in it.

This work proposes a circuit using a polarized PMOS transistor as a resistor, in what is known as an Active MOSFET-C or Active Pseudo-RC filter. This type of circuit has already been used in other applications, such as in biomedical electronics [2]. However, these applications use a different frequency range, while these works focus on wideband applications such as satellite communications. The chosen design allows for a tuner compatible with many possible bandwidths, and possibly other communication standards.

II. Filter Design

The traditional approach for filter design is the cascade of multiple identical cells in accordance with the desired order. Following this approach, a Rauch biquadratic cell is chosen as the unit cell for the filter design. This topology combines a passive filter cell with an active one, giving 2 poles (40dB/dec attenuation) with a single amplifier. This is ideal for both area and power consumption optimization. The Laplace low pass transfer function using the Rauch topology [3], can be written as

$$H(s) = \frac{1 - AR_{eq} - s(R_{eq}C)}{(1 + sR_{eq}C)^2}, \tag{1}$$

where R_{eq} is the equivalent resistance of the resistor in the circuit and C is the equivalent capacitance, and A is the DC gain of the amplifier. With the filter topology selected, the resistors are substituted by transistors. Using the equivalent model it's possible to directly correlate the system transfer function given in (1) with the transconductance and the gate control voltage (V_c) of the transistor as

$$R_{eq} = \frac{V_{SD}}{I_d} = \frac{1}{\beta \cdot (V_c - V_t)}, \tag{2}$$

where I_d is the current in the drain of the transistor, V_{SD} is the voltage between the source and drain of the transistor, β is a constant, V_t is the threshold voltage of the transistor, and V_c is the gate control voltage. If

V_c is used to control the gate, we can make $V_c = V_{SG}$ for the signal without the common-mode voltage. Also, analyzing both Equations 1 and 2, the poles of the first are correlated to V_c by using the second equation. This way, we can change the frequency behavior of the filter by use of this voltage.

Therefore, if we establish our desired frequency range and step, we know the necessary voltage range and step for V_c. For the purposes of this work, we use a range from 1MHz to 40MHz and step of 1MHz; with an equivalent range from 45mV to 320mV and step of 5mV.

Figure 1 is the final circuit design for the low-pass Rauch biquadratic cell used in the filter. The ratio between capacitors and transistors are shown in Equation (3), calculated to achieve maximum flat pass-band characteristics (Butterworth criteria). W_M and L_M are, respectively, the transistor width and length for each transistor in Figure 1 and C is the capacitance for the capacitors in the same figure. The complete filter is composed of 3 biquad cells cascaded, thus presenting a 6th Order behavior. The design is validated using the DVB-S2 standard for satellite communication, in the receiver end.

$$\begin{aligned} C_1 &= 2 \cdot C_2 \\ \frac{W_{M2}}{L_{M2}} = 2 \cdot \frac{W_{M1}}{L_{M1}} &= 2 \cdot \frac{W_{M3}}{L_{M3}} \end{aligned} \tag{3}$$

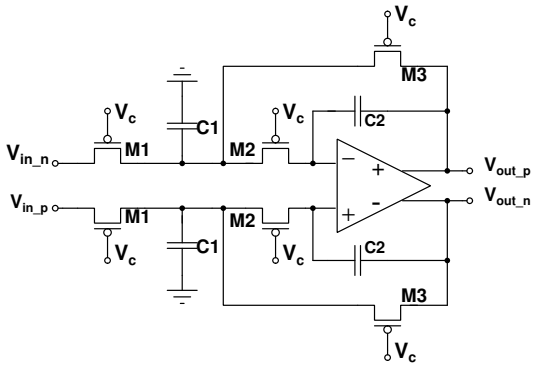

Fig. 1. Schematic of the implemented solution using a 2nd Order block (Biquad cell).

The Amplifier utilized in each biquad cell is shown in Figure 2. The chosen circuit has a single stage that helps to reduce the area. Finally, the layout of the complete filter can be seen in Figure 3, and its dimensions in Table I.

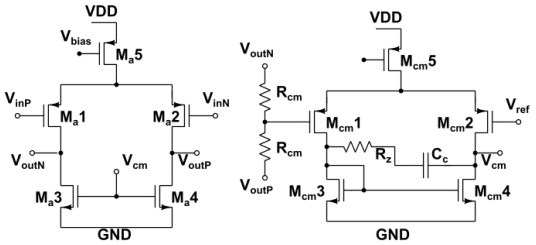

Fig. 2. Schematic of the amplifier utilized in the biquad cell

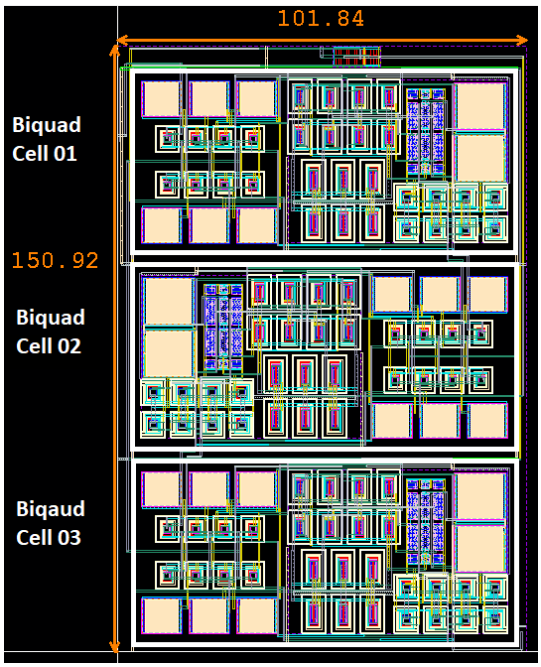

Fig. 3. Layout of the proposed filter, with all three cells and complete routing; measurement is in μm.

TABLE I
DIMENSIONS AND VALUES FOR THE PROPOSED CIRCUIT

Device	Dimension
$M1$, $M3$	0.95/0.2 μm
$M2$	1.9/0.2 μm
M_a1, M_a2	12/0.1 μm
M_a3, M_a4	4/0.1 μm
$M_{cm}1$, $M_{cm}2$	12/0.1 μm
$M_{cm}3$, $M_{cm}4$	4/0.1 μm
R_{cm}	50 $k\Omega$
R_z	1.2 $k\Omega$
C_c	300 fF
C_1	120 fF
C_2	240 fF

III. RESULTS

The results presented in this work are for post-layout simulation using a 65nm Low-Power CMOS

TABLE II
RESULT COMPARISON BETWEEN FILTERS

Reference	**[4]** (measured)	**[5]** (measured)	**[6]** (simulated)	**[7]** (measured)	**This Work** (simulated)
Tech	130nm	65nm	180nm	180nm	65nm
Filter Type	Active-g_m-RC	Active-RC	Active-g_m-C	Active-RC	Active MOSFET-C
VDD(V)	1.2	1.2	1.8	1.8	1.2
Order	4	2/4/6/8	2	6	6
Freq. Range(MHz)	1.45-3.6 / 5.87-19.44	0.5-22	0.2-20	7.1-20.3	1-40
Power(mW)	3.4 / 14.2	1.72-9.6	0.95-3.81	0.47	1.07
Area (mm^2)	0.9	0.8	0.013	0.21	0.015
IP3(dBm)	21	17.8	28.97	13.6	25
Input Ref. Noise	36 μV_{RMS}	87.2 $nA/sqrt(Hz)$	2.5 $pA/sqrt(Hz)$	66.2 $nV/sqrt(Hz)$	140 $nV/sqrt(Hz)$

technology, using Cadence® Virtuoso® Analog Design Environment and Schematics Editor. They include the parasitic extraction for the simulation, done after the physical design phase, for all 3 biquads.

Figure 4 shows the frequency response curve, set for five possible configurations. The cutoff frequency shown on each curve ranges from 1MHz to 40MHz. Numbers of compiled results can be seen in Table II, compared to other published works. The results for area and power are good, especially when compared with filters with a similar order, as filter design usually scales in both footprint and consumption the higher the order.

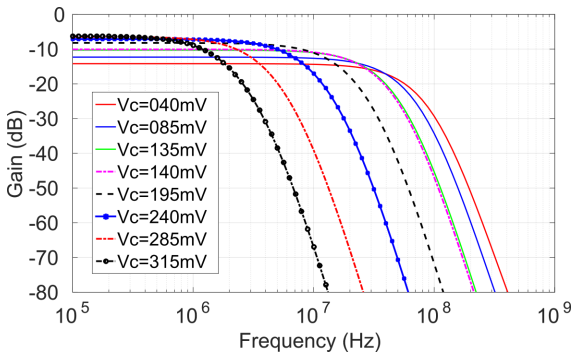

Fig. 4. Filter response for different control voltages, going from the range from 1MHz to 40MHz cutoff frequency.

Robustness for the CMOS process is also analyzed, and Figure 5 shows the results for a Monte Carlo analysis of the circuit behavior. The curves represent the cutoff frequency (f_c) of the filter according to the control voltage in the gate of the PMOS transistor, composed by the nominal value and a 3σ variation. The $+3\sigma$ is represented for the "Upper Boundary" and the -3σ is represented for the "Lower Boundary". Each curve has a similar slope, being only a shifted version of the average curve. This means the design can be calibrated accordingly without the need for additional structures, just by adjusting the control voltage (V_c) range instead.

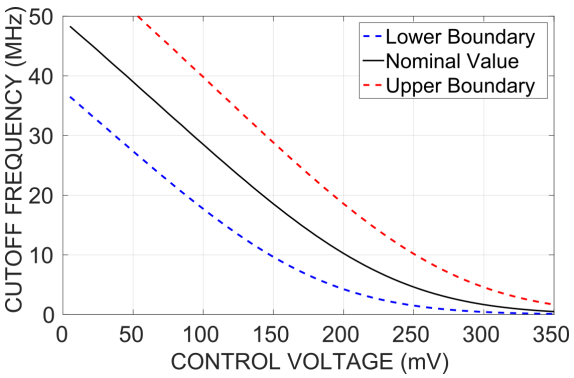

Fig. 5. Filter frequency response for different control voltages, analyzed in the variation points of the Monte Carlo analysis.

In the nominal curve of Figure 5, when looking from about 45MHz to 10MHz, the behavior is directly linear with 1MHz variation in the cutoff frequency of the filter for every 5mV. This allows us to establish a correlation for every bandwidth distant at least by 1MHz to the other, and the filter will have the desired selectivity, as it was originally intended. As the transistor changes from the linear region, the slope decreases, but that is not a problem as it means the selectivity is tighter than intended, just needing an extension in the voltage range.

IV. CONCLUSION

As stated, the challenge of building flexible analog blocks for front-end radios becomes especially important in satellite communications, as there are fewer restrictions in the channel bandwidth for these types of systems. However, the more common approach of switching between components has the compromise of adding a lot of components, which translates to an

increase in the area needed for an Integrated Circuit implementation. The approach of using a polarized transistor in the wide-band frequency area allows for a more flexible design that can also be calibrated without the need for any additional structures, further saving area for the circuit.

Looking at the results for the proposed circuits, they are generally on par with other published works. Power consumption is better compared to other filters, especially when observed at the higher operating frequencies. It also has the smallest footprint compared to other works, with the exception of one that uses a single biquad [6], while this work has 3. This small area combined with the flexibility for many different configurations gives it the capability to be used for multiple radio applications.

Therefore, the solution of exchanging multiple devices for a polarized transistor allows for a small, fully integrated analog filter that gives versatility of use to the front-end radio. The circuit could even be used in other wide-band applications as long as they are on its frequency range and minimum bandwidth.

Next steps include the measure results from a fabricated chip to validate the results. Full integration with other analog blocks and a digital modem for functional analysis is also planned.

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