A Patterning-Based Strain Engineering for Sub-22 nm Node FinFETs

Matthias Schmidt, Martin J. Süess, Angelica D. Barros, Richard Geiger, Hans Sigg, Ralph Spolenak, and Renato A. Minamisawa

***Abstract*— We propose a strain engineering approach that is based on the patterning and under etching of fins using strained Si grown on SiGe strain relaxed buffers. The method enhances the strain of the patterned Fins up to ∼2.9 GPa without the need of epitaxial source and drain stressors. We report a systematic simulation study on the scaling of this method for the present and future technology nodes down to 7 nm. Finally, we estimate that the technique deliveries an electron mobility enhancement up to 87% for FinFETs, independent of the technology node.**

***Index Terms*— Strained Si, FinFet, strain-relaxed-buffer, scaling, simulations.**

I. Introduction

STRAIN engineering is a crucial technology to provide enhancement of carrier velocity in scaled Si transistors through specific manipulations of their bandstructure [1], [2]. The state-of-the-art strain techniques are mostly based on the deposition of contact etch-stop layers (CESL), by depositing source and drain (S/D) from a lattice mismatched semiconductor (e.g., SiGe, Si:C), or at the *wafer level*, by growing strained Si on a strain-relaxed-buffer (SRB) [3]–[6]. Xu *et al.* have shown that S/D stressors deliver more strain in a Fin than CESL, though in both cases, the maximum achieved stress amounts less than 0.5 GPa [7]. In turn, Eneman *et al.* reported that strained Si grown on SRB ($Si_{0.75}Ge_{0.25}$) is the most effective technique to induce tensile stress in Fins for the 14 nm and smaller nodes, although epitaxial Si:C S/D stressors are required to achieve such high stress levels (>2 GPa) [8], [9]. However, because of the constrained geometry, such methods become difficult to implement and often ineffective for the presently employed Fin architecture featuring 22 nm and smaller gate lengths (L_g) [6]–[9].

Si nanowires with uniform stress distribution up to 2 GPa have been demonstrated using highly strained Si on insulator (H-SSOI) [10]. Unfortunately, these substrates have unacceptable defect density associated with the high Ge content (35%) SRB wafer utilized for fabrication.

In this letter, we discuss a new strain engineering method that mechanically increases the stress of Si Fins grown on SiGe SRB with low Ge content (25%) *without external S/D stressors*. This concept has been experimentally demonstrated in ∼600 nm long top-down fabricated Si nanowires on insulator with extended contact pads, delivering up to 7.6 GPa stress [11]. The process is based on pure elastic deformation, is compatible to different materials and length scales [12] and enables precise control over the induced strain. Here, we report a comprehensive simulation study on the effectiveness of this technology into scaled FinFETs down to sub-10 nm L_g.

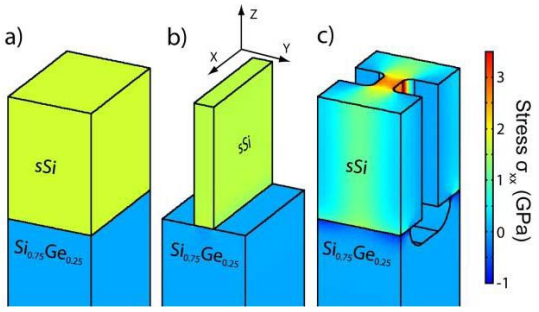

Fig. 1. Longitudinal stress (σ_{xx}) simulation of (a) starting 30 nm thick strained Si grown on $Si_{0.75}Ge_{0.25}$ SRB, (b) after conventional pattern of Fin structure and (c) after patterning and under etching of the Fins and contact pads. The full layer is in biaxial stress while the released Fin structure is under uniaxial stress.

II. Strain Engineering

All stress simulations are performed for Fins oriented to <110> on 30 nm thick strained Si/$Si_{0.75}Ge_{0.25}$ SRB (100) wafer using a finite element method (FEM) simulation software (COMSOL). The stress in the starting Si layer is given by the lattice mismatch between SRB and the Si layer and amounts ∼1.7 GPa biaxial stress [Fig. 1(a)]. The longitudinal stress in a conventional Fin fabricated by patterning the biaxially strained Si layer relaxes to 1.6 GPa due to the creation of free surfaces in the transverse direction [Fig. 1(b)].

Here, we extend the aforementioned method by simply patterning the Fins with contact pads followed by selectively etching the SiGe underneath. The under etching extends under the contact pads to a controlled length *UE*. The released Fins

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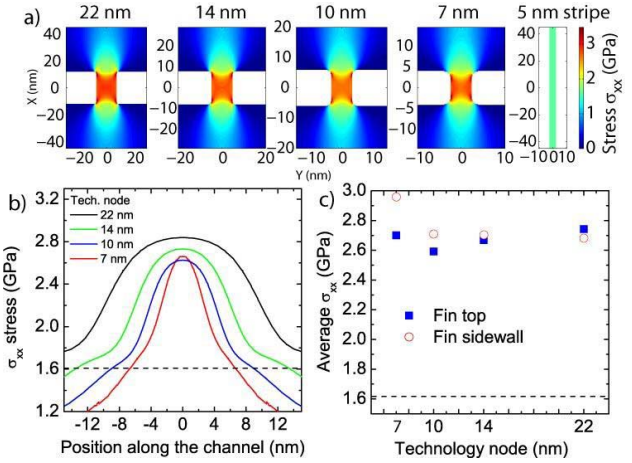

Fig. 2. (a) xy-slices of longitudinal stress σ_{xx} from the 3D simulations for Fins with dimensions summarized in Table I. The top indices indicate the technology node. A 5 nm narrow strained Si/SBR patterned stripe (right). (b) Stress profiles (σ_{xx}) along the Fins for the different technology nodes, and (c) the averaged σ_{xx} at the top and sidewalls of the Fins *vs.* the node. The σ_{xx} profile and average stress of the patterned stripe are plotted for comparison (dashed line) in (b) and (c).

and under etched contact pads are then approximately under *uniaxial stress*. As the layer thicknesses and the force in the structure remain constant, the stress is inversely proportional to the cross-sectional area, such that it accumulates at the Fin and relaxes at the pads [Fig. 1(c)]. The stress in the constriction can, therefore, be finely tuned by varying the dimensions of the Fins, pads and *UE*. Table I list the mesa dimensions simulated in this letter for the 22, 14, 10 and 7 nm technology nodes. The values are consistent with those given in Ref. [6], [9].

III. Results and Discussion

Fig. 2(a) depicts a *xy*-slice of the longitudinal stress σ_{xx} from the 3D simulations for Fins with dimensions listed in Table I. The σ_{yy} and σ_{zz} components in the center of the fin are below 100 MPa. The technique is effective for all investigated technology nodes since it only depends on the relative dimensions of the Fin, pads and *UE*, and provides up to ~3 GPa. A 5 nm narrow strained Si/SBR patterned stripe (right) is plotted for comparison. Whereas, the longitudinal stress on the top of the 5 nm narrow patterned stripe remains constant and equal to ~1.6 GPa, the 5 nm narrow constriction (7 nm node) displays an enhanced stress up to ~2.8 GPa in the central part and up to ~3.5 GPa in the corners of the Fin.

Fig. 2(b) shows the longitudinal stress profile at the surface of the Fin for the different nodes. The profile of the 5 nm narrow stripe is plotted for comparison. The variation between the maximum and minimum stresses within the Fin length amounts up to ~40% for the 22 nm node and decreases down to ~32% for the 10 and 7 nm nodes. Fig. 2(c) displays the average channel surface stress $\sigma_{xx}^{\text{sur}} \frac{1}{L_g A_v} \int_{A_v} \int_{L_g} \sigma_{xx}\, dxdv$ for the top ($v = y$, $A_y = W_{\text{Fin}}$ = Fin width) and sidewalls ($v = z$, $A_z = H_{\text{Fin}}$ = Fin height) [9]. The surface stress ranges from ~2.6 to ~3.0 GPa for the different nodes.

Scaled devices operate at quasi-ballistic regime, where only low field mobility has physical meaning [2]. Under such field conditions multigate FinFETs can experience volume

TABLE I
Dimensions for Different Technology Nodes

Dimension *vs.* Node	22	14	10	7
Fin width (W_{Fin})	15	10	7	5
Fin pitch	60	42	30	21
Fin height (H_{Fin})	30	30	30	30
Fin length (L_g)	24	16	12	8
Gate pitch	90	58	40	29
UE	22	14	10	6

Units: nm

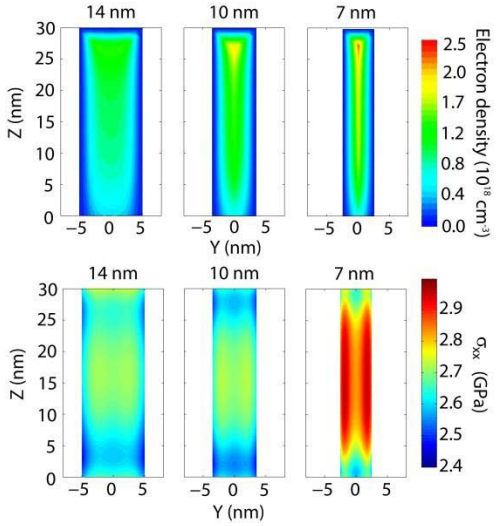

Fig. 3. (Top row) Cross sectional 2D simulations of charge density in trigate FinFETs using the 14, 10 and 7 nm nodes dimensions from Table I at gate voltage $V_G = V_T$. (bottom row) 2D longitudinal stress σ_{xx} simulations for Fins with the dimensions of the 14, 10 and 7 nm nodes.

inversion, provided that the width is sufficiently narrow [13]. Fig. 3(top row) depicts the cross sectional charge density for trigate FinFETs using the 14, 10 and 7 nm nodes dimensions at $V_G = V_T$. The volume inversion is weakly influenced by the uniaxial strain, which shifts the threshold voltage V_T by less than −35 mV [15].

High electron concentration in the center of the Fin begins to appear at the 10 nm width (14 nm node) and becomes stronger at 5 nm (7 nm node), as an indication of volume inversion. As a consequence, inversion carrier mobility is increased due to reduced surface scattering. Whereas most of works so far have analyzed surface stress in FinFETs, here we compare it to the volume stress in order to assess its impact on the transport enhancement.

Fig. 3(bottom row) displays *yz*-slices through the longitudinal stress σ_{xx} for Fins with the 14, 10 and 7 nm technology nodes dimensions. The average bulk stress $\sigma_{xx}^{\text{sur}} \frac{1}{L_g F_{\text{Fin}} W_{\text{Fin}}} \int_{L_g} \int_{F_{\text{Fin}}} \int_{W_{\text{Fin}}} \sigma_{xx} dxdydz$ for such nodes amounts ~2.5, 2.75 and 2.9 GPa. The stress is higher for the 7 nm nodes due to the comparable dimension of the Fin length L_g to the radius of the pad corners, which are points of stress concentration. Therefore, the smaller technology node exhibits simultaneously higher volume inversion and stress. Notice that these stress values are similar to those observed in the Fin surfaces as seen in Fig. 2(c).

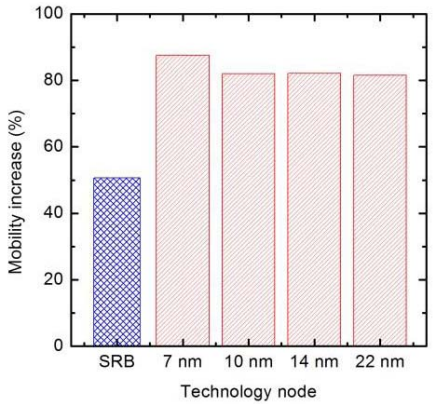

Fig. 4. Estimation of mobility increase in a n-type FinFET for different technology nodes using the patterning based strain technology (red). The mobility increase induced by SRB technology only is plotted for comparison.

We now estimate the potential enhancement in low field mobility induced by our strain engineering technique using piezoconductance theory [9]. The mobility variation is given by the product of the piezoconductance tensor and the average volume stress $\partial\mu^{\mathrm{vol}} = \Pi \cdot \sigma_{xx}^{\mathrm{vol}}$. Here, we assume bulk values for the piezoconductance tensor [8], [9], [14]. The absolute mobility of the strained Fin is then obtained from that of relaxed Si according to $\mu_{\mathrm{str}} = \mu_{\mathrm{rel}}(1 + \partial\mu^{\mathrm{vol}})$. The mobility enhancement is finally given by $\Delta\mu = \mu^{\mathrm{str}} - \mu^{\mathrm{rel}}/\mu^{\mathrm{rel}}$. Fig. 4 displays the mobility enhancement for the different technology nodes. The mobility increase induced by SRB (25% Ge content) technology is plotted for comparison.

Whereas the SBR induces 50% enhancement in electron mobility, further increase up to 87% can be reached using the patterning based strain engineering technique.

Regarding processing possibilities, high resolution lithography techniques would need to be further developed to provide the direct patterning of the nanostructures proposed here. A potential solution could be double exposure using EUV interference lithography [16]. Another possibility could be to pattern first the Fins by standard pitch doubling techniques followed by overgrowth of the Si pads prior to under-etching. This would inevitably increase the pad cross section, which further increases the stress multiplication effect described in this letter.

IV. Conclusion

A patterning based strain engineering method has been proposed as an alternative for sub-22 nm technology nodes. The technique is based on the patterning of constricted structures from pre-strained layers and is effective for all technology nodes down to the 7 nm. The stress is enhanced in both, surfaces and volume of the Fin structures. We demonstrate up to ~2.9 GPa average stress for the 7 nm technology node by patterning the constricted strained Si FinFETs grown on SRB with 25% Ge, without using any complementary strain engineering method. We estimate that this level of stress results in an increase of about 87% in electron mobility. Regarding the fabrication of a CMOS inverter, although the technique described here aims to increase electron mobility, the SBR could be used for the fabrication of the p-MOSFET since it exhibits enhanced holy mobility [17].

References

[1] C. W. Leitz, M. T. Currie, M. L. Lee, *et al.*, "Hole enhancement in strained $Si/Si_{1-y}Ge_y$ p-type metal-oxide-semiconductor field effect transistor grown on relaxed $Si_{1-x}Ge_x$ (x<y) virtual substrates," *Appl. Phys. Lett.*, vol. 79, no. 25, pp. 4246–4248, Dec. 2001.

[2] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," in *Proc. IEEE IEDM*, Dec. 2006, pp. 1–4.

[3] M. Chu, Y. Sun, U. Aghoram, *et al.*, "Strain: A solution for higher carrier mobility in scaled MOSFETs," *Annu. Rev. Mater. Res.*, vol. 39, pp. 203–229, Aug. 2009.

[4] D. J. Paul, "Si/SiGe heterostructures: From material and physics to devices and circuits," *Semicond. Sci. Technol.*, vol. 19, no. 10, pp. R75–R108, 2004.

[5] M. T. Currie, S. B. Samavedam, T. A. Langdo, *et al.*, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett.*, vol. 72, no. 14, pp. 1718–1720, 1998.

[6] C. Auth, C. Allen, A. Blattner, *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol. Circuits*, Jun. 2012, pp. 131–132.

[7] N. Xu, B. Ho, M. Choi, *et al.*, "Effectiveness of stressors in aggressively scaled FinFETs," *IEEE Trans. Electron Device*, vol. 59, no. 6, pp. 1592–1598, Jun. 2012.

[8] G. Eneman, N. Collaert, A. Veloso, *et al.*, "On the efficiency of stress techniques in gate-last n-type bulk FinFETs," *Solid State Electron.*, vol. 74, pp. 19–24, Aug. 2012.

[9] G. Eneman, D. P. Brunco, L. Witters, *et al.*, "Stress simulations for optimal mobility group IV p- and nMOS FinFETs for the 14 nm node and beyond," in *Proc. IEEE IEDM*, Dec. 2012, pp. 247–250.

[10] P. Hashemi, L. Gomez, and J. L. Hoyt, "Gate-all-around n-MOSFETs with uniaxial tensile strain-induced performance enhancement scalable to sub-10-nm nanowire diameter," *IEEE Electron. Device Lett.*, vol. 30, no. 4, pp. 401–403, Apr. 2009.

[11] R. A. Minamisawa, M. J. Süess, R. Spolenak, *et al.*, "Top-down fabricated silicon nanowires under tensile elastic strain up to 4.5 %," *Nature Commun.*, vol. 3, p. 1096, Oct. 2012.

[12] M. J. Süess, R. Geiger, R. A. Minamisawa, *et al.*, "Analysis of enhanced light emission from highly strained germanium microbridges," *Nature Photon.*, vol. 7, pp. 466–472, Apr. 2013.

[13] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. New York, NY, USA: Springer-Verlag, 2008.

[14] C. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, 1954.

[15] J.-S. Lim, S. E. Thompson, and J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 11, pp. 731–733, Nov. 2004.

[16] Y. Ekinci, M. Vockenhuber, B. Terhalle, *et al.*, "Evaluation of resist performance with EUV interference lithography for sub-22 nm patterning," *Proc. SPIE*, vol. 8322, pp. 83220W-1–83220W-11, Mar. 2012.

[17] R. A. Minamisawa, M. Schmidt, L. Knoll, *et al.*, "Hole transport in strained $Si_{0.5}Ge_{0.5}$ QW-MOSFETs with (110) and (100) channel orientations," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1105–1107, Aug. 2012.