Ga^+ focused ion beam lithography as a viable alternative for multiple fin field effect transistor prototyping

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A novel method for fast and flexible fin field effect transistor (FinFET) prototyping using a Ga^+ focused ion beam is presented. The fin width and height control is explored, aiming for the successful fabrication of prototypes. This method results in fins with negligible Ga incorporation, when compared to traditional focused ion beam milling techniques. Our method for multiple fin FinFET prototyping enables advanced device fabrication and great flexibility regarding both the number of fins and fin width. Working FinFET prototypes have been fabricated using the proposed fin definition method, and the electrical characterization is discussed. © *2016 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4963879]

I. INTRODUCTION

Ion beam approaches for nanopatterning have gathered significant attention in the last few years, with improved controllability and versatility.[1] When compared to electron beam lithography, considerable advantages are observed due to the reduced lateral scattering, since ions are several orders of magnitude heavier than electrons. Low line width and line edge roughness are reported for ion beam lithography, especially when employing low mass ions such as helium.[1–4]

Flexibility is greatly enhanced when ion beam solutions are employed. By tailoring parameters such as ion mass, acceleration voltage, and dose, a wide range of applications can be addressed.[5] Examples range from transmission electron microscopy sample preparation[6] to junctionless-FET (Refs. 7 and 8) and FinFET (Ref. 9) fabrication, with important contributions in microelectromechanical systems (MEMS)[10] and failure analysis.[11,12] Focused ion beam (FIB) for device fabrication has two main approaches: milling and lithography. While several works have been carried out using milling and ion-assisted material deposition for transistor fabrication,[7–9,13,14] here we explore a maskless and resistless lithography method for nanoscale multiple fin definition, which is used for FinFET prototype fabrication.

The Ga^+ FIB lithography relies on the formation of a thin nonvolatile mask on the silicon (Si) regions irradiated by the Ga^+ ions, when exposed to a fluorinated plasma such as SF_6 and Ar, as evaluated elsewhere.[15,16] The time required for multiple fin definition by combining the Ga^+ FIB lithography and SF_6/Ar plasma etch techniques is drastically reduced when compared to the traditional Ga^+ FIB milling. While the quantitative analysis of the Ga^+ masking mechanism, such as dose threshold and selectivity, has been performed in other works,[15,16] here we evaluate its suitability for 3D device prototyping and focus on the fabricated FinFETs and their electrical characterizations.

II. EXPERIMENT

A. Multiple fin Ga^+ FIB lithography calibration

Multiple fins are defined using Si surface modification through shallow Ga^+ implant on silicon. Using a FEI Nova Nanolab 200 with beam energy of 30 keV, a 27 nm layer of silicon is incorporated with Ga ions, according to Monte Carlo TRIM calculations.[17] Figure 1 shows the number of gallium ions that stop at each depth in the silicon substrate, for a simulation of over 70 000 ion collisions. The graph reflects the profile of the focused ion implantation (energy of 30 keV and tilt angle of 0°) performed. This incorporation is associated with material sputtering, and thus, we named the process of Ga patterned implantation as "FIB shallow cuts." The sputtering yield, calculated by TRIM, is 2.28 Si atoms for every implanted Ga ion, at 0° tilt angle. Figure 2 presents the schematic for the multiple fin definition. We used a silicon-on-insulator (SOI) substrate with a 340 nm silicon layer, thinned to different dimensions (for example, 120 nm as in the figure) by wet oxidation in 1000 °C. Optical lithography, aluminum sputter deposition, and lift off create hard masks of additional features, for example, source and drain pads for FinFETs. Focused ion beam processing is carried out only in the regions directly on top of the fins. During silicon etching, the implanted Ga reacts with SF_6/Ar plasma producing a GaF_x nonvolatile mask that protects the fins from the etching process.[15,16] It is important to note that by combining the optical and FIB lithography techniques, both large and small patterns are defined, and the total processing time is reduced. Also, FIB lithography does not require additional resist deposition or development steps; it is a direct definition technique.

Maximum Ga^+ incorporation with minimum straggle is desired in order to fabricate fins with nanometer scale width.

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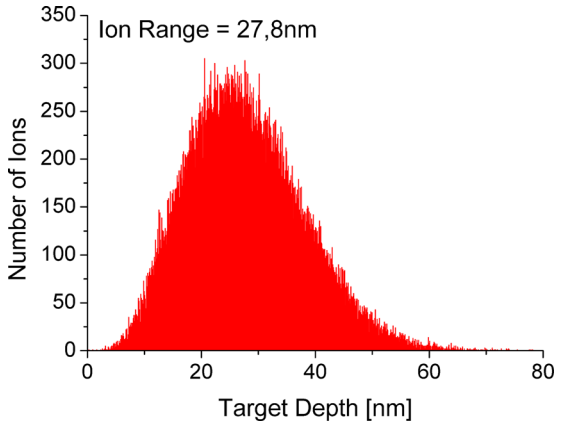

FIG. 1. (Color online) Histogram of implanted gallium ions in silicon as a function of their stopping depth. A 27 nm thick Ga rich silicon layer is formed on the silicon surface.

Different ion beam currents, from 0.5 nA to 30 pA, have been used and evaluated regarding the fin width after silicon etch. The beam energy was set to 30 keV and the cut depth to 60 nm. The substrate used for the experimental calibration was a SOI wafer with 400 nm buried oxide and 340 nm thick silicon layer, which was thinned by wet oxidation to evaluate fin height. All fins were defined in the same sample which was afterward etched using an inductively coupled plasma (ICP). With the same beam current, different cut depths were also tested, to evaluate how the cut depth influences ion straggle. The fin width was measured after silicon etch, using FIB/SEM cross sections, where the fin sidewall slope angle is also evaluated.

Once the fin definition process was calibrated, FinFET prototypes were fabricated using the method above. While calibration of the fin definition method is important, the focus of this work is on the FinFETs. The experimental procedure will be detailed in Subsec. II B.

B. FinFET device fabrication

FinFETs were fabricated on SOI substrate, as the one presented schematically in Fig. 2, but with a 340 nm thick Si layer. Thinning of the silicon layer was not carried out, in order to obtain taller fins and avoid recrystallization issues after source and drain ion implant.[18] The source and drain regions were covered with a 50 nm thick aluminum (Al) deposited by DC sputtering, which was used as an etching hard mask. Nine parallel fins, with length of 8 μm, were defined in each device using the Ga^+ FIB, with energy of 30 keV, current of 30 pA, and 150 nm cut depth. Each device is processed in 39 s. In this step, the ion beam was used only for a shallow cut of the Si upper layer of the fin structure. Using a Raith e-LINE Plus electron beam lithography system, the same structures can be defined in approximately 6 s, with resist development and hard mask definition steps still being required, however.[19,20] For reference, fin definition through silicon milling has a processing time of 10 min, when using the same ion beam current. Silicon etch was done using SF_6/Ar ICP after the FIB step, with 10 sccm of SF_6, 15 sccm of Ar, 1200 W RF power, 80 W forward power, and 20 mTorr process pressure. Three minutes sacrificial oxidation in dry ambient and 1000 °C was used to reduce sidewall plasma etch damage.

An aluminum layer was deposited on the channel to act as a hard mask for ion implantation. Phosphorus was implanted with energy of 30 keV, dose of 5×10^{14} cm^{-2} and tilt angle of 7° to form the FinFET n-doped source and drain. Rapid thermal annealing for 60 s at 1000 °C was carried out after hard mask and sacrificial oxide stripping. Silicon oxynitride (SiON) is grown by plasma oxynitridation as the gate dielectric,[21] and titanium nitride (TiN) metal gate is formed by 1 nm thick titanium e-beam evaporation and subsequent electron cyclotron resonance plasma nitridation.[22,23] An aluminum cap layer is deposited by DC sputtering to reduce the gate stack series resistance and to avoid further incorporation of oxygen in the TiN electrode in the postprocessing steps.[9] The gate last integration scheme was employed to prevent parameter shifts in the TiN electrode after high temperature annealing.[24,25] Self-alignment using chemical–mechanical planarization step is still being calibrated in our lab, which impacts our design choices. Source, drain, and gate Al landing pads are created by sputter deposition. Forming gas (92% N_2, 8% H_2) anneal at 450 °C for 6 min is performed to improve metal-silicon ohmic contact. The devices were measured using a Keithley 4200 semiconductor characterization system, and the results will be discussed in Sec. III.

III. RESULTS AND DISCUSSION

Figure 3 presents the fin width (left hand axis) and sidewall slope angle (right hand axis) as a function of ion beam current, showing that both parameters monotonically increase with ion beam current. Measurements were done

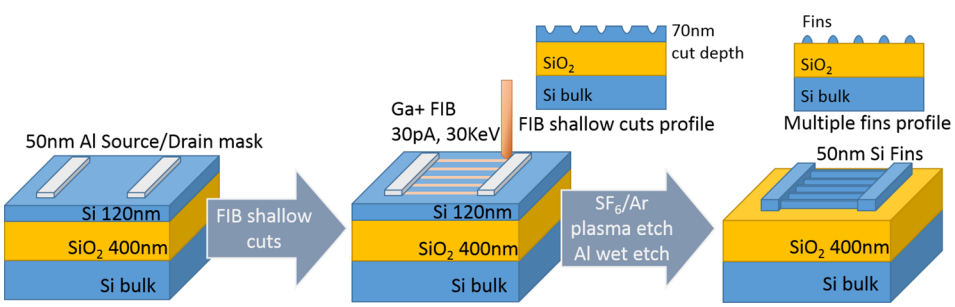

FIG. 2. (Color online) Schematic of the experimental procedure for multiple fin definition using Ga^+ FIB lithography.

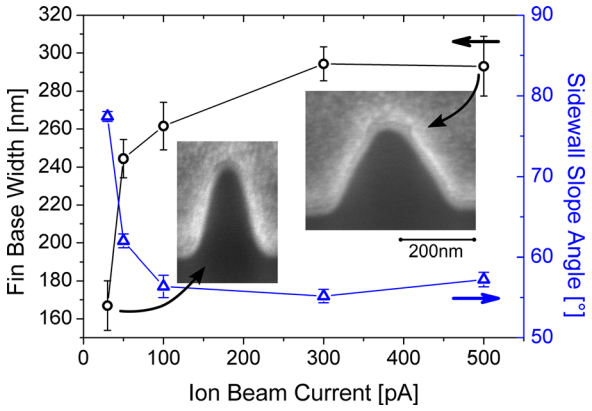

FIG. 3. (Color online) Fin base width and sidewall slope angle dependence on the ion beam current. Average and deviation values are presented for five parallel fins. The insets present fins fabricated with 30 pA (left) and 500 pA (right) currents. Smaller ion beam current result in thinner fins with steeper sidewalls.

using FIB/SEM cross sections, which are presented in the insets for a fin fabricated using a beam current of 30 pA (left) and 500 pA (right). A lower beam current results in a lower beam diameter and also reduces the lateral distribution of implanted ions, which translates in thinner fins after etching. Thinner fins with the same height, in turn, present steeper sidewalls. While the resulting fin sidewall is not vertical, with a slope lower than 90°, triangular fins are in fact expected to reduce leakage currents in FinFETs.[26]

The resulting fin width is also controlled by the cut aspect ratio. A higher aspect ratio indicates lower ion spread and thus higher Ga concentration in the desired region. Increasing the cut depth results in increased aspect ratio. The fin height, however, is controlled, by the remaining silicon layer beneath the shallow cut, creating a trade-off between the fin width and height. The cut depth of 70 nm was found to provide a good compromise between the fin width and height. By changing the SOI substrate silicon layer thickness—using wet oxidation to reduce its original thickness of 340 nm to any desired thickness—fins with different heights could be obtained, as presented in Fig. 4. Although our fins are wider than the sub-10 nm reported from the industry,[27] this should not prevent the FinFETs from working. Future etching optimizations are expected to further reduce the fin width. Also, changing the focused ion beam parameters (cut depth, beam current) could potentially result in fins with different heights without the need for an oxidation step. There is, as mentioned, a loose correlation between cut depth and resulting fin width, which leads to wider fins when more shallow cuts are employed. As such, altering the cut parameters between devices would result not only in fins with different heights but also with different widths.

For a current of 30 pA, knowing that the parallel definition of nine lines of 8 μm takes 39 s, we can estimate the implanted dose, according to Eqs. (1) and (2), where Q is the charge, t the time, q the electron charge, and A the implanted area. From the cut cross section we have that the bottom width—where most of the gallium ions are implanted—is 70 nm, and thus, the total area of the lines is 5.04×10^{-8} cm^2. The implanted dose, with the 30 pA current is then calculated as 1.44×10^{17} cm^{-2}, agreeing with Henry *et al.*,[16] which reports that a dose of 10^{17} cm^{-2} sustains a 600 nm deep etch

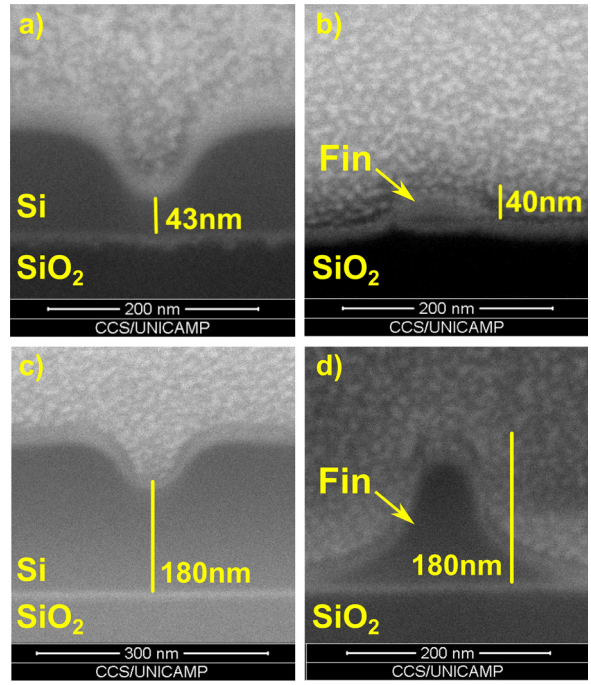

FIG. 4. (Color online) Cross sections of FIB shallow cut for Ga incorporation [(a) and (c)] and resulting fin after SF_6/Ar plasma etch [(b) and (d)].

$$I = \frac{dQ}{dt}, \tag{1}$$

$$\text{Dose} = \frac{Q \cdot q}{A}. \tag{2}$$

The Ga incorporation in the resulting silicon fins was evaluated by energy-dispersive x-ray spectroscopy (EDS), as shown in Fig. 5, which compares silicon fins fabricated by

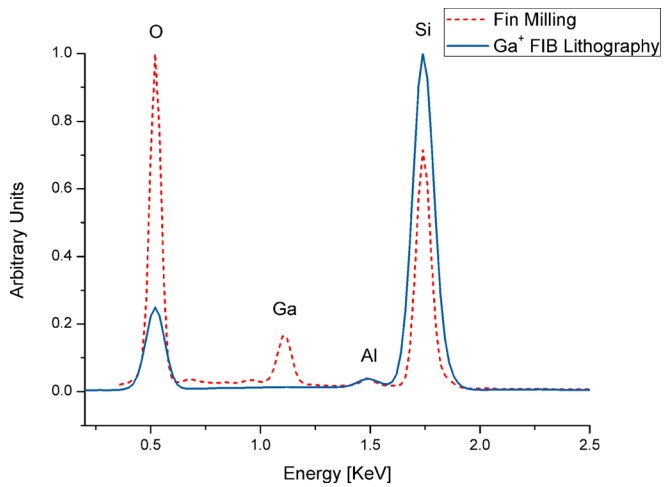

FIG. 5. (Color online) EDS spectra of fins fabricated by FIB fin milling and Ga^+ FIB lithography techniques, showing the absence of Ga peak in the latter case. This indicates a sharp reduction in Ga incorporation in devices fabricated using this method.

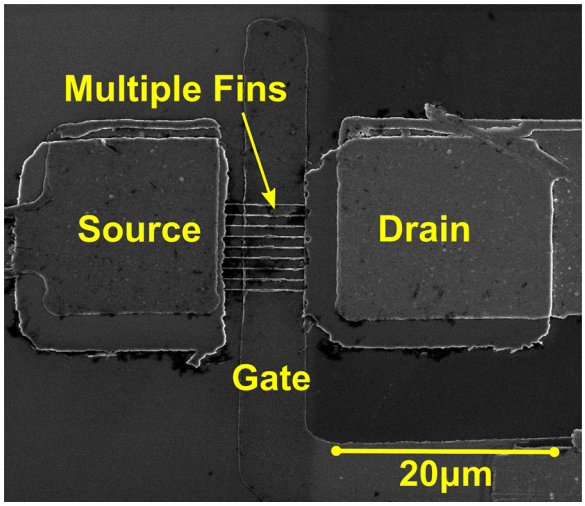

FIG. 6. (Color online) Final fabricated FinFET prototype, with source and drain regions, as well as multiple fins indicated.

FIB milling and by Ga^+ FIB lithography. In the latter case, negligible Ga is identified after SF_6/Ar plasma etch, indicating that either the nonvolatile GaF_x etch mask is sputtered away or the atomic concentration of Ga is below the detectable limit of EDS equipment. In the latter case, residual gallium exists and will still affect the electrical characteristics. Nevertheless, it is possible to conclude that this technique sharply reduce process-induced Ga incorporation, when compared to more traditional milling techniques. Gallium is a p-type dopant in silicon, and thus reducing its concentration when fabricating MOSFET devices is desired. In modern FinFET devices, for example, the body doping should be kept to a minimum, to avoid nonuniformities which contribute to threshold voltage (V_{TH}) shifts.[28]

The fabricated FinFET prototype is presented in Fig. 6, with source, drain, gate, and multiple fins indicated. It can be noted that our technique successfully defined the multiple fins, and a complete FinFET could be fabricated.

Electrical measurements in Figs. 7–9 show that the devices work as nMOS transistors, with the gate electrode

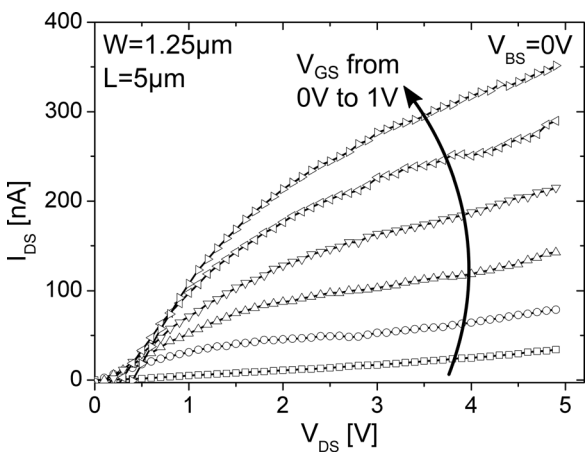

FIG. 7. Electrical $I_{DS} \times V_{DS}$ characterization of the fabricated FinFET prototypes, showing that the gate electrode controls the current in the multiple fins.

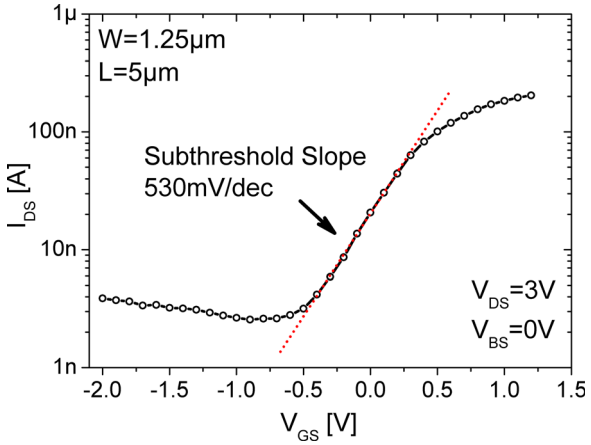

FIG. 8. (Color online) Logarithmic $I_{DS} \times V_{GS}$ curve, highlighting the subthreshold characteristics.

controlling the drain current. FinFET channel width (W) and length (L) are presented in each graph. The curve superimposition observed in the $I_{DS} \times V_{DS}$ graph in Fig. 7, for low V_{DS} values, is due to high gate leakage currents allied with high contact resistance. The high contact resistance reduces significantly the drive current, which in this case is below 400 nA with 1 V of V_{GS} and 5 V of V_{DS}. With a low overall drain current, the gate leakage current becomes proportionally more significant, and at low V_{DS} values, measurement superimposition can be observed. This was verified through Silvaco ATLAS simulations.[29] Gate leakage current comparable to the drain current (e.g., greater than 10 nA) is an indicative of issues in our SiON, which has 3.6 nm of equivalent oxide thickness (EOT), since quantum mechanical tunneling current becomes significant only in oxides below 2 nm thick.[30]

Leakage issues result in substandard subthreshold characteristics, presented in the logarithmic $I_{DS} \times V_{GS}$ curve in Fig. 8. A subthreshold slope of 530 mV/dec indicates that, although working, the transistor is far from optimal. Sloped—and possibly rough—fin sidewalls result in poorer dielectric interface, which can also contribute to degrade the subthreshold characteristics.[31] Further improvements in the plasma etching are expected to improve this interface,

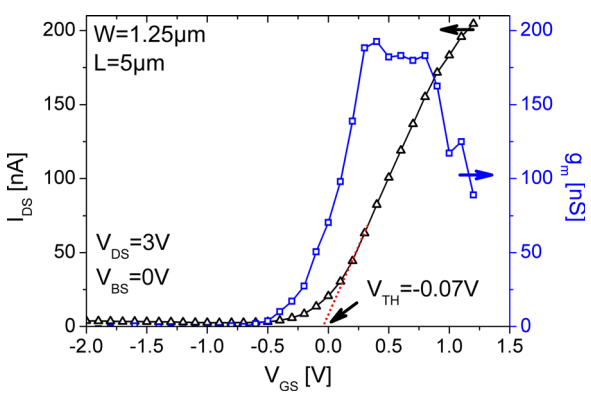

FIG. 9. (Color online) Linear $I_{DS} \times V_{GS}$ measurement shows that cutoff and conduction regions are distinguishable in the FinFET.

reducing the interface trap density, and consequently the subthreshold slope.[32]

In the linear $I_{DS} \times V_{GS}$ curve (Fig. 9), the cut-off and conduction regions are easily discernible, and a V_{TH} of -0.07 V is obtained by extrapolating the linear region of the I_{DS} measurement. For a FinFET with undoped or lightly doped channel and with fins wider than 20 nm, V_{TH} can be modeled as shown in Eq. (3).[33] The channel doping is estimated as 1×10^{16} cm^{-3} after Ga^+ FIB processing. This relatively high channel doping accounts for the fact that no trace of Ga in the EDS spectrum (Fig. 5) does not mean that incorporation is totally absent. With this doping level, however, transistor can still be considered undoped or lightly doped, for modeling purposes.[34] We have that a V_{TH} of -0.07 V is equivalent to a TiN gate work function (ϕ_m) of 4.54 eV, knowing that the oxide capacitance (C_{ox}) is 287 nF/cm^2, the silicon fin width (t_{Si}) is 100 nm, the temperature (T) is 22 °C (295 K), and the silicon work function (ϕ_{Si}) is 4.96 eV to account for the light Ga doping. The electron charge (q), Boltzmann constant (k), and intrinsic carrier density (n_i) are taken from the literature. Separate gate stack capacitance–voltage (C-V) measurements, performed in planar gate stack structures, resulted in TiN metal work function between 4.5 and 4.7 eV, consistent with the value calculated from the FinFET threshold voltage

$$V_{TH} = (\phi_m - \phi_{Si}) + \frac{k \cdot T}{q} \ln\left(\frac{2 \cdot C_{ox} \cdot k \cdot T}{q^2 \cdot n_i \cdot t_{Si}}\right). \quad (3)$$

The transconductance (g_m) indicates the variation in I_{DS} for an increase in V_{GS}, and for our FinFETs, it is presented in the right-hand axis in Fig. 9. A maximum transconductance of nearly 200 nS is still low for FinFETs.[34] This parameter is strongly influenced by both the channel length (L) and EOT, and our 5 μm L FinFETs with 3.6 nm SiON dielectric are bound to present such low values. In this work, however, we are focusing in a proof-of-concept, to present the Ga^+ FIB lithography method as a viable alternative for FinFET fabrication, whereas future works will focus on gate length and oxide thickness reductions, which will significantly increase the transconductance. Reducing scattering mechanisms also contribute to improve the transistor performance by increasing the carrier mobility. The main source of mobility scattering is sidewall roughness or charged states in the silicon–oxide interface. One solution to improve this interface is to perform a high temperature annealing to reduce vacancies and trapped charges in the plasma grown SiON gate dielectric.[35,36] Reducing the defect density in the dielectric will also mitigate the gate leakage current issues on the fabricated FinFET prototype.

IV. SUMMARY AND CONCLUSIONS

We demonstrated a novel method for FinFET prototype fabrication using the focused ion beam and discussed its viability. The Ga^+ FIB lithography method for multiple fin FinFET prototyping is faster than traditional FIB milling and enables advanced device fabrication, with flexibility regarding both the number of fins and fin width. It also reduces process induced gallium incorporation, minimizing its influence on FinFET electrical characteristics. In this work, we proposed the Ga^+ FIB lithography as a proof-of-concept, and it can be optimized with further studies. By combining our direct patterning with optical lithography we define both small and large features, thus using each technique's advantages. Moreover, when comparing to other serial lithography methods, ours present only slightly higher processing time per device, with the added advantage of defining the fins directly on silicon. As such, there is no need for additional process steps such as resist coating, development, and hard mask etching that can be challenging in the nanoscale. Therefore, this new lithography method is a viable alternative for initial FinFET prototyping.

Although our initial results on fin definition are wider than reports from the industry, they show interesting developments for device prototyping. Future etching optimizations are expected to reduce the fin width. A FIB/SEM system is a versatile equipment, and in conjunction with this technique, complex prototype devices can be more easily fabricated in smaller research institutes. Initial electrical results are presented, with working FinFETs. Although lacking in performance, the results point that this technique is viable for FinFET prototyping. Optimizations to the FinFET fabrication flow (e.g., self-aligned gate, high-κ dielectric, and source and drain silicidation) can render improved electrical characteristics.

These results are valuable due to the importance of device prototyping in the development cycle of new materials and techniques. Moreover, while in this work we applied the Ga^+ FIB lithography technique for FinFET fabrication, it could potentially be used for vertically integrated nanowire FETs or other complex devices.

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