UNIVERSIDADE ESTADUAL DE CAMPINAS
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ASIC Implementation of a MR-FSK Modem Compliant with IEEE 802.15.4g Standard

Implementação em ASIC de um Modem MR-FSK Aderente ao Padrão IEEE 802.15.4g

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Orientador: Prof. Dr. Luís Geraldo P. Meloni

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A Ata de Defesa, com as respectivas assinaturas dos membros da Comissão Julgadora, encontra-se no SIGA (Sistema de Fluxo de Dissertação/Tese) e na Secretaria de Pós-Graduação da Faculdade de Engenharia Elétrica e de Computação.

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“A vida merece algo além do aumento da sua velocidade.”
(Mahatma Gandhi)

ABSTRACT

This work presents a fully integrated Multi-Rate and Multi-Regional Frequency Shift Keying (MR-FSK) modem compliant with IEEE 802.15.4g standard for Smart Metering Utility Networks (SUN). The total chip die area is 884,400.0 μm^2 and the modem power consumption is 63.17 μW. The architecture of the modem is depicted with a brief study of baseband and intermediary frequency demodulator techniques. Besides, those resource estimations for ASIC and FPGA are presented in order to assist the construction of SUN system and applications, such as Advanced Metering Infrastructure (AMI).

Keywords: MR-FSK, IEEE 802.15.4g, SUN.

RESUMO

Esse trabalho apresenta um modem MR-FSK (Multi-Rate and Multi-Regional Frequency Shift Keying) completo, compatível com a norma IEEE 802.15.4g, para Smart Utility Networks (SUN). A área total do chip é 884.400,0 μm^2 e o consumo de energia do modem é 63,17 μW. A arquitetura do modem é mostrada, com um breve estudo de técnicas de demodulação em banda base e frequência intermediária. Além disso, estimativas do uso de recursos são apresentados para ASIC e FPGA, com o intuito de auxiliar a construção de sistemas SUN e suas aplicações, como AMI (do inglês: *Advanced Metering Infrastructure*).

Palavras-chaves: MR-FSK, IEEE 802.15.4g, SUN.

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1 INTRODUCTION

Applications focusing on real-time energy metering, which enables the efficient management of information, have a potential impact upon utility distribution. Remote devices based on wireless sensor networks providing energy data and automatic pricing system can reduce the operational cost of manual reading at the consumers' houses (LIU, 2012).

Such applications, most specifically Smart Metering Utility Networks (SUN) applications, with low-rate and low-energy consumption characteristics, can have a considerable impact on lifestyle (MA et al., 2013). These applications have systems requirements not fulfilled by existing 802 standards established by IEEE, such as network robustness, prolonged battery lifespan, and communication range (KOJIMA et al., 2015). In the context of Low Rate (LR) Wireless Personal Area Network (PAN), the IEEE established the amendment IEEE802.15.4g (IEEE, 2011) at the IEEE802.15.4 standard (IEEE, 2006), targeting SUN applications. The amendment's purpose is to provide a global standard focused on facilitating very large-scale process control applications, such as those used in smart-grid network (HEILE, 2008). It should also support geographically large networks with minimal infrastructure. Three Multi-Rate Multi-Regional (MR) physical layers (PHYs) are proposed in the standard to be compatible with different market applications. Such standard PHYs are MR-FSK (Multi-Rate Multi-Regional Frequency Shift Keying), MR-OQPSK (Multi-Rate Multi-Regional Offset Quadrature Phase Shift Keying, and MR-OFDM (Multi-Rate Multi-Regional Orthogonal Frequency Division Multiplex).

1.1 Problem Contextualization

This work is part of a project targeting ASIC implementation of a complete transceiver compliant with IEEE.802.15.4g standard (IEEE, 2011), containing all the three PHYs. This work's main goal is to implement an MR-FSK modem, covering all the standard specifications. The specific objectives to achieve that goal are literature review, FSK (Frequency Shift Keying) and GFSK (Gaussian Frequency Shift Keying) models, simulations over AWGN (Additive White Gaussian Noise) channel, architecture definition, and implementation in FPGA and ASIC. It was determined to implement both GFSK and FSK modulations for the MR-FSK PHY. Other PHYs like MR-OFDM and MR-OQPSK proposed in the standard have the implementation and characteristics described in (ALVES et al., 2016), (SILVA et al., 2017) and (ALVES; LIMA, 2016). This work was already presented in the paper (OLIVEIRA et al., 2016).

In order to better understand the IEEE802.15.4g protocol's role, few topics will be introduced and later discussed in this section. Smart Grids are fundamental to provide efficient, reliable, and safe energy automation service. Through Advanced Metering Infrastructure (AMI), it can give advance monitoring and control applications (ELSER, 2013). A fundamental part of smart grid operability is communication technologies that guarantee the quality, data availability, security, and good coverage (DEPURU et al., 2011). The standard here in focus (IEEE 802.15.4g) comes as a solution to the communication requirements, focusing SUN applications. The Wi-SUN alliance promotes the standard establishing HAN and FAN profiles. All these subjects are going to be further detailed in the current chapter.

1.1.1 Smart Grid

The motivation for Smart Grids comes from climate changes, along with the rising quantity of electric components and the phenomena of declining reliability and power quality (LO; ANSARI, 2012). Renewable energy sources can be a solution for many of those problems. However, intermittency of generation and lack of distributed control algorithms are barriers to its integration into existing grids (FAN et al., 2013).

Smart Grid can provide efficient, reliable, and safe energy automation service with two-way communication. Due to its self-awareness, smart grids can reconfigure, coordinate and heal itself, characterizing the intelligence of the grid (LO; ANSARI, 2012).

Smart metering is a major component of the overall smart grid communications architecture. Smart meters are a two-way communication devices that provide real-time energy consumption information (DEPURU et al., 2011). It enables capture and analysis of data related to power usage, delivery and generation (LIU, 2012), enhancing the operation of the connected devices from the generation plant to the distribution system (SHABANI et al., 2016). The entire grid status and performance in real time is known and understood, based on the information that it receives. According to (LIU, 2012), smart grid can provide predictive power information (e.g., meter reading data, monthly charge, and power usage recommendation) for both utilities and consumers (LO; ANSARI, 2012).

1.1.2 AMI

Advanced Metering Infrastructure (AMI) integrates technologies in different infrastructure hierarchies to achieve its goals, using components such as smart meters, communication networks and Meter Data Systems (MDMS) (MOHASSEL et al., 2014). AMI have an important role on smart cities development, where extensive data will flow from many sources through many communication networks, in order to provide benefit

for all the people in smart cities. AMI will allow two-way communication between smart electricity, gas and water meters at utility companies, enabling control and measurement of utilities consumption (ULLAH; FAHEEM; KIM, 2017).

AMI networks are composed by millions of endpoints, including smart meters, distribution automation elements and, eventually, Home Area Network (HAN) devices. They are typically interconnected using a combination of wireless and power-line communications (MOHASSEL et al., 2014).

Due to its larger degree of freedom for information collection, dissemination and processing, wireless communication networks are presented as a more viable and practical solution than wired communication infrastructure, especially for Smart Grid networks which extends the last mile communications, connecting smart meters to advanced metering infrastructure (AMI) access point (GHARAVI; HU, 2011)

1.1.3 Smart Meters Communications

Smart meter communication is a vital part of the Smart Grid. Data flow from the smart metering to the grid is used to assist grid control and to identify the demands. Information from the grid to the end-user provides incentive to the consumer to adapt their consumption (FAN et al., 2013). Quality, data availability and security of data transmission must be guaranteed, hence, the communication technology must be well evaluated as they have to be cost-efficient, provide good coverage and power quality with the least number of repetitions (DEPURU et al., 2011).

Smart meter communication networks typically links Wide Area Network (WAN), local area network (LAN) and occasionally Home Area Network (HAN). HAN allows communications from the smart meter installed into the home to the user, with information about energy consumption, for example. LAN, for instance, covers the communication between the meter and a substation or any other data concentrator. WAN links that data concentrator to a utility Back-End system (ERLINGHAGEN; LICHTENSTEIGER; MARKARD, 2015). In the Smart Grid context, Neighborhood Area Network (NAN) often fulfill the gap between HANs and WANs, with the last one acting as a backbone communication between NANs and utility control centers (YU et al., 2011). Smart Grid NANs implementation has the challenge to connect large amount of communication nodes in a complex large geographical area (YU et al., 2011), directly connecting end users in a regional area, forming a primary sector to the power grid. That can determine the whole grid efficiency through the capacity of controlling and monitoring electricity delivery, in order to adapt distribution according to each user demand and energy availability (MENG; MA; Chen, 2014). Those are examples of the smart meters communication requirements that vary substantially in distance and data volume. Hence, different technological and standards options must be considered for

each situation (ERLINGHAGEN; LICHTENSTEIGER; MARKARD, 2015).

1.1.4 IEEE 802.15.4g

The addendum to the IEEE 802.15.4 standard is responsible to define medium access control (MAC) and PhysicalLlayers (PHY) for low-rate, low-data and low-power consumption (IEEE, 2006), focusing on Smart Utility Networks (SUN) applications that have systems requirements not fulfilled by existing 802 standards, such as network robustness, prolonged battery lifespan, and communication range (LU, 2014). This amendment uses a multi PHY approach to support initially outdoor wireless low-data-rate and smart utility network applications, in the context of Low Rate (LR) Wireless Personal Area Network (PAN) (IEEE, 2011). Its purpose is to provide a global standard focused in promoting very large-scale process control applications, such as those one used in Smart Grid network (HEILE, 2008). It should also support geographically large networks with minimal infrastructure.

In order to be compatible with different market applications, three Multi-Rate Multi-Regional (MR) Physical Layers (PHYs) are proposed by the standard, named as MR-FSK (Multi-Rate Multi-Regional Frequency Shift Keying), MR-OQPSK (Multi-Rate Multi-Regional Offset Quadrature Phase Shift Keying) and MR-OFDM (Multi-Rate Multi-Regional Orthogonal Frequency Division Multiplex). The focus of this work will be the MR-FSK PHY. Those three alternative PHYs provide a large range of parameters and configurations to deal with all requirements defined by the IEEE Project Authorization Request (PAR), listed below:

1. Operation in any of the regionally available not certified frequency bands, such as 700 MHz to 1 GHz, and the 2.4 GHz band;
2. Data rate between 40 kbps and 1000 kbps;
3. Achieve the optimal energy efficient link margin given by the environmental conditions encountered in smart metering deployments;
4. Mainly application in outdoor communications;
5. A minimum of 1500 octets to PHY frame sizes;
6. At least 3 co-located orthogonal networks operating simultaneously;
7. A minimum of one thousand direct neighbors connections, characteristic of dense urban deployments;
8. Enable coexistence with other systems in the same band(s) including IEEE 802.11, 802.15 and 802.16 systems (HEILE, 2008).

1.1.5 SUN

Smart Metering Utility Network (SUN) is defined by IEEE 802.15.4g as a shared network resources that provides monitoring and control to the utility systems devices, designed to operate in low-power wireless and large-scale applications (IEEE, 2011), including electricity, gas and water utilities services. The network main information is the data collected from sensor, used to monitor machines and transmit commands over an unlicensed frequency band (LIU, 2012). Both utility providers and utility consumers are benefit by full duplex communication between end-user and control entity, which apply complex command and control features to optimize power and resource management (KOJIMA et al., 2015).

1.1.6 WI-SUN

Wireless Smart Ubiquitous Network (Wi-SUN) is a technology based on IEEE 802.15.4g and promoted by WI-SUN Alliance™, a global organization created in 2011 to endorse the adoption of smart utility networks as detailed in IEEE 802.15.4g (ALLIANCE, 2017b). With the purpose of leading the challenge to optimize and automate metering control monitoring, Wi-SUN Alliance is driving the Smart Ubiquitous IoT (Internet of Things) Network applications, focusing on interoperability (ALLIANCE, 2017a). Wi-SUN Alliance consists of more than 130 companies, of various types, that contributes to Wi-SUN ecosystem. They define testing and certification programs for multi-vendor interoperability.

The Wi-SUN technology provides some advantages like low latency and high data rates that are consistent throughout the network support to IPv6 protocols and support to Mesh networks scaling in capacity and size (MAYETTE, 2016). There are already several Wi-SUN compatible products and components in use by many companies.

Smart Utility Networks applications were initially the main focus of Wi-SUN technologies, but with analysis of the technology characteristics and advantages, Wi-SUN Alliance started to provide support to Ubiquitous applications, covering IoT applications as well.

1.1.7 FAN and HAN Profiles

Field Area Network (FAN) and Home Area Network (HAN) profiles were defined by Wi-SUN Alliance. FAN profile specification enables interoperable, multi-service and IPv6 communication over IEEE 802.15.4g on enterprises and service providers. That specification enables resilient, secure and cost effective connectivity from dense urban neighborhoods to rural areas through mesh-enabled field area networks

(MAYETTE, 2016). HAN profile specifications cover communication between user and smart meter device, providing energy consumption information (ERLINGHAGEN; LICHTENSTEIGER; MARKARD, 2015).

1.1.8 MR-FSK

The Multi-Rate Multi-Regional Frequency Shift Keying (MR-FSK) is the mandatory PHYs for the IEEE 802.15.4g, and focus of this work. It consists on level 2 or 4 FSK or GFSK modulation with configurations that can cover several frequency bands and data rates from 2.4 kb/s to 400 kb/s, including narrowband modulation from 2.4 kb/s to 40 kb/s. As an example, for the worldwide used ISM (Industrial, Scientific and Medical) band of 2400-2483.5 MHz, the modulation scheme to be used is 2FSK, with data-rate of 50 kHz. The standard specify a frame format for the PHY, as well as data processing blocks, like forward error correction (FEC) or data whitening (DW); those will be further detailed through the next chapters.

1.2 Work Organization

This work is organized as follows. The current chapter presents subjects related to research contextualization, like the IEEE 802.15.4g standard, and its applications and technologies. In the next chapters, a literature review will be given at Chapter 2, followed by MR-FSK overview at Chapter 3. Further details in terms of high level is presented at Chapter 4 and hardware implementation is presented at Chapter 5, highlighting FSK/GFSK modem implementation and performance. Synthesis and performance results will be presented at Chapter 6, followed by the work conclusions.

2 LITERATURE REVIEW

The main scope of this work was based on standard interpretation; few papers covering specific parts of the project were used, but there is no literature showing a complete system that can be fairly compared to the work here presented. Some similar architectures will be exposed and explained in this section. In addition, papers covering GFSK and FSK modems implementation, with methods performance comparison are presented and were used for deciding demodulation methods.

The first paper presented focus on MR-FSK implementation (OH et al., 2014). The article shows a fully integrated MR-FSK System-on-Chip (SoC), compliant with IEEE 802.15.4g, which implementation includes a RF/Analog transceiver, a digital modem, MAC layer and security functions. As a result, power consumption and die area are presented. With focus on the integrated system, not much details on dataflow are given, but it is specified that scrambling/descrambling blocks and channel codification/decodification blocks were implemented. In addition, the digital demodulation implements a CFO (Carrier Frequency Offset) and FSK signal demodulation is done by phase differentiation. No GFSK modem is covered by this work. In conclusion, no equivalence can be found, since the results showing digital area include MAC implementation and the digital modem do not include frequency modulation, which is done in analogue domain.

Paper (WU et al., 2016b) shows an architecture for the Micro-Power Wireless Data Transmission Protocol (MPWDTP), for wireless AMR (Automatic Meter Reading) applications, a technology that has an important role in the Smart Grid. This approach uses GFSK modulation and all-digital baseband circuits, targeting SoC (System on Chip) implementation. Signal demodulation is done with a trigonometric sum and difference operation calculator (SDO), arc-tangent function (ATAN) calculator and a symbol decision circuit. The paper also covers a symbol synchronizer (Sync) algorithm, with few implementation details given, presenting schematics of the complete system, as well as area and power results, for PHY and MAC layers. Once again, this paper can not be directly compared, but the results regarding GFSK modem performance were taken into consideration.

There are other works with focus on IEEE 802.15.4g, but in different PHYs implementation. In (ALVES et al., 2016) the architecture for MR-OFDM digital modem supporting all data rate options and MCS codes, is described, including dataflow description, and also presenting synthesis results. In (ALVES; LIMA, 2016), more details of OFDM digital modem are given. Frame synchronization, together with a complete

functional hardware implementation is the main subject of the paper, with performance results. Paper (SILVA; LIMA; CHAVES, 2016), for once, introduce a frequency dispreading method, comparing performance improvement results with other techniques. For the MR-OQPSK, details of algorithms used in implementation are given in (SILVA et al., 2017), focusing on area optimization and implementation for ASIC.

In the early stages of this work, the MR-FSK digital modem compliant to IEEE802.15.4g was already described in (OLIVEIRA et al., 2016). An initial architecture design and implementation was approached, concerning only FSK modem, with area and power results. Up to this date, a vast number of modifications in the architecture were made, for the modem to be compliant with all operations modes and frequencies band stipulated by the standard. Signal processing blocks for synchronization and frequency correction were added, as well as blocks for ASIC testing. All this modifications will be detailed on this work.

It can be interpreted by the standard, that MR-FSK supports FSK or GFSK modulations schemes. For both modem implementation, papers were examined. GFSK is the modulation used by Bluetooth. Hence, there are several articles exploring demodulation techniques and performance. In (YU; YANG; CHONG, 2011), (ABDALLAH et al., 2015) and (HE et al., 2008), GFSK modulation is mathematically explained and (CHANG; SHIN, 2006) shows a digital implementation approach for GFSK modulator. Modem implementations with performance analysis can be found in (SCHIPHORST; HOEKSEMA; SLUMP, 2002), (JIA; NALLANATHAN; GARG, 2002), (T; BISWAGAR, 2017), (HE et al., 2008), (XIA et al., 2003) and (YU; YANG; CHONG, 2011). The method of phase differentiation, explained in (SCHIPHORST; HOEKSEMA; SLUMP, 2002) is used in this work, due to simple implementation associated with good performance.

FSK is a well known modulation hence, mathematical explanation can be found in many books. In (MCCUNE, 2010), mathematical and a more practical implementation can be found. (SKLAR, 2001) explains about coherent and non-coherent detection. For non-coherent detection, the book demonstrates two different approaches. A correlation with energy measurement, without phase information. The demodulator consists in two branches, where each one evaluates the correlation between the received signal and two reference waves with the tone frequencies for the two symbols. In each of this branches it is performed a squaring operation. The data output is decided upon maximum energy between both branches. The second approach covered by the book uses bandpass filters and envelop detection. The bandpass filters are centered in each of the frequency tones that carries symbol information. Each filter output is input for envelop detection, which consists of a rectifier and a lowpass filter. The decision is done based on the maximum amplitude between the envelop output. This approach is also well known and was the first approach for binary FSK demodulation

in this work. Then, there was a need for adapting demodulation scheme and the first non-coherent approach shown was implemented. The reasons are presented further in the dissertation.

(ZGAREN; MORADI; SAWAN, 2015) shows the use of FSK for medical applications, with low-power characteristics, using FSK to ASK demodulation technique, with a wakeup system for the receiver. The system is built to support high data rates with low-power consumption, and these characteristics were validated in fabrication.

For the data processing part of the modem, a few references were used, when applicable. Data processing algorithms are established by the standard in the modulation part. Some of the processing blocks, like data whitening (wich will be explained in 4.1.4) have a straightforward implementation, yet, for data codification algorithm specified by the standard, there are a few algorithms for the decoding process. (WICKER, 1995), gives an insight on convolutional encoders, which are used by the standard. The well know Viterbi decoding algorithm is detailed as an optimum approach for decoding convolutional codes, which was used in this work. Interleaving is another data processing algorithm used by the standard, (ANDREWS; HEEGARD; KOZEN, 1997) gives a mathematical approach for it, and also present insights on hardware implementation.

3 MR-FSK OVERVIEW

This chapter will show an overall of the MR-FSK transceiver, with main focus on theoretical aspects of FSK and GFSK modulators, details of control parameters, and a first glance at data processing and signal processing.

At the multi-PHY layer design proposed by the IEEE 802.15.4g standard, the MR-FSK (Multi-Rate Multi-Regional Frequency Shift Keying) is mandatory PHY. The three PHYs were designed to provide high flexibility and diversity. Modulation parameters (i.e data rate and modulation order) are defined by the standard, as well as data processing blocks. Figura 3.1 shows a simplified schematic of the MR-FSK diagram, given by the standard, with Forward error correction, and data whitening blocks as non-mandatory, and remaining blocks related to frame generation and modulation.

In this work, the modulator and demodulator are the group of data processing blocks, and signal processing blocks responsible for complete package reception in the transmitter and management portion, respectively. Blocks responsible for FSK or GFSK signal modulation and demodulation will be refered as signal modulators or signal demodulators.

In this and at the following chapters, data and signal processing blocks are defined for construction of the MR-FSK system. The first blocks are used to manipulate bit data, like forward error correction, data whitening and concatenation. The last blocks applies processing in the signal domain, like the signal modulation blocks.

This chapter gives an overview on data processing and signal processing for the MR-FSK. Then, algorithm implementations are detailed. Subsections 4 describes the system modeled at Matlab, a high-level language, as a golden model. Afterwards, at Subsection 5, all modules implemented using the VHDL hardware description language are depicted.

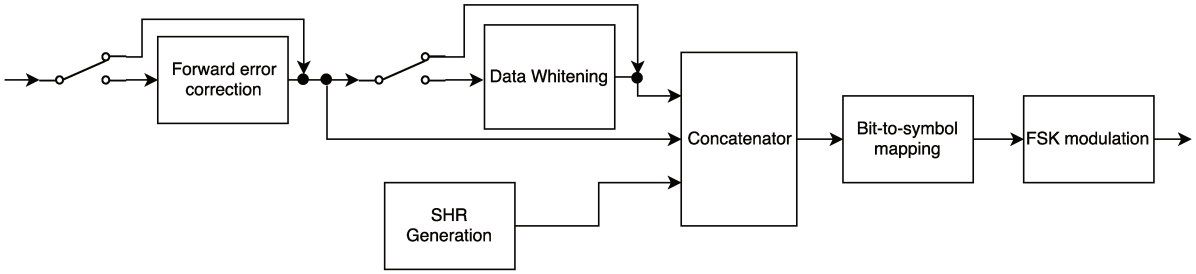


Figura 3.1 – MR-FSK PHY modulator architecture.

3.1 Data Processing

Data processing block applies transformation or analysis in data bits at transmitter and receiver. The standard establishes mandatory and non mandatory blocks in the modulator portion. This work implements all data processing blocks. The majority of the blocks were implemented by the author, which will be made explicit in the implementation Subsections 4 and 5.

Demodulator architecture is not a straightforward implementation, since it is not defined by the standard. The algorithms for retrieving data at receiver had to be defined appropriately for the project, in terms of area reduction or ease of implementation. Therefore, for each data processing block at modulation, there is an equivalent block at demodulation. For instance, for the Forward Error Correction (FEC) presented at both transmission sides. the Viterbi algorithm was implemented for FEC at receiver.

3.2 Signal Processing

Signal processing applies modification or analysis on the signal. The signal processing portion of MR-FSK, consists in signal modulation and demodulation. The standard defines two types of signal modulation schemes that can be used for the MR-FSK: FSK (Frequency Shift Keying) and GFSK (Gaussian Frequency Shift Keying), also known as filtered FSK. Some modulation parameters are defined by the standard according to Personal Area Network Information Base (PIB) attributes, some of them shown in Table 3.1. Those parameters can be changed in a frame-by-frame fashion, by MAC, in the modulator, or by reception of a mode switch frame, which will not be detailed on this work.

Table 3.1 shows part of the complete table with all attributes required to manage a PHY, defined in (IEEE, 2006). One of these parameters is the *ModulationScheme*, which defines the modulation scheme to be used. IEEE 802.15.4g also defines two modulation order to be used by the MR-FSK PHY (*FSKModulationOrder* parameter in Table 3.1), a 2-level or 4-level modulation, also known as 2FSK, 4FSK or 2GFSK or 4GFSK, depending on modulation scheme. It is worth to mention that in this work it was only implemented a 2FSK modem, only. Nevertheless, extension to 4FSK and 4GFSK is straightforward. Other modulation parameters, regarding modulation frequency, depends on the frequency band and operation mode defined in (IEEE, 2006). These two parameters define modulation index, data rate and channel spacing.

In the worldwide ISM frequency band of 2400-2483.5 MHz, the modulation scheme to be used as defined in the standard, is 2GFSK, as shown in Table 3.2. The symbol rate (f_{symbol}) and modulation index (h) determine the frequency deviation (f_{dev})

Tabela 3.1 – PHY Personal Area Network Information Base (PIB) attributes.

Name	Type	Valid range	Description
ModulationScheme	Integer	0–3	The modulation scheme of the MR-FSK Generic PHY entry. This parameter can take one of the following values: 0 = FSK 1 = GFSK 2–3 = reserved The remaining parameters in this table are determined based on the value of the ModulationScheme parameter.
FSKModulationOrder	Integer	0–3	The modulation order for a value of ModulationScheme 0 or 1. This parameter can take one of the following values: 0 = 2-level 1 = 4-level 2–3 = reserved.
FSKModulationIndex	Float	0.25–2.50	For a ModulationScheme parameter values of zero or one, FSKModulationIndex is the modulation index.
FSKBT	Integer	0–3	The BT value if the value of the ModulationScheme parameter is one. This parameter can take one of the following values: 0 = BT is 0.5 1 = BT is 1.0 2–3 = reserved

of FSK or GFSK pulses by Equation 3.1:

$$f_{\text{dev}} = f_{\text{symbol}}\, h/2, \tag{3.1}$$

where the symbol rate is related to the data rate by:

$$f_{\text{symbol}} = \begin{cases} f_{\text{data}}, & \text{for 2-level modulation} \\ f_{\text{data}}/2, & \text{for 4-level modulation.} \end{cases}$$

As a matter of example, Table 3.2 shows the parameters of MR-FSK PHY according to IEEE 802.15.4g used in commonly applicable regulatory domains such as Worldwide (2400-2483.5 MHz), US (902-928 MHz) and Korea (917-923.5 MHz) (IEEE, 2006). There are three different operation modes that can be used on these domains, being the operation mode 1 the mandatory one.

In the modem reception portion, symbol and frequency synchronization is needed, so, many implementation options were studied in order to consider the most suitable in terms of implementation complexity and resources cost. Although those

Tabela 3.2 – MR-FSK modulation and channel parameters for the Worldwide ISM.

PARAMETER	Operating Mode 1	Operating Mode 2	Operating Mode 3
Data Rate (kb/s)	50	150	200
Modulation	Filtered 2FSK	Filtered 2FSK	Filtered 2FSK
Modulation Index	1	0.5	0.5
Channel Spacing (kHz)	200	400	400

algorithms were not implemented by the author, it is important a deep understanding of its functionalities for integration of the overall architecture.

The algorithm used to implement symbol synchronization uses Symmetry Correlation Symbol Synchronization algorithm (DSCSSA), with low-complexity for zero-IF GFSK demodulator, based on the approach showed in (WU et al., 2016a), which uses a known sequence as the preamble (“01010101”), in the begginig of every data frame, to extract symbol synchronization, making use of the symmetry property on the received signal. The extracted value is then used to correct the symbol border and auxiliary signal demodulation. For the frequency synchronization, an approach based on (CHANG; SHIN, 2006) is used, where the frequency offset is estimated by a decision-aided data cancellation, using a phase-lock loop for carrier recovery.

3.2.1 Frequency Shift Keying

Mathematically FSK can be written as:

$$s(t) = A\cos(\omega_c(t)t + \phi_0), \tag{3.2}$$

where

$$\omega_c(t) = k_f \sum_{k=-\infty}^{\infty} a_k g(t - kT_s) + \omega_0, \tag{3.3}$$

where $g(t)$ is the band limiting pulse, ω_0 is a fixed frequency offset, and k_f is a scaling factor, and a_k is the symbol to be modulated (MCCUNE, 2010).

Figura 3.2 shows the equivalence between bit value and signal modulation frequency, during the symbol period. FSK signals, which do exhibit phase continuity across symbol boundaries are called continuous-phase FSK (CPFSK) (MCCUNE, 2010). Figura 3.2 is an example of CPFSK signal.

Orthogonality is another important characteristic, signals to be orthogonal must be uncorrelated over a symbol interval (SKLAR, 2001)

$$\int_0^{T_b} s_1(t) \cdot s_2(t)dt = 0, \tag{3.4}$$

the symbol tones s_1 and s_2 in (3.4) will be

$$s_1 = \cos(2\pi f_1 t)rect(t/T),\ s_2 = \cos(2\pi f_2 t)rect(t/T).$$

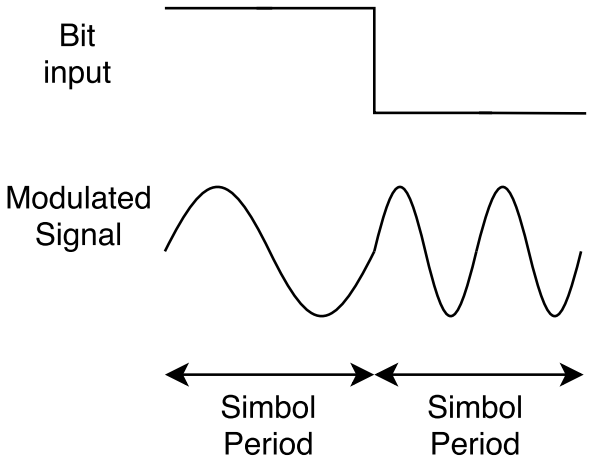


Figura 3.2 – FSK modulation.

Orthogonal FSK signals must meet the criterion set forth in Equation 3.4, which establishes that tones separation must be a multiple of $1/T$, where T is symbol time (SKLAR, 2001).

Very often, FSK modulation takes into consideration the modulation index h, which is a descriptor relating the modulation bandwidth with the symbol rate,

$$h = 2\left(\frac{\Delta f}{f_s}\right). \tag{3.5}$$

It is no surprise then, that the power spectral density of FSK signals varies widely with modulation index. Figura 3.3 shows two examples of FSK spectrum, using a modulation index of 0.5 and 1. It can be seen that signal bandwidth increases with the single variation of the modulation index.

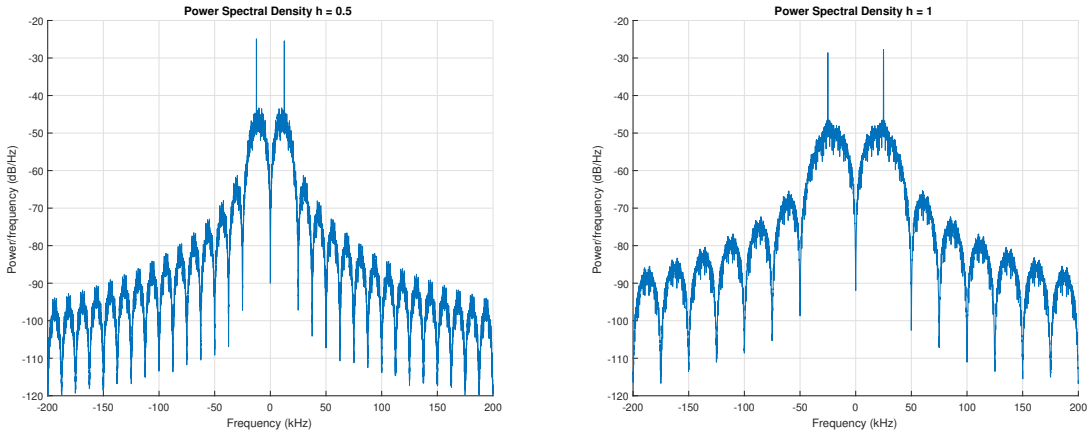


Figura 3.3 – h-influence in the FSK spectrum for h = 0.5 and h = 1.

Frequency separation is another parameter to be set in the FSK modulation, but there is a confusion relating that topic. From the analog FM definition, frequency separation is the tone deviation from carrier frequency, center of the FM signal. However,

many authors prefer to consider spacing between tone frequencies as the frequency separation (MCCUNE, 2010). For 2 FSK, the standard specifies $f_{\text{separation}} = 2\Delta f$ as can be seen in Figura 3.4, where f_sep is $f_{\text{separation}}$ and delta_f is Δf.

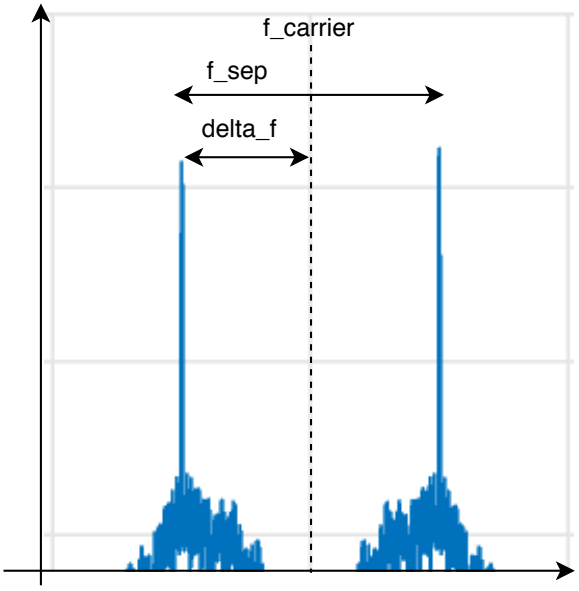


Figura 3.4 – FSK tone separation and frequency delta.

3.2.2 Gaussian Frequency Shift Keying

Also known as filtered FSK, GSK signals are FSK signal filtered by Gaussian lowpass filter and can be mathematically expressed by Equation 3.6 (MUNIR; OLSEN, 2001):

$$s(t) = cos(2\pi f_c t + 2\pi h \int_{-\infty}^{t} \sum_{n=0}^{N} [I_n \otimes g(t - nT)]dt + \phi_0), \tag{3.6}$$

where $g(t)$ is the product of Gaussian pulse convoluted with the rectangular input signal I_n, which represents the data bit at the instant nT of time, T is the bit duration in seconds, h is the modulation index, already explained in Section 3.2, f_c is the carrier frequency and ϕ_0 is an arbitrary phase.

The lowpass Gaussian filter has impulse response described by equation 3.7 (MCCUNE, 2010):

$$h(t) = BT\sqrt{\frac{2\pi}{\ln 2}} e^{-(\frac{2}{\ln 2}(\pi BT\, t))^2}, \tag{3.7}$$

where BT is a scaling factor to set filter bandwidth. Figura 3.6 show the filter behavior in time domain, for different values of BT. It can be observed that the filter has a Gaussian shape, as expected, and it gets larger with the decrease of BT. In this work, BT can assume a value of 0.5 or 1, depending on a modulation parameter defined by the standard.

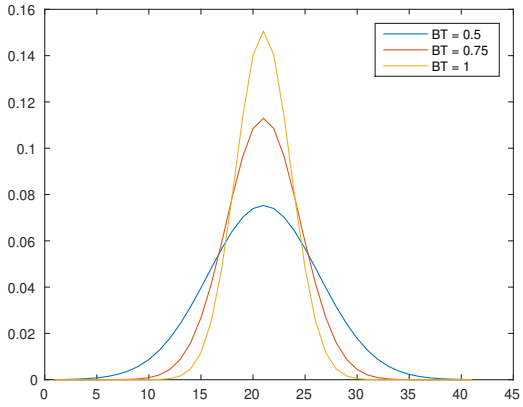
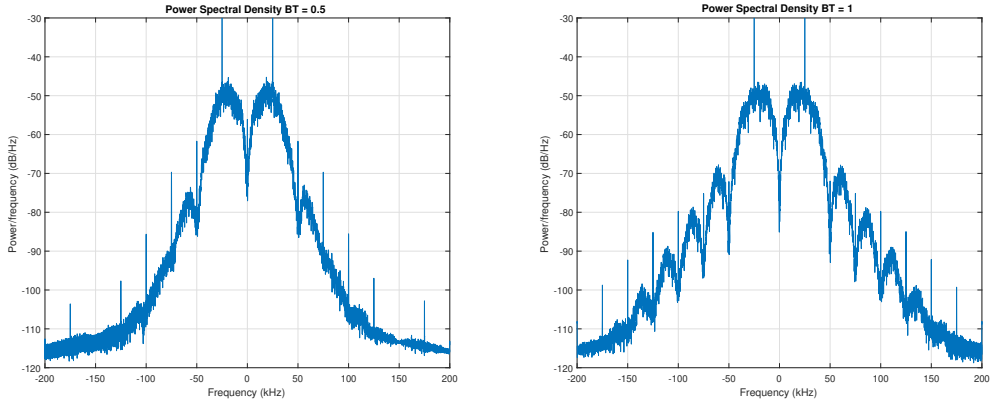


Figura 3.5 – BT influence in the Gaussian filter.

The lowpass filter approach is used in order to narrow the transmitted spectrum and therefore GFSK has more spectrum efficiency in comparison with FSK modulation at the cost of an increased Bit Error Rate (BER) (RAPPAPORT, 1996). A Gaussian filter is used because of the well-behaved time-domain response (MUNIR; OLSEN, 2001).



(a) (b)

Figura 3.6 – BT influence in the GFSK spectrum.

Figura 3.6 shows the BT effect over the GFSK modulated signal, in frequency-domain. Gaussian Filters with smaller bandwidths cause faster spectral roll-offs, that is the case of Figura 3.6(a), compared with Figura 3.6(b), but, as the relative filter bandwidth is lowered, more and more ISI (Inter-Symbol Interference) is imparted to the waveform (MUNIR; OLSEN, 2001).

4 MR-FSK MODELING

This chapter will cover the functionality of each data and signal processing block, implemented as Matalab functions, which one will have a brief explanation about implementation. Hardware implementation will only be addressed in Chapter 5. It is divided into Section 4.1 covering the transmitter portion of MR-FSK modem (modulator) and Section 4.2 covering the reception part (demodulator).

4.1 MR-FSK Modulator Architecture

This section focus on modulator implementation, each subsection here presented corresponds to a block in Figura 4.1. Concatenation blocks did not need implementation, since Matlab functions were used.

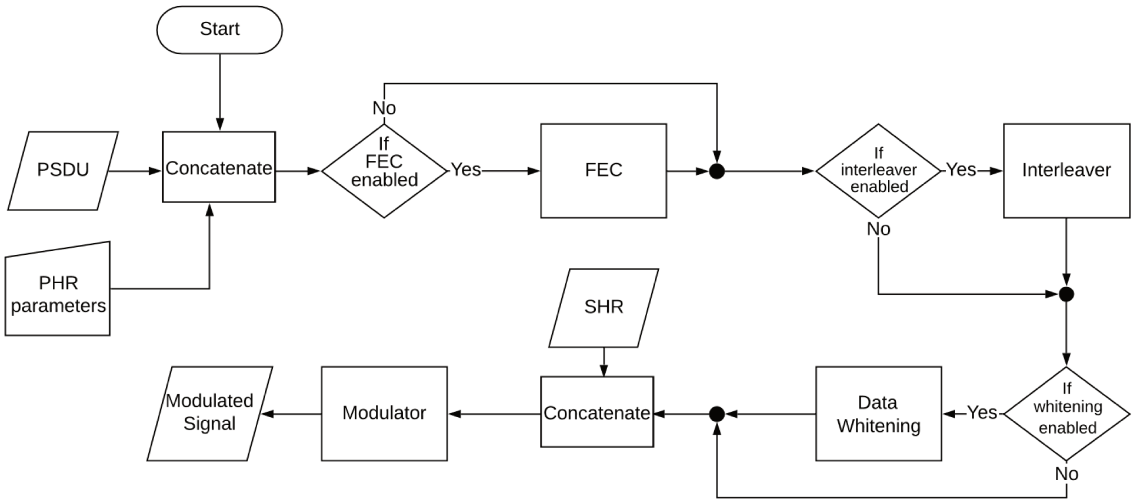


Figura 4.1 – Flowchart of MR-FSK transmitter model.

By receiving a start signal, the system creates the protocol frame. The basic MR-FSK PHY frame structure - PHY Protocol Data Unit (PPDU), is shown in Table 4.1. First, PHR (PHY Header) and PSDU (PHY Service Data Unit) are concatenated. PSDU is the frame payload loaded from a text file. PHR parameters are set before the beginning of the simulation.

Tabela 4.1 – MR-FSK PPDU containing SHR, PHR and PSDU.

Preamble	SFD	PHY Header	PHY Payload
SHR		PHR	PSDU

With PSDU and PHR concatenated, the use of FEC for that frame is checked and the data processing is applied accordingly. The same process is done for interleaving and data whitening, except, whitening is only applied to PSDU. After data processing is done, SHR (synchronization header) is concatenated and the complete frame is then modulated, resulting in the modulated signal sent to a file. In the items bellow, each of this process are further detailed.

4.1.1 PHR

All packets in MR-FSK PHY must have a Physical Header (PHR) carrying the basic information for receiver configuration, so the PSDU data can be retrieved upon demodulation and delivered to the MAC layer. Table 4.1 shows the PPDU with the PHR to be concatenated.

The PHR Generator assembles the PHR field with the need attributes. The first bit corresponds to Mode Switch field, which is responsible for making the transition to other PHY modes that modem may support. For PHR shown in Table 4.2, Mode Switch shall be set to zero, indicating that data rate and modulation scheme shall not be changed. The case where Mode Switch is set to one is not covered in this work.

The second field is two bits long, reserved for future purpose. It is followed by the Frame Check Sequence (FCS), which corresponds to the PHY PIB attribute *macFCStype* specifies the tail length for the MAC packet inserted after the MAC payload (MPDU).

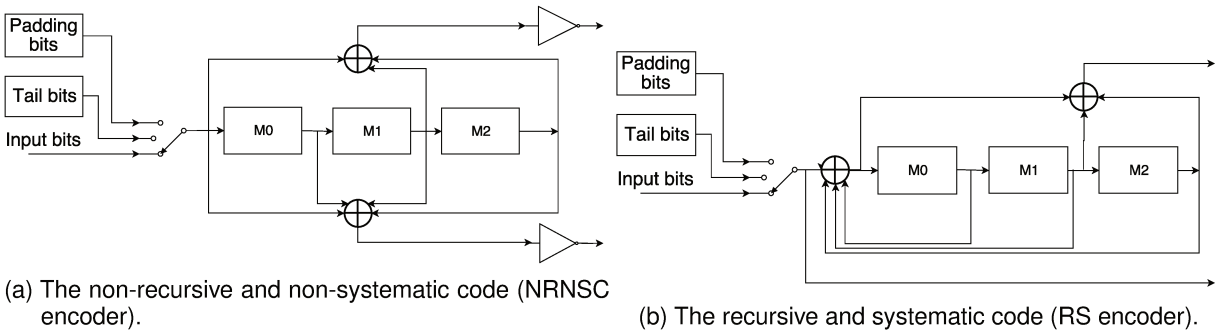
Data Whitening field (DW) indicates whether data whitening of the PSDU is used upon transmission, according to the PHY PIB attribute *phyFSKscramblePSDU*. Frame Length field (L10–L0), is 11 bits long and specifies the total number of octets in PSDU.

Tabela 4.2 – PHR without mode switch structure.

Bit index	0	1-2	3	4	5-15
Field Name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length

4.1.2 FEC Encoder

Forward Error Correction (FEC) is a technique used to control errors in data transmission. It is optional in MR-FSK, which is enabled by the parameter *phyFSK-FECEnabled* from PIB attributes table. The FEC encoder can apply a Recursive and Systematic Code (RSC) or a Non-Recursive and Non-Systematic Code (NRNSC), depending on *phyFSKFECScheme* attribute. The process results in two outputs, u^0 and u^1.



(a) The non-recursive and non-systematic code (NRNSC encoder).

(b) The recursive and systematic code (RS encoder).

Figura 4.2 – FEC encoder schemes for MR-FSK.

Both coding schemes are X by three memory states (M0, M1 and M2) and XOR operator. The NRNSC is a convolutional encoder, illustrated in Figura 4.2(a), with negated outputs and masks as follow: 1011 and 1111. The first and second outputs are produced by the following equation:

$$u_{\text{i}}^{0} = \overline{b_{\text{i}} \oplus b_{\text{i-2}} \oplus b_{\text{i-3}}},$$

$$u_{\text{i}}^{1} = \overline{b_{\text{i}} \oplus b_{\text{i-2}} \oplus b_{\text{i-1}} \oplus b_{\text{i-3}}}.$$

The RSC is a Recursive and Systematic encoder, described in the Figura 4.2b. The first and second output bits of encoder have the following equation:

$$u_{\text{i}}^{1} = b_{\text{i}} \oplus b_{\text{i-1}} \oplus b_{\text{i-2}} \oplus b_{\text{i-3}} \oplus b_{\text{i-2}} \oplus b_{\text{i-3}},$$

$$u_{\text{i}}^{0} = b_{\text{i}}.$$

After coding PHR and PSDU bits, as a single block of code, three tail bits are inserted. The sequence value differs, depending on coding scheme, as shown in Table 4.3.

Tabela 4.3 – Tail bits pattern for the RSC and NRNSC encoders.

Memory State	RSC	NRNSC
000	000	000
001	100	000
010	110	000
011	010	000
100	111	000
101	011	000
110	001	000
111	101	000

Padding sequence should be inserted after tail bits only when the interleaver is used. This process is required to fill up the last interleaver buffer completely. Length of the bit sequence is computed as follows:

Tabela 4.4 – Padding patterns when $(L_{\text{PHR}} + L_{\text{PSDU}})/8$ is odd (5-bit) or even (13-bit).

	5-bit	13-bit
Padding Pattern	01011	0101100001011

$L_{\text{PAD}} = 5$, when $\frac{L_{\text{PHR}}+L_{\text{PSDU}}}{8}$ is odd,

$L_{\text{PAD}} = 13$, when $\frac{L_{\text{PHR}}+L_{\text{PSDU}}}{8}$ is even.

Padding bits patters should not contain a long series of '1's or '0's. Table 4.4 shows the two possible sequences used in this encoder. The padding bits are inserted in the encoder.

4.1.3 Interleaver

Wireless communication channels errors typically occur in bursts and there is a limit to the number of sequential errors in a code word that can be handled by an Error Correcting Code algorithm (ANDREWS; HEEGARD; KOZEN, 1997). The interleaver block is used to improve performance of forward error correcting codes, creating a more uniform distribution of errors.

The interleaver receives PHR and PSDU field encoded by FEC Encoder block and performs a permutation of code-symbols, where each permuted element contains exactly one code-symbol (two bits). Interleaver block is always enabled when FEC Encoder uses NRNSC coding and may also be applied with RSC when the PIB attribute *phyFSKFECInterleaverRSC* is set to '1'. This data processing shall not be applied when FEC Encoder is not enabled.

4.1.4 Whitener

Data Whitening is intended to randomize the data payload, so it does not present a long sequence of bits with the same value. This process makes transmission more efficient, once the power distribution will be spread over the bandwidth. The Whitener receives PSDU field only, and applies a XOR operation with a Pseudo Random Binary Sequence (PRBS). A PRBS Generator is basically a Linear Feedback Shift Register (LFSR), illustrated in Figura 4.3, with a specific configuration. In MR-FSK, the specific configuration corresponds to the generator polynomial $X^9 + X^4 + 1$, with seed 111111111.

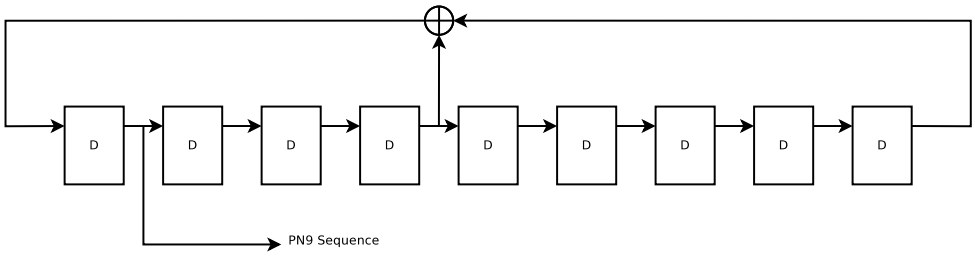


Figura 4.3 – Linear Feedback Shift Register for generating the PRBS.

4.1.5 SHR

A synchronization Header (SHR) is needed to assist the packet acquisition. This header, as can be seen in Table 4.1, it is composed by a preamble field and a Start-of-Frame Delimiter (SFD). The second one indicates if the system has FEC (Forward Error Correction) enabled or not.

The preamble is the first bit sequence to be generated. All possible preamble bit sequence are defined in Table 4.5. It will be repeated according to the variable *phyFSKPreambleLength*, a parameter of the PIB table defined in (IEEE, 2006), which is an integer in range 4 - 1000:

Tabela 4.5 – The preamble frame should contain multiples of the equivalent sequence, depending on the FSK mode used.

	2FSK mode	**4FSK mode**
Preamble sequence	0101 0101	0111 0111 0111

For SFD field, the generated sequence depends on *phyFSKFECEnabled* and *phyMRFSKSFD* attribute which is binary and change the SFD according to Tables 4.6 and 4.7.

Tabela 4.6 – MR-FSK PHY SFD values for 2-level modulation.

	SFD for phyFSKFEC = 1	SFD for phyFSKFEC = 0
phyMRFSKSFD = 0	0110 1111 0100 1110	1001 0000 0100 1110
phyMRFSKSFD = 1	0110 0011 0010 1101	0111 1010 0000 1110

Tabela 4.7 – MR-FSK PHY SFD values for 4-level modulation.

	SFD for phyFSKFEC = 1	SFD for phyFSKFEC = 0
phySFD=0	0111 1101 1111 1111 0111 0101 1111 1101	1101 0111 0101 0101 0111 0101 1111 1101
phySFD=1	0111 1101 0101 1111 0101 1101 1111 0111	0111 1111 1101 1101 0101 0101 1111 1101

4.1.6 FSK/GFSK Modulator

After all digital data process is performed, the signal needs to be modulated. This block converts processed bits into FSK or GFK modulation in baseband, as the RF

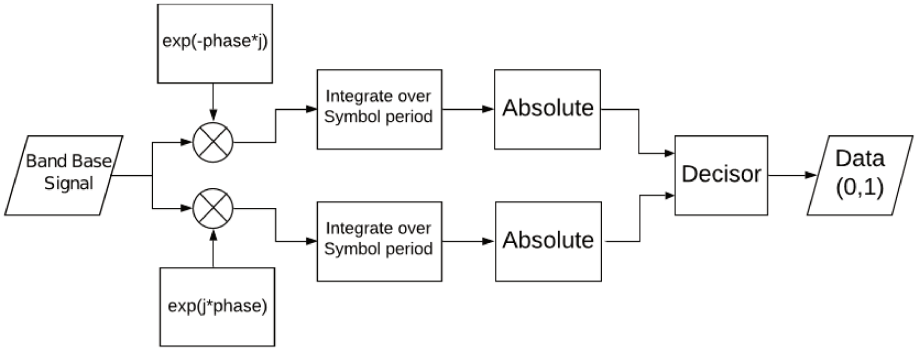


Figura 4.4 – FSK baseband modulator.

transmission is not covered in this work. According to (3.3), FSK modulator accumulates the bits, maps to a frequency deviation, which is input of a phase generator, followed by cosine and sine functions. For a baseband 2-level FSK, there will be two frequencies, one representing the bit '0' and the other one representing bit '1'. These two frequencies only differ by the sign and the phase step is determined in the following way:

$$\phi_0 = 2\,\pi f_{\text{dev}},$$

$$\phi_1 = -2\,\pi f_{\text{dev}},$$

where f_{dev} was defined in Equation 3.1. In that way, for a data rate (f_{data}) of 50 kb/s and modulation index of 1, as the example in Table 3.2, operation mode 1, there will be two frequencies tones in the spectrum, at -25 kHz and 25 kHz. Figura 4.5 shows the spectrum for the FSK modulation using Matlab function *fskmod*, for this example.

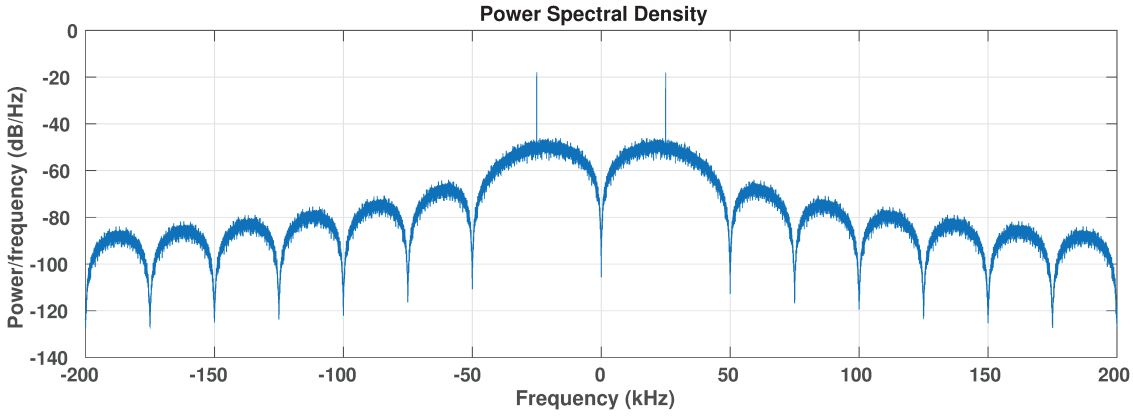


Figura 4.5 – FSK spectrum for frequency deviation of 25 kHz.

GFSK modulation is similar to FSK, but with addition of a Gaussian filter. For implementation, bits are mapped in rectangle pulses as the input for the Gaussian filter, designed using the Matlab function *gaussfir*, with the BT parameter defined by PHY attribute *FSKBT* that can have the value of 0.5 or 1. The number of symbols parameter was defined to be '1' and the samples per symbol (*sps*) parameter is given by the

following equation: $sps = F_s/f_{data}$, where F_s is the sampling frequency, set to 1MHz to initial simulations.

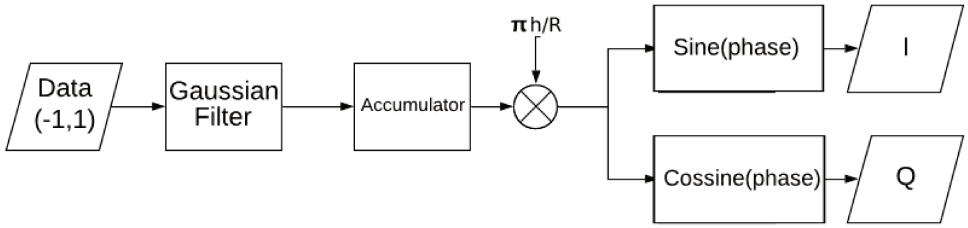


Figura 4.6 – GFSK Modulator.

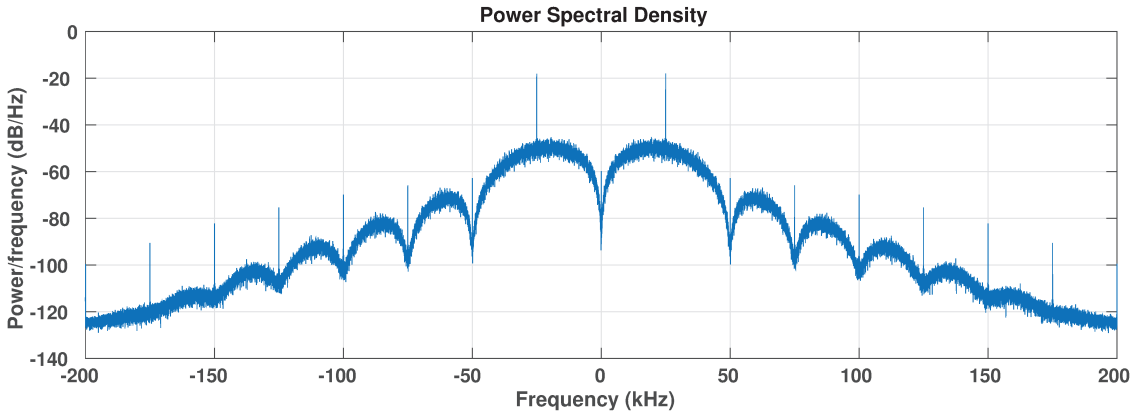


Figura 4.7 – GFSK spectrum for frequency deviation of 25 kHz.

As shown in Figura 4.6, Gaussian filter output is accumulated, multiplied by $h\pi/R$, where R is the bit rate in symbol per second. This signal feeds a cosine and sine blocks in quadrature modulation, giving I and Q signals, which are sent to the RF chain. GFSK frequency spectrum for the frequency from Table 3.2, equivalent to Worldwide ISM (2400-2483.5 MHz), operation mode 1, with $f_{dev} = 25$ kHz, is shown in Figura 4.7.

4.2 MR-FSK Demodulator Architecture

This subsection describes the reception part of the MR-FSK modem and each block in Figura 4.8 will be described in a corresponding item. For Matlab simulation, signal demodulation starts by reading the modulated signal file from transmission. Once the data bits are retrieved, frame header (SHR) is detected, delimiting frame starting point and extracting SHR parameters need for internal control, like FEC and interleaving enabling parameters. Once PHR and PSDU are extracted, the first one bypasses data whitening and is processed by the remaining enabled data processing blocks. Once PHR is parsed, PSDU can continue on the data path, passing through data whitening, if applicable, FEC and interleaver. At the end of receiving process, the PSDU is extracted and written in a file for further use.

4.2.1 Demodulator

This work makes use of two approaches for the demodulation of GFSK and FSK signals, one of them at intermediate frequency (IF) and the second one at baseband (BB).

Both GFSK and FSK modulations have a similar spectrum, as shown in Figura 4.5 and 4.7, with distinct frequency tones, for each symbol modulated. Therefore, classical demodulation process for the FSK can also be applied to GFSK demodulation. Figura 4.9 shows a schematic for asynchronous demodulation with filters, for a 2-level modulation scheme. In this example, there are two frequencies: f_0 and f_1, correspondent to bit '0' and bit '1', respectively. For an IF demodulation, the frequencies will assume the value: $f_0 = f_c - f_{\text{dev}}$ and $f_0 = f_c + f_{\text{dev}}$, where f_c is the frequency carrier to intermediate frequency.

First, two distinct bandpass filters are applied, to separate the distinct frequencies in two different signals. Matlab implementation uses IIR filter for bandpass filter design with 10 coefficients and cut-off frequencies: left_cutoff_frequency = $f_0 - 0.5f_{\text{dev}}$ and right_cutoff_frequency = $f_0 + 0.5f_{\text{dev}}$. The same parameters are calculated for f_1. The output for those bandpass filters can be seen in Figura 4.10a in different colors and lines. It can be observed that when one output is high in magnitude, the other one has a minimum response, as the filters are designed to detect one bit being received and cut out the other one.

Each signal is then input in an envelope detection, implemented in a lowpass filter, which output can be seen in Figura 4.10b, resulting in the cancellation of higher frequencies, when comparing with the filter input in Figura 4.10a. That output absolute value is computed, resulting in a plateau in the branch correspondent to the symbol transmitted in that symbol period. The down sampling of that can be seen if Figura 4.10c.

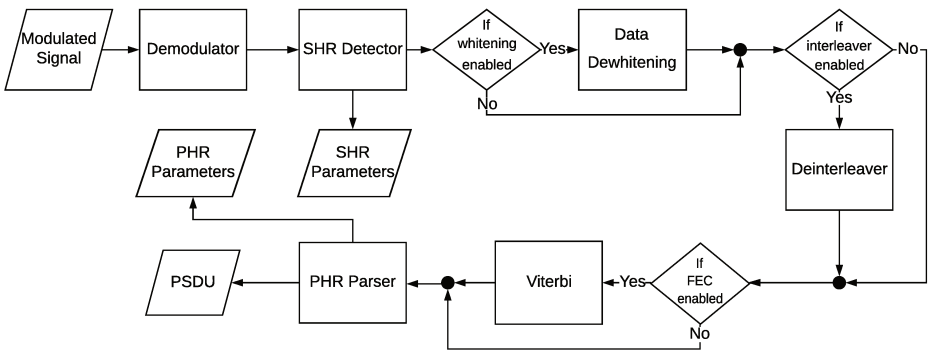


Figura 4.8 – Flowchart of MR-FSK model integration.

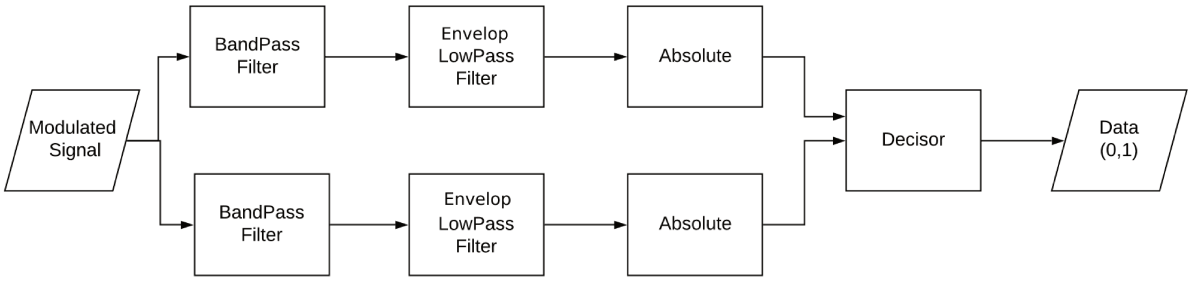


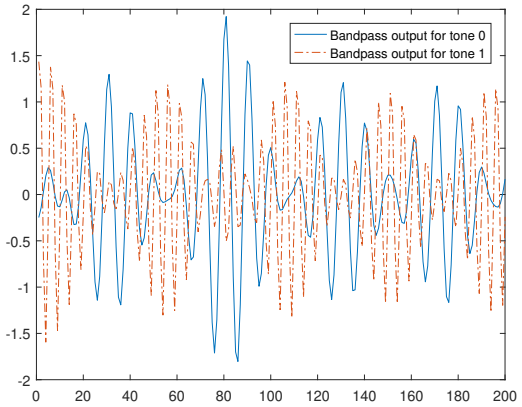
Figura 4.9 – Filter based demodulation in IF, used for GFSK and FSK demodulation.

Based on that, symbol decision is a simple magnitude comparison between the two values each one corresponding to a symbol.

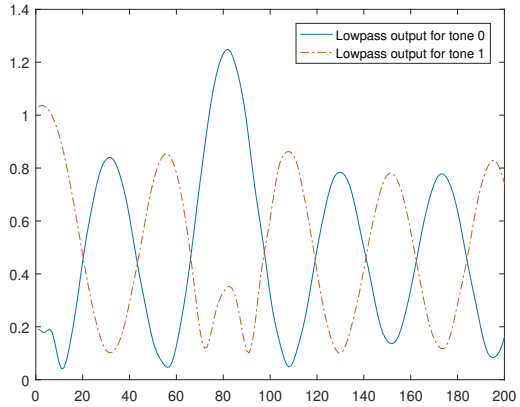
Other two demodulations approaches were chosen for GFSK and FSK demodulation, in baseband. One approach for bandbase demodulation of FSK signals is correlation-based as illustrated in Figure 4.11. The correspondent signals are shown in Figures 4.12a and 4.12b, respectively, real time-domain, with the input data bit for reference, and respective waveforms for imaginary part of the FSK modulated signal. As it was explained previously, the imaginary part, corresponding to signal phase, is the only variant between symbols. Figures 4.14b and 4.14c shows the same information, but for a GFSK signal.

A correlation demodulation approach was used to FSK demodulation, which consists in reproducing the FSK pulses, and correlating with the received signal. The reference FSK pulses can be seen in Figures 4.12c and 4.12d, for tone 1 and tone 0, respectively. When a tone is correlated with itself, the output results in a constant value of 0 for the real part and 1 for the imaginary part. When it is not the case, a periodic signal with zero mean can be observed. That result can be observed in Figure 4.12e and 4.12f. So, the bit decision is based on comparing the absolute mean value of correlation result from both reference pulses, during symbol period. The signal corresponded to the symbol being transmitted would assume a value of one, and the other signal a value of zero. Figura 4.12g shows the final result for that example. It can be seen, that the first two bits matches tone 1 (depicted by Figura 4.12c), correspondent to bit 0, followed by one bit 1 and one bit 0, which matches with the input data that can be seen in Figura 4.10a.

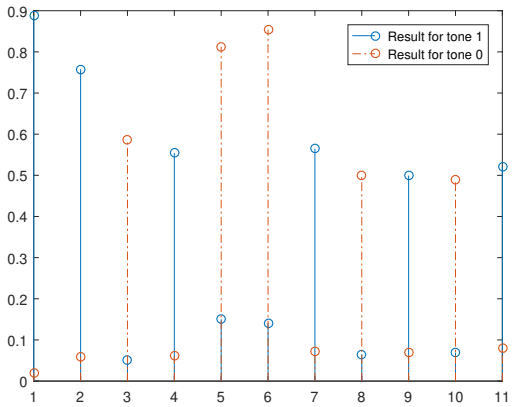
GFSK synchronous demodulation retrieves phase information from the received signal. Due to Gaussian filtering, GFSK signal has a smoother phase variation. Hence, phase derivation during symbol period decides which bit is being transmitted. If it has a positive value, the decoded symbol has a value of ’1’, or ’0’ otherwise.



(a) Bandpass Filter output for a FSK input, in time.



(b) Lowpass Filter output for a FSK input, in time.



(c) Decisor input in symbol time.

Figura 4.10 – Filter based demodulation steps for a FSK input.

Figura 4.14a shows the effect of the Gaussian filter, applied to the input data, in the modulation. Figures 4.14b and 4.14c represent the GFSK signal modulated in base band, for the input data also highlighted in the same plots, as explained earlier in this section. Figures 4.14d and 4.14e are correspondent to demodulation process. The first one is the output of the actan block, in the diagram of Figura 4.13. This result is the filtered and down sampled, obtaining the plot in Figura 4.14e, in which the decisor block delivers 1 when the value is positive and 0 in contrary case.

4.2.2 SHR Detector

The SHR detector receives data sent by the demodulator block, compares each bit with a preamble sequence, presented in Table 4.5. Once it gets a match, the following bits could be another preamble repetition or a SFD. Both sequences are checked, until a SFD sequence is detected, witch indicates the beginning of a PHR. The SFD values for both FSK modes are presented in Tables 4.6 and 4.7. The detected SFD

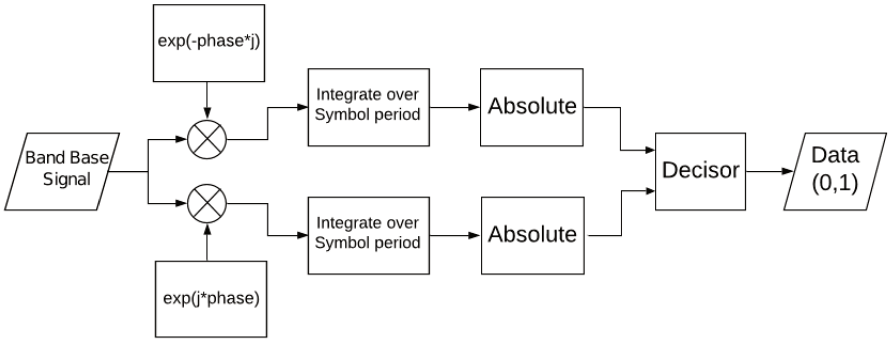


Figura 4.11 – Correlation based demodulation for baseband FSK.

indicates whether the frame is FEC coded or not, which enables FEC decoder block.

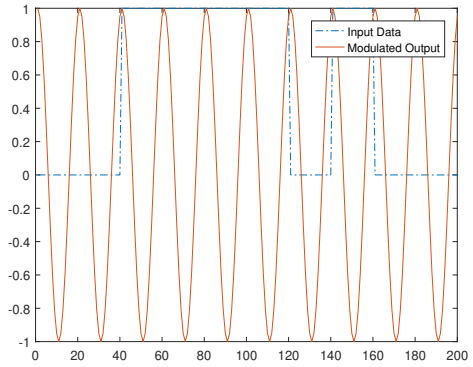
4.2.3 Deinterleaver

The deinterleaving process is done to retrieve data from the interleaving block. In order to achieve that, the same bits permutation in transmitter is done here in the interleaving block.

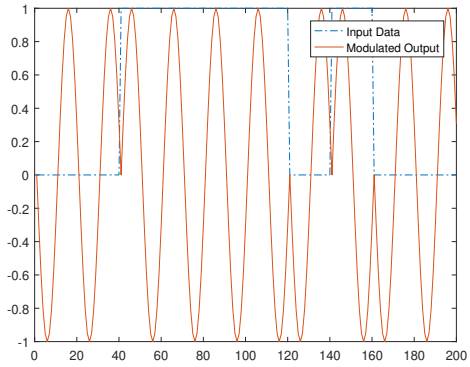
4.2.4 Viterbi

Viterbi is a classical maximum-likelihood decoding algorithm for convolutional codes (FORNEY, 1973). Flexibility and reliability are key aspects for chosen Viterbi algorithm. In addition due to the fact that the block was already implemented and validated in ASIC, only requiring modifications regarding trellis parameters. The Viterbi function coded in Matlab, is able to decode both NRNS (Non-Recursive and Non-Systematic) and RSC (Recursive and Systematic) coding, since the equivalent trellis is provided. Each trellis node corresponds to a state in a given moment of time, and branches are transitions between states, caused by data input. An important characteristic that makes decoding possible is that, for every state sequence, there is only one trellis path (FORNEY, 1973).

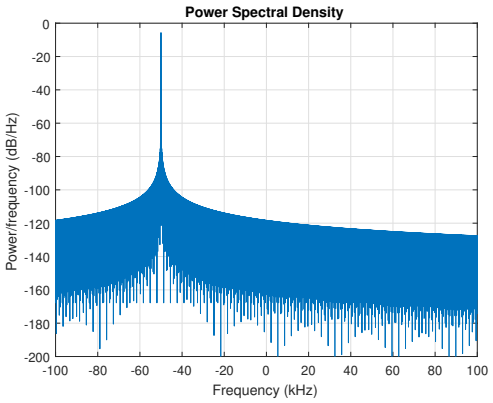
As a key to decoding, trellis can be obtained from the encoder state machine, where each state corresponds to the memory state in the encoder, changed due to the given bit input. Given a memory state and input, the transition costs are calculated, by the difference of convolutional coder output at a given trellis state and the input. Afterwards the Viterbi algorithm calculates the minimum distance path, for a sequence of bits. In that way, wrong bits that corresponds to a non-existent transition are corrected.



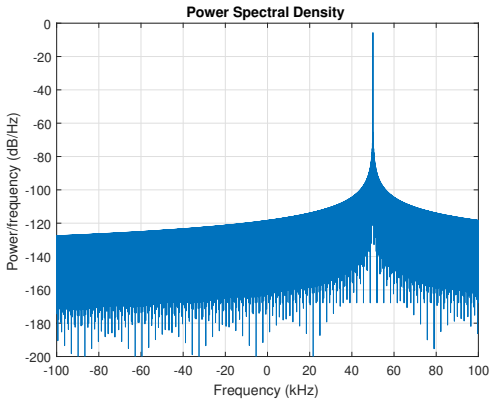
(a) Real part of FSK modulated signal, for a given data input.



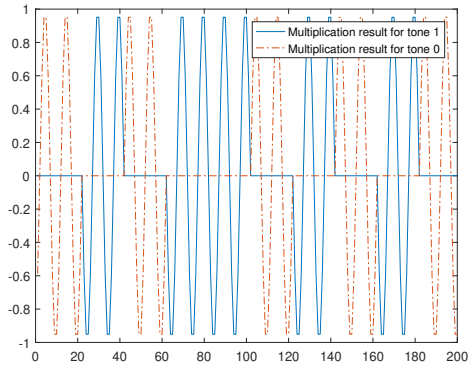
(b) Imaginary part of FSK modulated signal, for a given data input.



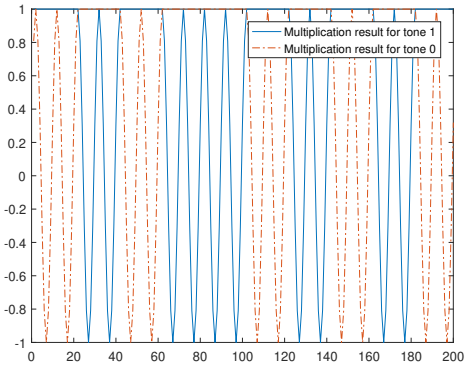
(c) FSK reference signal in frequency domain, correspondent to the bit 0.



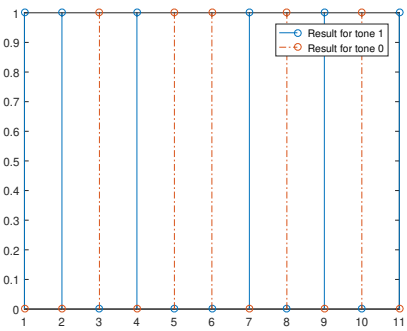
(d) FSK reference signal in frequency domain, correspondent to the bit 1.



(e) Real part of the correlation output.



(f) Imaginary part of the correlation output.



(g) Decisor block input.

Figura 4.12 – Correlation based demodulation steps for FSK.

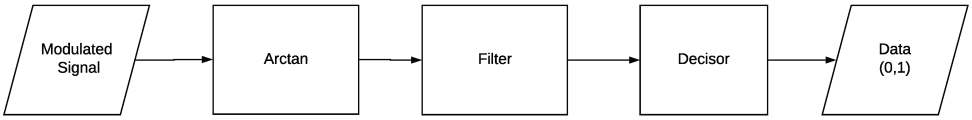


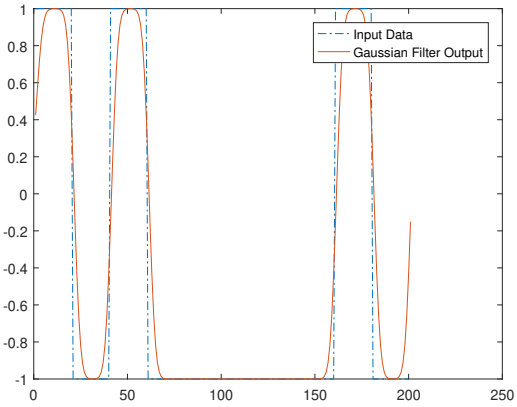
Figura 4.13 – GFSK baseband demodulation based on phase variation detection.

4.2.5 Dewhitener

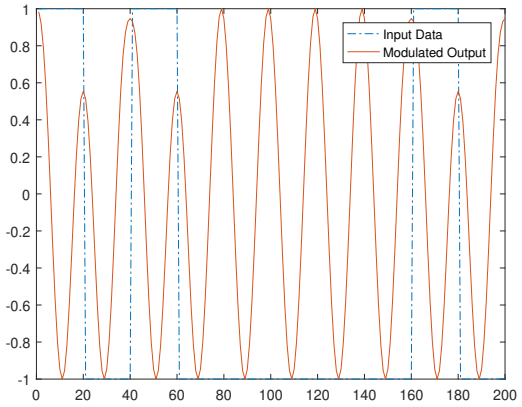
When data whitening is applied in the transmission portion, dewhitener process must be applied to retrieve PSDU data upon reception. The process is the same done by the whitener: an Exclusive OR (XOR) between the PRBS and PSDU field. Since PRBS generator will give same output if the same seed in used, which is the case, the XOR operation will return the original data.

4.2.6 PHR Parser

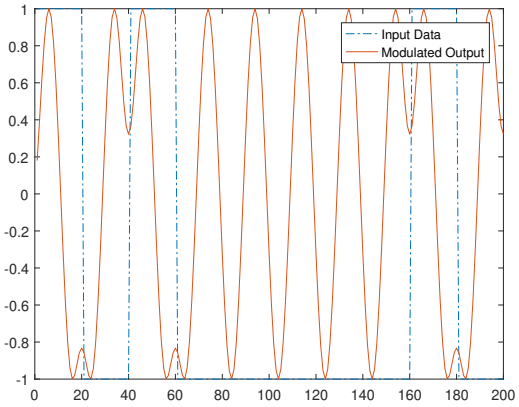
PHR parser receives PHY header and, having a previously knowledge of the PHR format, shown in Table 4.2, the block separates each multi-bit field in an output, to be used by other blocks, or to be passed to MAC. Data whitening bit, for instance, enables DE whitening. Internal integration control and other blocks also use frame length information.



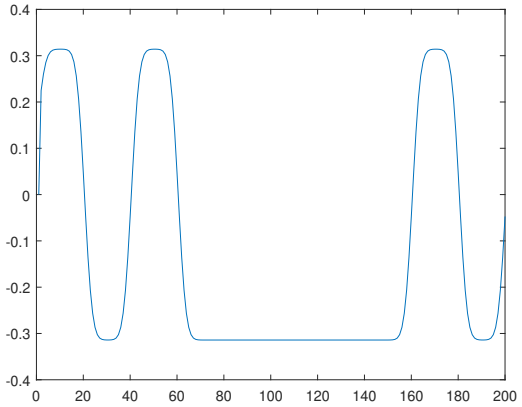
(a) Gaussian filter output for the given data input.



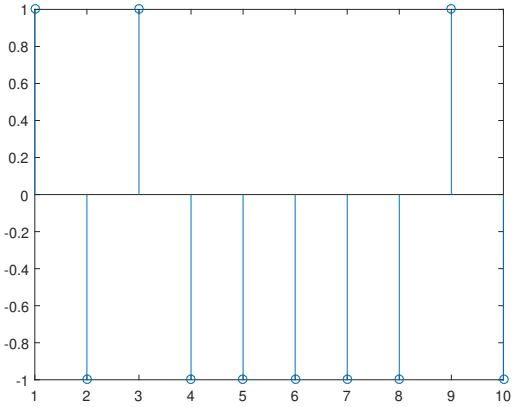
(b) Real part of GFSK modulated signal.



(c) Imaginary part of GFSK modulated signal.



(d) Arctan output in GFSK demodulation process.



(e) Decisor block input.

Figura 4.14 – Phase variation detection based demodulation steps for GFSK.

5 MR-FSK DESIGN

This chapter will cover VHDL design, passing through blocks used in this implementation context, such as block communication protocols, validation and test blocks. Other blocks stipulated by the standard will be detailed with block diagrams to illustrate implementation.

Once the blocks models were tested, digital circuit design aiming ASIC was the next step. For that, the overall system architecture must be taken into account. An overall architecture of IEEE 802.15.4g MR-FSK system is detailed in Figura 5.1. A microprocessor is needed to implement Medium Access Control (MAC) and Smart Metering Utility network (SUN) application software, altogether with an external RF for wireless communication. Inside IEEE 802.15.4g PHYs block, all the three alternative PHYs can be implemented: MR-FSK (detailed on this work), MR-OFDM or MR-QPSK.

The MR-FSK modem, inside IEEE 802.15.4g PHYs block, consists in an interface for the PHY register and MAC layer, MR-FSK modulator (FSK TX), MR-FSK demodulator (FSK RX), and an interface with the RF transceiver, as depicted in Figura 5.2. MAC interface consists of digital implementation of SPI and I2C protocol, for data payload and configuration interface, respectively. RF interface is responsible to take the signal from baseband to RF.

Some of PHY registers are PIB (personal area network information base) attributes, as the ones in Table 3.1, defined by the standard, introduced in Chapter 3. Those registers can only change value when no frame is being transmitted. A controller module is needed to switch between modulator and demodulator, as well as control the RF interface. Besides the overall structure, other new variables are introduced in digital circuit design, related to word quantization, protocol communication between blocks and clock synchronization.

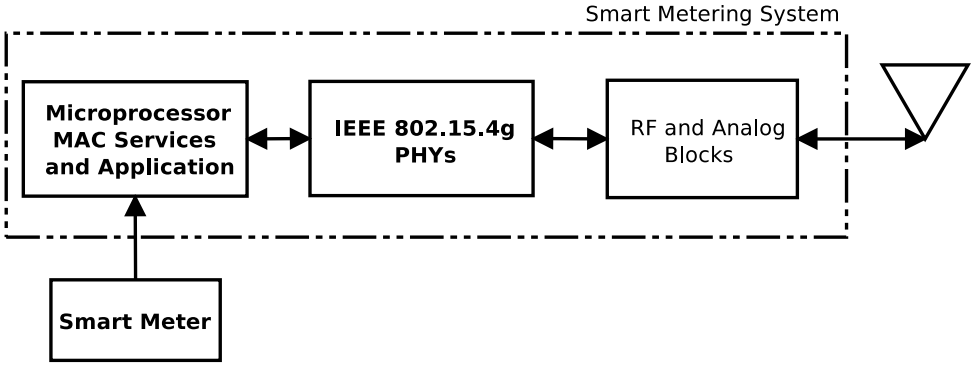


Figura 5.1 – IEEE802.14.4g overall architecture.

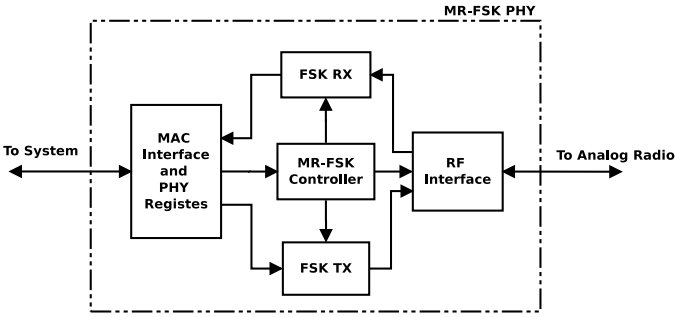


Figura 5.2 – MR-FSK overall Architecture.

Figures 5.3 and 5.4 are the MR-FSK integration equivalence to the processing proposed by the standard, shown in Figura 3.1, which are expanded in Figures 4.1 and 4.8. For hardware implementation, multiplexers and demultiplexers are used for bypass blocks that are not enabled, and FIFOs are used when there is the need to buffer data. In the modulator, FIFO is used before the signal modulator block, to assure data throughput to it, whereas the demodulator needs a valid input at every clock. In the demodulator, FIFO is used after SHR detection for control purpose, holding PSDU until PHR is parsed, so PSDU data path is completely defined.

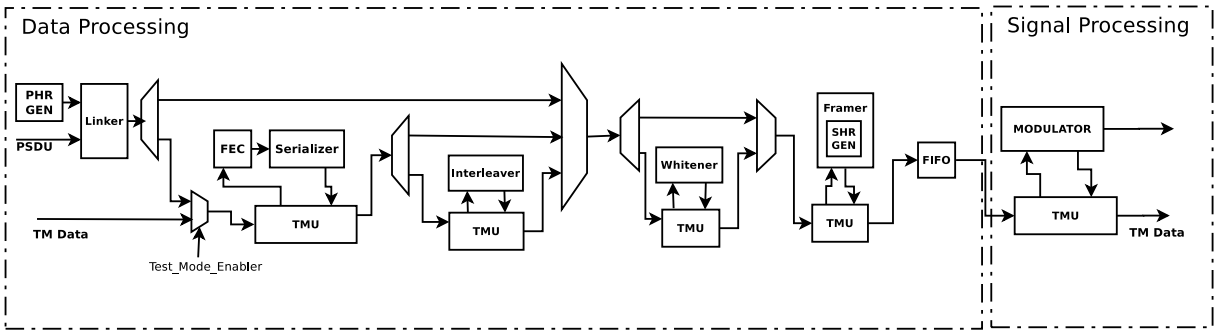


Figura 5.3 – MR-FSK PHY modulator architecture.

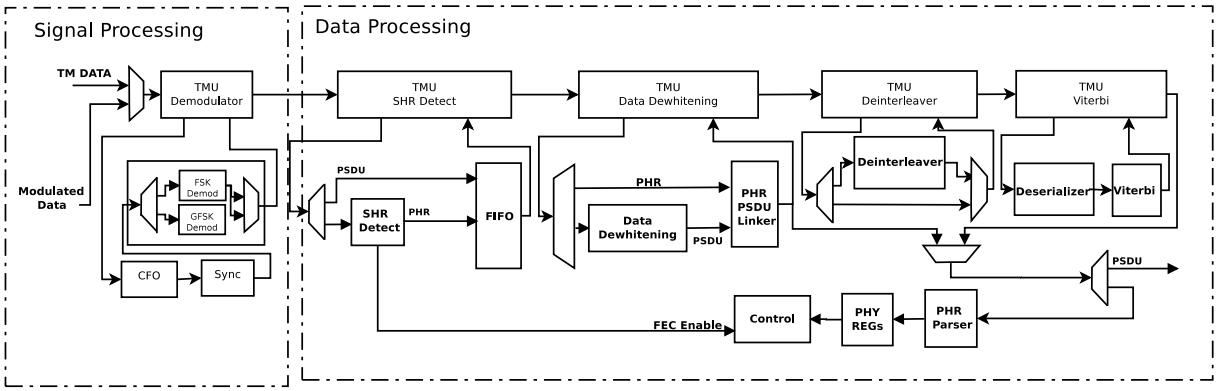


Figura 5.4 – MR-FSK PHY demodulator architecture.

This chapter will detail each block shown in Figures 5.3 and 5.4, focusing in HDL implementation using VHDL, as well as blocks integration, describing the data

flow in the MR-FSK modulator (Section 5.3) and MR-FSK demodulation (Section 5.4) integration. Important topics for both parts of the modem, such as communication protocol between blocks, and a module to assist ASIC test, will be approached in Section 5.1 and 5.2, respectively.

5.1 Ready-Valid Protocol

Communication between internal blocks of the modem are an important part of design implementation, because it directly influences system functionality and latency. Among with many protocols that can be used, the one chosen for this work is the Ready-Valid protocol, which has already been used by the author's research group. Protocol basic functionality is to keep low-level out_valid signal while receiving a low ready-signal from the connected block.

All signals for protocol functionality are listed below:

- in_ready: Output port, set to high to indicate that the block will be ready on the next clock cycle for receiving a valid data.
- in_valid: It is an input port, asserted to indicate when the input data in the current clock cycle is valid.
- out_ready: An input port, which value indicates that the following block will be ready to receive data in the next clock cycle.
- out_valid: Output port, set to high when there is a valid data bit in block output, in the current clock cycle.

Figura 5.5 shows an example of read-valid protocol functionality, with the signals explained above and the signal in_data and out_data, which are input and output ports for the communication data. When the block is ready to receive (in_ready high), it receives a valid data (in_valid high) in the next clock cycle. Because of internal functionalities of the block in question for this example, one cycle after it receives a valid input, the block can output a valid data (out_valid high), but only one clock cycle after receiving an out_ready signal.

Other signals can be added to the communication protocol, to assist the system integration control. The ones in use in this work are the *eof* and *sof*, that stands for end of frame and start of frame, respectively. They both are a single bit indicating that the current valid data is the last or first bit from the received or transmitted frame.

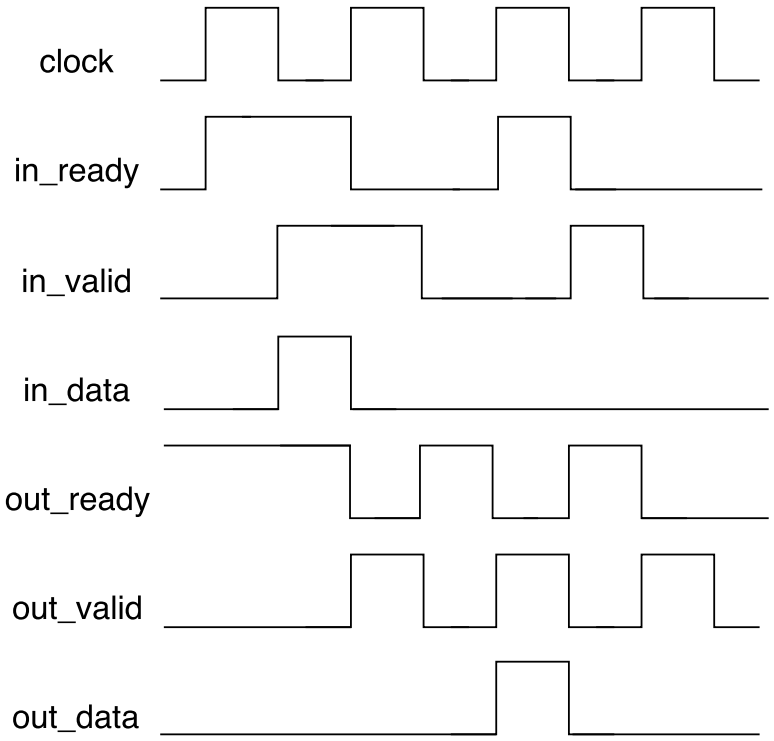


Figura 5.5 – Ready-Valid functional diagram.

5.2 Test Mode Blocks

An important point to be addressed is the testability of hardware implementation. Simulations during development does not assure total functionality due to manufacturing defects. In addition, the possibility of testing individual blocks is a good motivation for testing blocks implementation. As it can be seen in Figures 5.3 and 5.4, each strategic block has a Test Mode Unit block that can achieve the testability by intercepting any data going through the blocks, as it can be seen in Figura 5.6.

When a specific block has the test mode unit enabled, the data will flow from the test mode input/output directly to and from the block being tested. While the remaining blocks, not being tested, would have that data bypassed. With that functionality, data can be bypassed trough all blocks in integration shown in Figures 5.3 and 5.4, but not in the block, or set of blocks to be tested. Test Mode Unit also enables testing of the entire integrated system, but with a controlled data input, instead of data coming from MAC or RF interface. As another testability resource, control signals, specially at the modulator part, can be bypassed to use the value set in the register bank, instead of internal calculated values, that, together conjunction with the Test Mode Unit, can assure the testability of the manufactured chip.

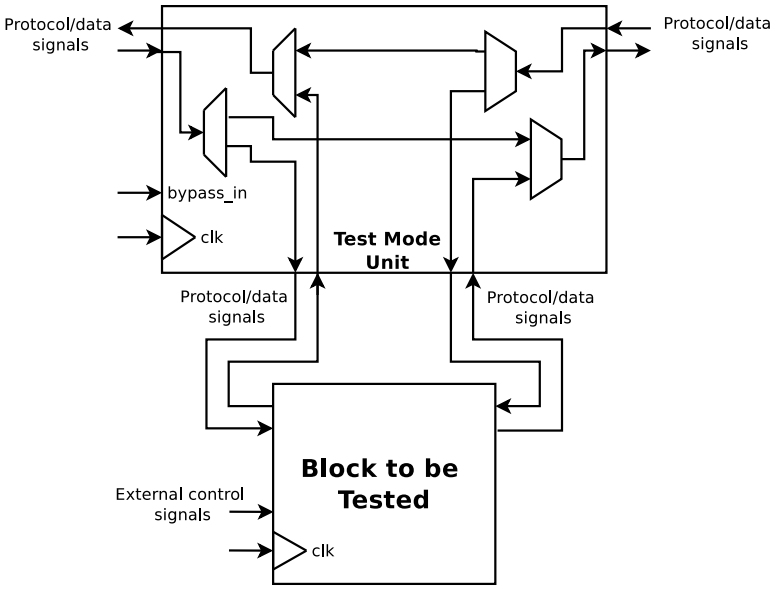


Figura 5.6 – Test Mode block diagram.

5.3 MR-FSK Modulator Architecture

The digital transmitter in Figura 5.3 is enabled when all PHY parameters are valid. The first block to output bits is the Framer block, generating the correct SHR sequence. No data processing needs to be applied for SHR, so it is delivered to a FIFO block, used to guarantee the data rate compliance to the modulator. When the last SHR bit is at block output, the framer block requests bits to the PHY header (PHR) generator that is responsible to serialize all PHY parameters necessary for the packet, as specified in PHR Generator item, in Section 4.1.1. Blocks connections changes, through multiplexers, depending on PHY registers, which will enable non-mandatory data processing blocks.

A linker module, implemented only in VHDL, receives the header and requests PSDU field from MAC. It concatenate PHR and PSDU fields, besides generating start of frame and start of PSDU signals. Considering a transmission where all data processing blocks are enabled, bits from the output of linker block are delivered to FEC Encoder. As depicted in the block diagram shown in Figura 5.7. The coding scheme (RSC or NRNSC) is selected by fec_scheme_in signal. Both have rate of $1/2$, so two parallel outputs are produced for each input. Since all data processing blocks work with serial input, parallel FEC encoder output is sent a serializer block input.

The tail block is enabled immediately after encoding of the PHR and PSDU, and the corresponding tail sequence is inserted. During that time, the encoder block is not ready to receive external valid bits. After tail bits, the control unit checks the need for pad bits, that must be used whenever interleaver is enabled, repeating the same process used for tail bits.

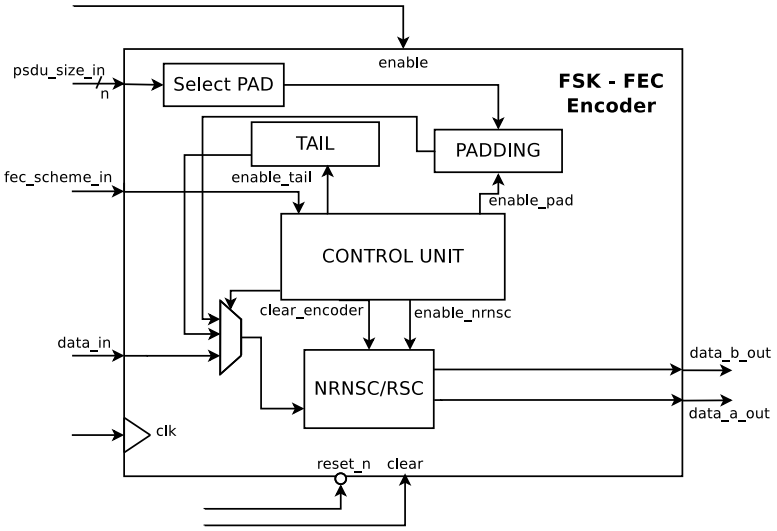
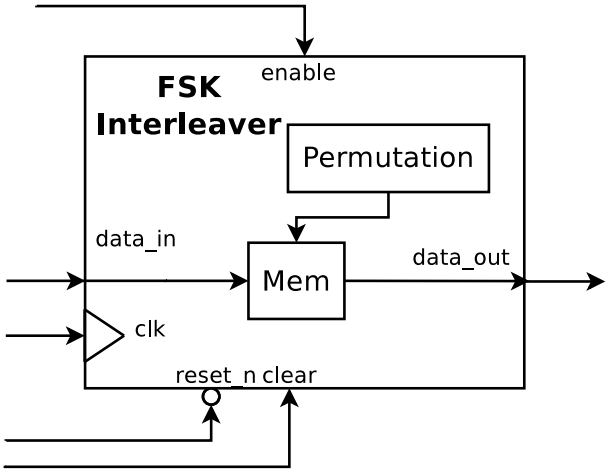
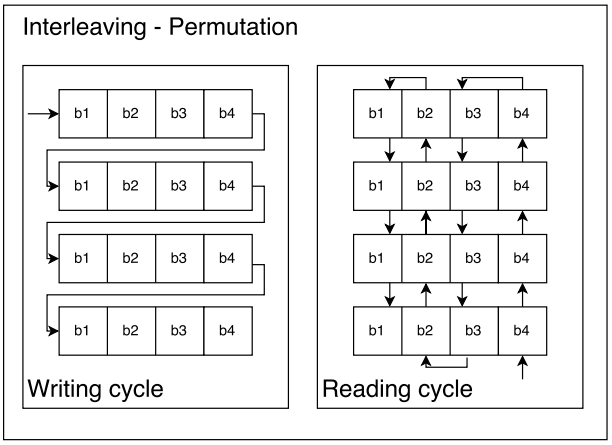


Figura 5.7 – MR-FSK FEC Encoder internal architecture.



(a) MR-FSK interleaver internal architecture.



(b) Block Diagrams detailing interleaver functionality.

Interleaver uses a 4x4 memory block to make bits permutation. During writing cycle, the input bits are written left to right, up to bottom. For the reading cycle, the opposite direction is used to assign data_out bits, as shown in Figura 5.8b. Interleaver output consists in PHR and PSDU fields. As data whitening is only applied in PSDU field, PHR is delivered to Framer, and PSDU goes to data whitening, if enabled. The block internal architecture is built of a control unit, a PRBS generator sub-block and a XOR operator, as detailed in Figura 5.9.

PHR and PSDU bits are bypassed in Framer block to FIFO, then to the signal modulator. It can perform FSK or GFSK modulation, depending on register configuration, as shown in Figura 5.10.

For the FSK modulation process, a digital COordinate Rotation Digital Computer (CORDIC) algorithm is implemented in conjunction with a phase generator, to compose a Numerically Controlled Oscillator (NCO). This block is used to synthesize the frequencies in the digital domain, providing the modulated signal for the RF up

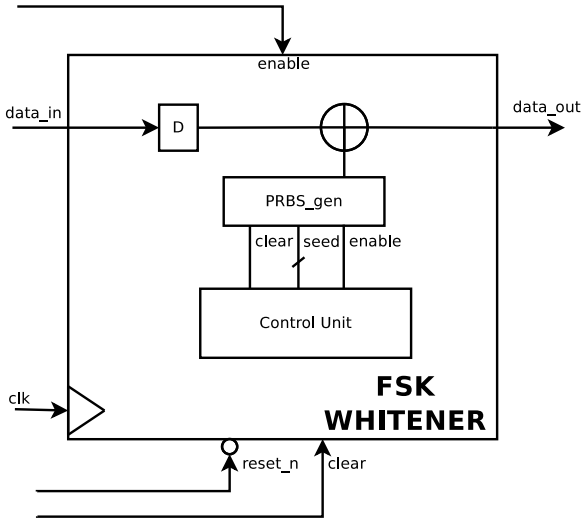


Figura 5.9 – MR-FSK data whitener internal architecture.

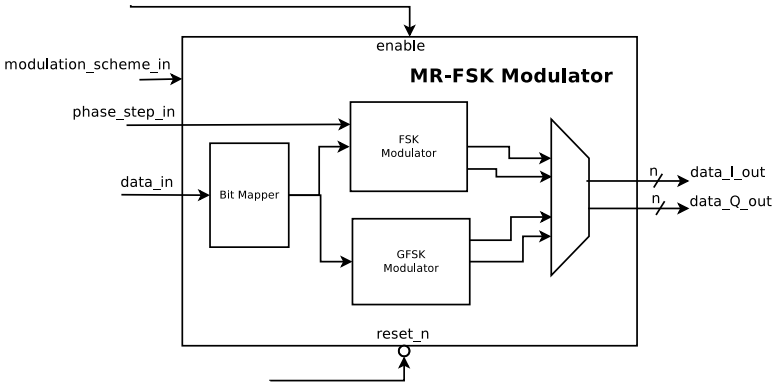


Figura 5.10 – MR-FSK modulator internal architecture.

conversion. The GFSK modulation has a similar architecture, only with the Gaussian filter applied to the input data, as can be seen in Figura 5.12.

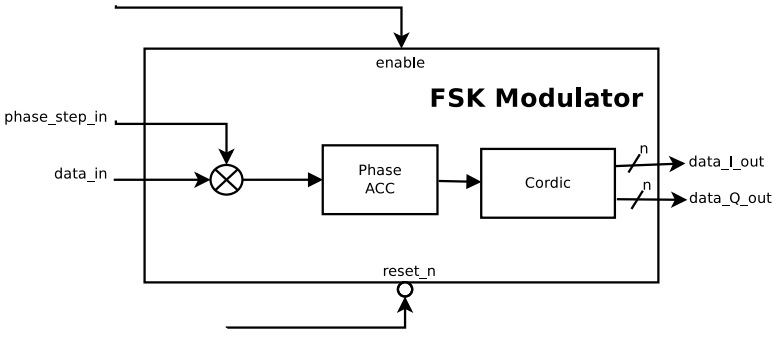


Figura 5.11 – MR-FSK FSK modulator internal architecture.

Both FSK and GFSK spectrum achieved with VHDL implementation, are shown in Figura 5.13, with similar result from the one found in Section 4.1.6, besides from side lobes with more noise from quantization.

Both modulation blocks use a CORDIC block, a well-used algorithm in mi-

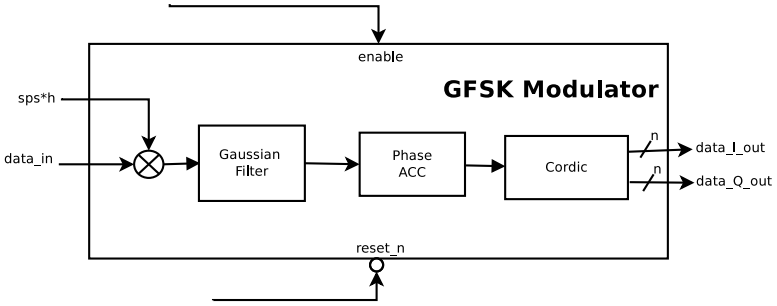
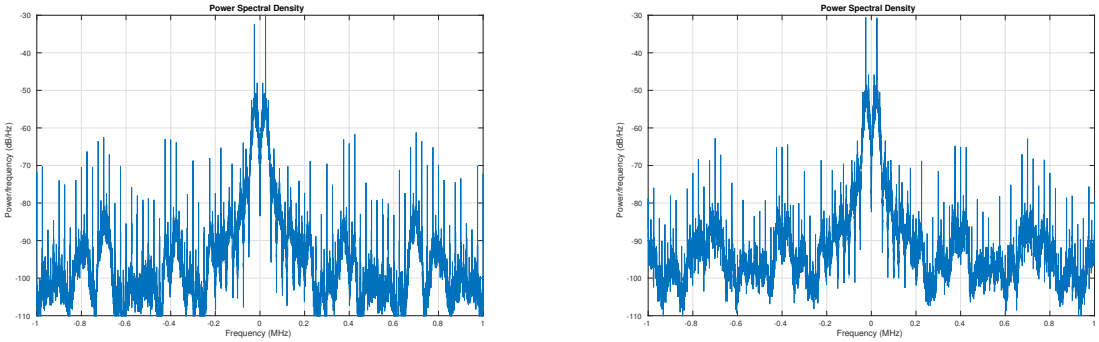


Figura 5.12 – MR-FSK GFSK modulator internal architecture.



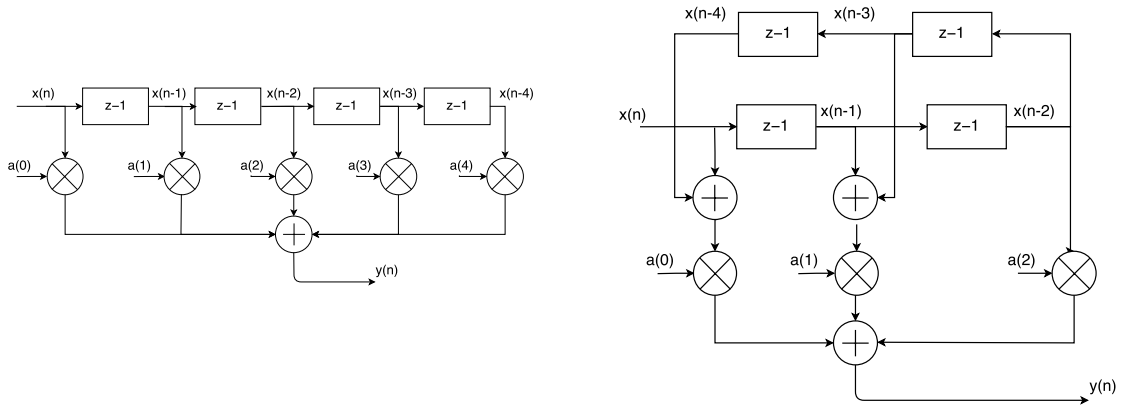
(a) FSK spectrum of VHDL data.

(b) GFSK spectrum of VHDL data.

Figura 5.13 – Spectrum for both modulations, obtained with VHDL data.

croelectronics, since it was developed to be used in real-time digital computation. The COordinate Rotation Digital Computer (CORDIC) is a computing technique that uses basic arithmetic to cover a range of function such as conversion from rectangular to polar coordinates and solve trigonometric computations. It has two possible computing modes, rotation and vectoring (VOLDERT, 1959). In the rotation mode, vectors coordinates and an angle are given; the algorithm rotates through the given angle resulting in new vector coordinates. In vectoring mode, the calculation results in magnitude and angle to a given vector (VOLDERT, 1959).

During work implementation, a different approach regarding filter implementation was used, since filters can use a significant amount of area, hence, Gauss filter used in modulation and others filters used in demodulation where implemented as symmetric filters, which reduces the number of multipliers used. That architecture can be used when the set of coefficients is symmetric. In the example shown in Figura 5.14a two pairs of coefficients have the same value, due to the the symmetric characteristic $a(0) = a(4)$ and $a(1) = a(3)$, which allowed the architecture simplification that can be seen in Figura 5.14b, reducing two multipliers. The amount of saved area increases with the number of coefficients used in filters.



(a) Linear FIR.

(b) Symmetric FIR.

Figura 5.14 – Diagram of Linear and Symmetric FIR implementation.

5.4 MR-FSK Demodulator Architecture

First block of MR-FSK demodulation is the signal demodulator, which will receive FSK or GFSK signals in baseband and demodulate them accordingly. However, before signal coming from antenna pass trough MR-FSK, a block outside this work scope, the resampler, does down sampling and interpolation based on a given ratio between input data sampling frequency and the desired output sampling frequency. Therefore, independently of data rate being transmitted at the time, the input signal in the MR-FSK receiver will be 20 samples per symbol. That number was proven sufficient for the demodulation process, for both GFSK and FSK. With that in mind, demodulation schemes were designed.

In a first approach, FSK demodulation is accomplished by passing the incoming signal through a sequence of two FIR filters (bandpass and lowpass) followed by a decision device, as can be seen in Figura 5.15. The filter coefficients are fixed and quantized with 8 bits, same as the output MR-FSK output. The bandpass filter is followed by a lowpass filter that works as an envelope detector. The envelope signal pass through an edge detector that work as a rough clock recovery algorithm. After that, a decision device chooses, based on a threshold, if the current signal is a logical zero or one.

The demodulation process demands significant amount of die area, as shown in Section 6.1.1. This approach was taken for rapid prototyping, since this FIR IPs are already in the groups library and are silicon proved. Later an IIR filter was implemented, and the demodulator was tested with IIR bandpass filters. Filter demodulation can also be applied for GFSK signal, as explained in Section 4, but with lower performance,

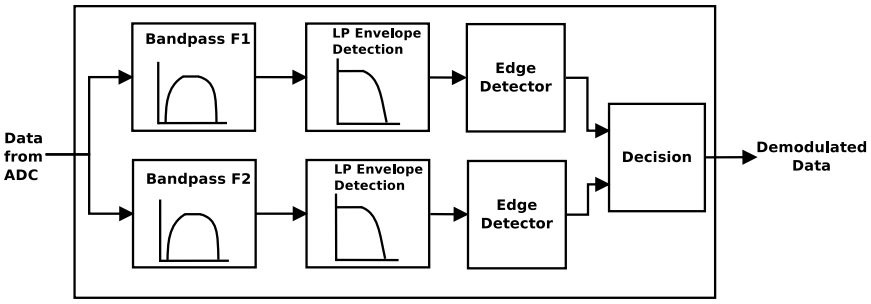


Figura 5.15 – FSK Demodulation using bandpass and lowpass FIR filters.

as will be detailed in Section 6.2. This approach was used for validation and FPGA synthesis results, but it was later deprecated.

In order to comply with all frequencies deviation required by the standard, filter demodulation approach was not possible, since filtering must adequate to the cutting frequencies, which would require a considerable amount of coefficients to be stored, as well as not adaptive multipliers, which consumes more area. Hence, other demodulation approaches were considered. The final MR-FSK architecture uses FSK correlation demodulator and GFSK asynchronous demodulation, in baseband, with phase derivation detection. Both demodulation schemes were explained in Section 4 and are detailed in Figures 5.16 and 5.17. These hardware implementation schemes will be further detailed.

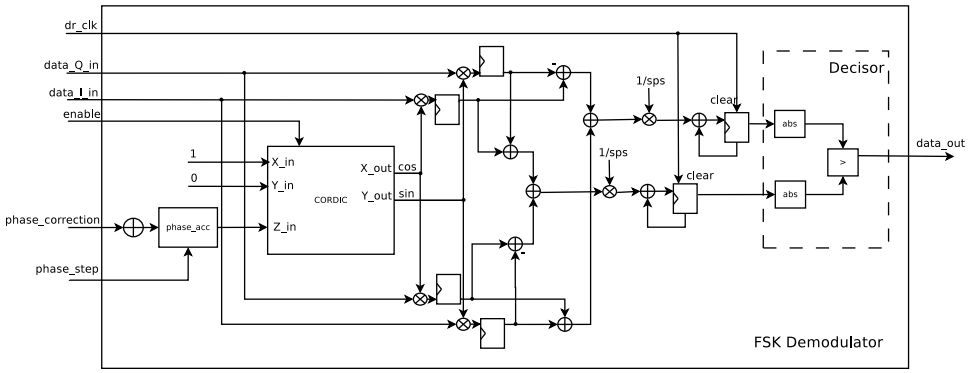


Figura 5.16 – FSK Demodulation using correlation.

The FSK demodulator uses a CORDIC block to compute cosine and sine wave. Multipliers, adders and registers are used to implement correlation functions, which will be used to correlate that computed signal with the received modulated signal. The decisor block decides which bit corresponds to the received pulse.

In the GFSK demodulator, depicted in Figura 5.12, CORDIC is used to retrieve the input signals phase. Then, signal derivation is calculated and compared with phase derivation expected for symbols 1 and -1. A IIR lowpass filter is used to smooth phase variations.

To make a better use of hardware area resource, it was used the same decisor block, for both demodulators.

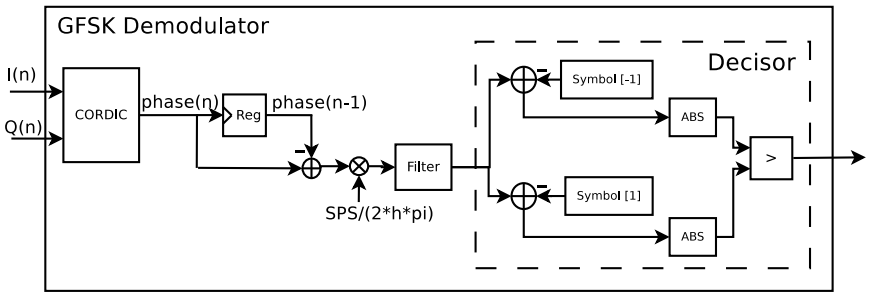


Figura 5.17 – GFSK Asynchronous Demodulation.

After signal demodulation, SHR detector block finds the preamble and detects if a valid packet has arrived. This block also compares the SHR sequence with four possible values to find out if FEC is enabled or not.

PHR and PSDU bits are input in FIFO, which bypasses PHR and holds PSDU until PHR parsing is complete. Therefore, data whitening can be applied to PSDU field according to PHR data.

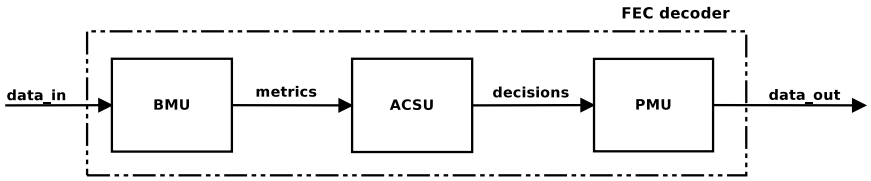


Figura 5.18 – Viterbi Decoder overview.

FEC decoder block implementation uses the well-known Viterbi algorithm. This block was silicon proven in a previous project. So, that hardware implementation was reused here with some adaptations to suit the trellis of the equivalent polynomial used by FEC encoder. Figura 5.18 gives an overview of the Viterbi decoder implementation, where the three blocks represents how the basic steps of the Viterbi algorithm are depicted. The Branch Metric Unit (BMU) that uses hard decision to calculate the distance between every possible bit and the input, the Path Metric Unit (PMU) which is responsible to decide which paths are more probable, discarding non optimal paths, and also storing each decision, finally, the Addition and Comparison Unit (ACS) obtains the most likely output based on the decision made by PMU. When FEC encoding is enabled, the PHR is also encoded. After the transmission parameters are known, the demodulated data can follow through the data path and the PSDU is delivered to the MAC layer.

5.5 Validation

The first validation of any block implemented in VHDL is to compare the output with the equivalent golden model (Matlab implementation) output, for a given input, through simulations.

Figura 5.19 is a simplified diagram of MR-FSK modem, for the case that all blocks are enabled. The highlighted points, with letters, shows the equivalence of data in both sizes of the modem. Observe that there are an equivalence of the transmitter signals to the receiver signals which are indicated by the same letter in the figure. This equivalence was used as a second validation of the process, using only in VHDL implementation.

The comparison is done automatically, using monitor blocks to receive the valid data and write it in text files. After simulation, files from correspondent points are compared with scripts automating that task.

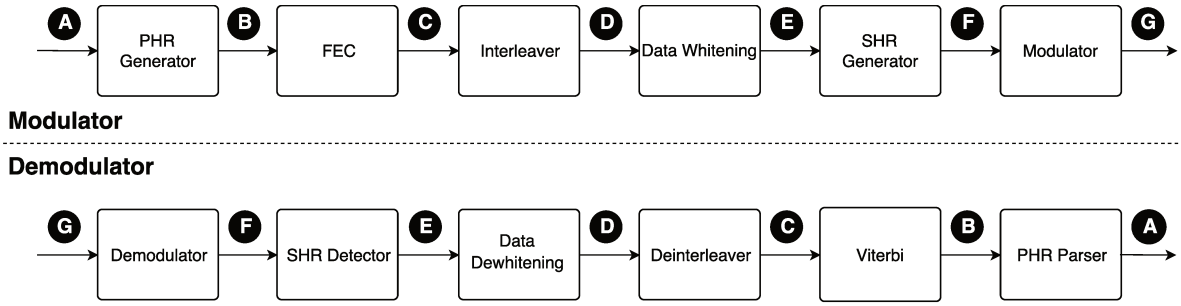


Figura 5.19 – Validation Diagram.

6 RESULTS

This chapter will present Synthesis (Section 6.1.1) and Performance Results (Section 6.2) for the complete MR-FSK modem VHDL implementation, comparing demodulation techniques when applicable.

6.1 Synthesis Results

Synthesis results can be obtained through code compilation in Altera and Cadance software, for synthesis results aiming FPGA devices and ASIC, respectively. For FPGA results, Quartus II software, from Altera was used. The compilation process accomplishes logic synthesis, which optimize design logic and performs technology mapping, resulting in logic blocks used as resources to implement the design in a target device. For ASIC, besides the logic synthesis, also a physical synthesis is done. The physical synthesis transforms the gate level netlist, obtained in logical synthesis to a silicon layout. This section will show the results of both FPGA and ASIC synthesis, detailing each VHDL block of the complete MR-FSK modem.

6.1.1 FPGA

FPGA result target the EP4SGX230KF40 Altera device, of Stratix IV family, showing the number of Adaptive Logic Modules (ALM), Memory and Registers used by the digital architecture, presented in Table 6.1, the results are divided in TOP (modulator and demodulator), TX (modulator) and RX (demodulator) results. TOP results are related to integration control logic, data processing and signal processing blocks of transmitter and receiver, only including GFSK and FSK baseband demodulation schemes (FSK correlation demodulator and GFSK asynchronous demodulator) at demodulator. Modulator is further divided into data processing, detailing each block of this category, FSK modulator and GFSK modulator. Demodulator also contains internal control logic, data processing, and all demodulators options. Filter demodulator is related to FSK and GFSK asynchronous demodulation, implemented with IIR bandpass filter and FIR lowpass filter. Also, baseband demodulation schemes for FSK (correlation demodulation) and GFSK (synchronous demodulation), were computed.

Comparing ALMs results of data processing blocks with modulators and demodulators, it can be concluded that signal processing blocks, in the MR-FSK, uses more ALMs resources than data processing blocks. Modulator (Tx) data processing blocks uses 596 ALMs, on the other hand, signal processing blocks uses 987 ALMs.

Tabela 6.1 – MR-FSK Modem Implementation Results for Altera's 5CGXFCC5C6F27C7N.

		ALMs	Memory	Registers
TOP		6324	64	6335
TX	Data Processing	596	32	430
	FSK Mod	456	0.0	446
	GFSK Mod	531	0.0	664
RX	Data Processing	915	32	713
	Filter Demod	2041	0.0	2685
	Correlator Demod	989	0.0	938
	GFSK Sync Demod	1145	0.0	1128

For the demodulation (Rx) portion, we have a similar result, with correlator demodulator using more ALMs than all data processing blocks. Register utilization follows the same trend, with filter demodulation using more resources

The difference between resource utilization in FSK and GFSK modulator is due to the FIR filter, used to implement Gaussian filtering, in GFSK modulation. All memory blocks where used in interleaver and deinterleaver data processing block, where each one uses a memory of 16 symbols, equivalent to two codded bits.

6.1.1.1 FSK Filter (IIR) x FSK Correlator

IIR filters can achieve better performance than FIR filters using less coefficients. Less coefficients demand fewer multipliers that result in lower resources utilization. FSK Correlation demodulator architecture, as shown in Figura 5.16 uses 8-bit multipliers and a CORDIC that result in more resources utilization than demodulation using filters. A further area reduction on the correlation architecture can be implemented by substituting multipliers for other CORDIC.

6.1.1.2 GFSK Synchronous x Asynchronous

GFSK asynchronous demodulation is achieved using the filter demodulation approach. GFSK synchronous demodulation uses fewer ALMs and registers, and also provide a better performance, as it will be shown in Section 6.2.2. The asynchronous demodulation is not ideal for GFSK signals, this demodulation approach was used only to modulator validation, since it was already implemented and used for FSK demodulation.

6.1.2 ASIC

An important outcome for this work is synthesis results for the ASIC implementation, conducted with Cadance software for 65nm CMOS technology. The synthesis

Tabela 6.2 – Logical synthesis results for 65nm CMOS.

MR-FSK Modem	**Cells**	**Area** (μm^2)	**Leakage Power** (nW)	**Dynamic Power** (nW)
TOP				
└ TX	117020	528231	1060.663	2355076.852
└ Total Data Processing	9659	39053	290.486	384838.581
└ PHR Generator	1895	8492	187.723	64790.658
└ Linker	189	663	1.884	7072.844
└ FEC Encoder	240	841	2.577	5116.286
└ Interleaver	563	1697	4.944	16156.783
└ Whitener	203	3138	171.912	19717.689
└ Framer	272	887	2.638	5890.825
└ Total Signal	313	898	2.668	10836.231
Processing	6890	27671	94.417	284634.601
└ GFSK Modulator	2632	10509	36.048	103223.953
└ FSK Modulator	4311	17383	59.055	181627.335
└ RX	41911	173744	763.859	1957013.171
└ Total Data Processing	4790	20493	227.675	184927.18
└ SHR Detector	1698	6691	21.596	67791.734
└ Dewhitener	366	1289	3.960	12503.966
└ Linker	215	757	2.253	8794.933
└ Deinterleaver	222	3154	171.964	23393.410
└ Viterbi Decoder	1922	7331	24.179	60584.493
└ PHR Parser	278	984	2.868	9349.043
└ Total Signal	36706	151557	307273.146	1483506.229
Processing	13426	59808	225.146	571877.266
└ Time Sync	8146	33485	112871	307273.146
└ CFO	6656	25601	84574	253158.566
└ GFSK Demodulator	8478	32663	109603	351197.251
└ FSK Demodulator				

flow steps cover logic and physical synthesis, where the HDL code results in cells mapped to the chip area.

The amount of required cells, area occupation and device power consumption for the entire MR-FSK modem, resulted of logical synthesis, are detailed in Table 6.2.

The power results for logic synthesis are divided in Leakage and Dynamic power. The former one has no contribution to circuits functionality, as it comes from leakage current and characterizes the static power dissipation. Dynamic Power is the

Tabela 6.3 – Physical synthesis results for 65nm CMOS.

	Die Area (μm^2)	**Density**	**Instances**
MR-FSK	884400.00	43.79	117466

Tabela 6.4 – Physical synthesis results for 65nm CMOS.

	Internal Power (mW)	**Switching Power (mW)**	**Leakage Power (mW)**	**Total (mW)**
MR-FSK	43.79	19.36	0.02538	63.17

actual power consumed by the circuit to change their logic state. Although the IEEE 802.15.4g standard focus in low power, no power optimization codification technique was used, but MR-FSK control logic was designed to reduce power, by enabling blocks only when they are being used.

As can be seen in Table 6.2, leakage power, as expected, corresponds to a small percentage of the total power. Signal processing blocks, in general, use more power than data processing blocks, as expected. Interleaver and deinterleaver blocks show more leakage power, by a great range, than the rest of the data processing blocks, which can be attributed to the internal memory used in implementation.

Table 6.3 lists the physical synthesis results of the complete digital MR-FSK Transceiver, with a $884400.0\mu m^2$ die area using 65nm CMOS technology, with 43.79 of density, using 117466 instances. This result include the system depicted in Figura 5.2, where the RF interface contains a resampling block, detailed in 5.4 and MAC interface are composed of SPI an I2C protocol.

Physical synthesis acquire different power results than logical synthesis. Table 6.4 shown results for internal, switching, leakage and total power. Internal power is the one consumed by the circuit dynamic elements. Switching power is the power used by gate capacitance, to charge and discharge. In addition, the total power is the sum of each power category.

By the time of completion of this work, no other estimative of area and power, using the same technology or prototype boards and covering fully digital implementation of an MR-FSK transceiver, were found in the literature.

6.1.2.1 Tape-out

As mentioned before, this work is part of a project aiming to tapeout a IEEE802.15.4g chip. In the moment of conclusion of this work, the chip went through a tape-out process. The results here present involve the works from other people from the author's research group.

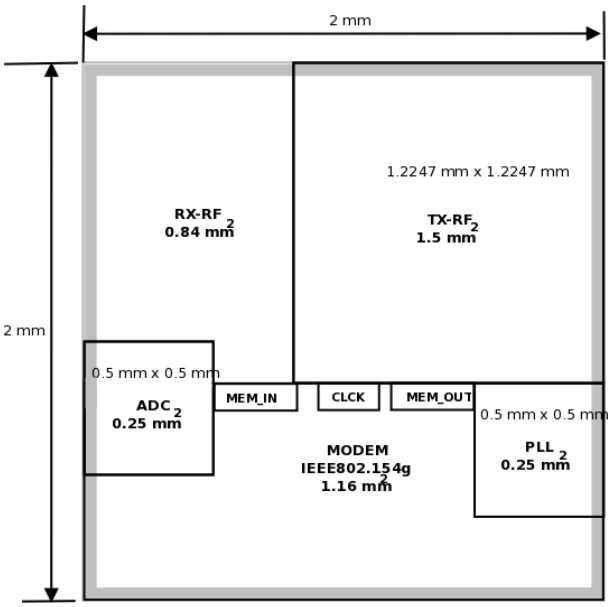


Figura 6.1 – Die diagram for chip.

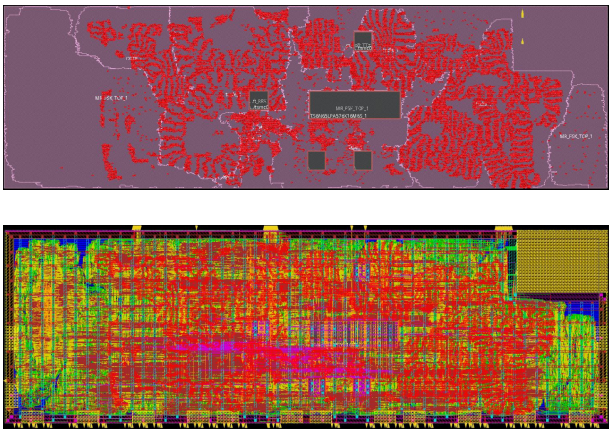
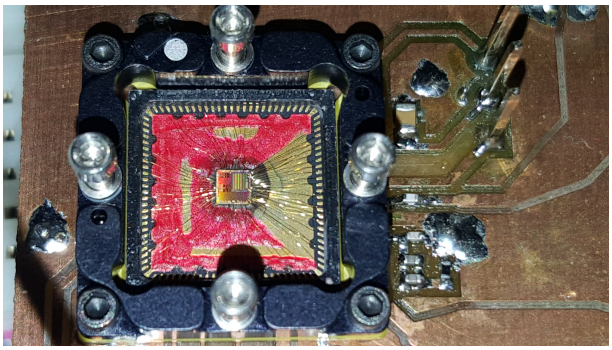


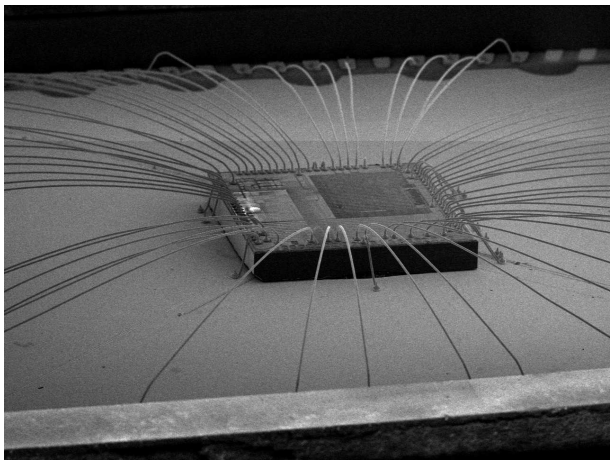
Figura 6.2 – Amoeba image from Calibre Software.

Figura 6.4 illustrates the components, position and dimension for the project die. The total area is 4mm^2, where 1.16mm^2 is used by the IEEE 802.15.4g modem. Figura 6.3 shows pictures from one of the chip samples (Figura 6.3a), and detailed pictures of the die, taken from Scanning Electron Microscope (SEM) (Figura 6.3b and 6.3c).

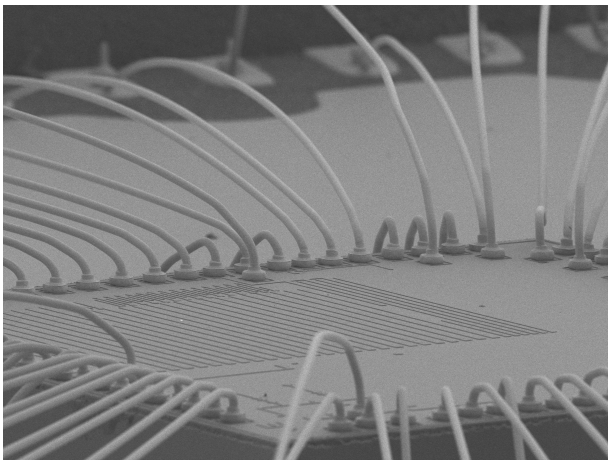
With the first die samples, a test board was designed (Figura 6.3a) and, at the time of this work, a few tests could be made as the result shown in Figura 6.4, where the quadrature channel of FSK modulation for a data rate of 50kbps.



(a) Chip photograph, in test board.



(b) Die picture taken from Scanning Electron Microscope (SEM).



(c) Detailed Die picture, from Scanning Electron Microscope (SEM).

Figura 6.3 – Integrated Circuit pictures.

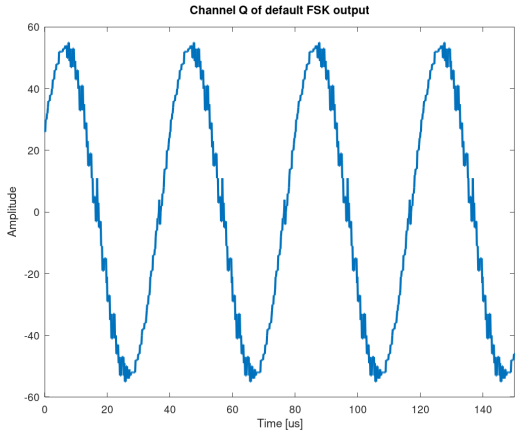


Figura 6.4 – Q Channel for 50Kbps FSK modulation.

6.2 Performance analysis (BER)

Bit Error Rate (BER) is a performance measure for signal demodulation techniques. As a case of study of this work different demodulations for FSK and GFSK, the BER performance for baseband and intermediate frequency demodulation, implemented in Matlab, are compared, along with the VHDL implementation of baseband demodulation BER. This section will be divided in performance results related to FSK and GFSK signal modulation.

Forward error correction is a technique that enhances BER results, as explained in 4.1.2, but the efficiency is directly related to the trace back of Viterbi algorithm implemented in the demodulation part. Trace back should be at least 5 times the constraint lengths (k). The standard specifies k=3, so trace back should be at least 15 (MOISION, 2008). Meaning that, after 15 coded symbol (2 bits, for standard specification), Viterbi will output the first decoded bits. However that causes a problem regarding MR-FSK internal data flow control. As explained in Section 5.4, PSDU data bits are held in FIFO, until PHR parser is done passing through Viterbi block. If a trace back of 15 is used, 32 bits will be needed for one output bit. So, for all PHR to be decoded, since PHR coded symbols are 32 bits length, Viterbi decoder needs a total of $b_{\text{tv}} = 32 + 32 = 64$ input bits, which would include PSDU bits. That configuration is not possible, since PHR holds the information to enable PSDU dewhitening, a process that needs to be done before data decodification. One approach can be used to reduce b_{tv} value. Hence the fifth bit of PHR holds data dewhitening enabler information, b_{tv} can be reduced to $b_{\text{tv}} = 32 + 10 = 42$, which would still need PSDU bits. For that reason the Viterbi decoder trace back must have a maximum value of 11 ($b_{\text{tv}} = 32 = 10 + (2\,traceback)$) to work with MR-FSK integration. As it does not meet minimum traceback required for FEC efficiency, modem performance using FEC codification is not going to be analyzed.

6.2.1 FSK

Frequency Shift Keying is one of the signal modulations covered by the IEEE802.15.4g, for the MR-FSK modem. Demodulations techniques are compared using AWGN channel. For a non-coherent demodulation, theoretical M-FSK bit error rate (P_{b}) is given by the equation 6.2, from (PROAKS, 2001) :

$$P_s = \sum_{m=1}^{M-1} (-1)^{n+1} \binom{M-1}{m} \frac{1}{m+1} exp\left[-\frac{m}{m+1}\frac{E_b}{N_0}\right], \tag{6.1}$$

$$P_b = \frac{1}{2}\frac{M}{M-1}P_s. \tag{6.2}$$

For a 2FSK non coherent demodulation, M = 2 :

$$P_b = \frac{1}{2} exp\left[-\frac{1}{2}\frac{E_b}{N_0}\right]. \tag{6.3}$$

Equation 6.3 corresponds to the theoretical BER performance, designated in Figura 6.5. There is not a non-coherent demodulation scheme that will achieve better performance than the theoretical, as the theoretical curve represents the best performance that can be achieved in terms of BER, if no error correction algorithms is applied. Figura 6.5 shows that FSK correlation model, meets the theoretical BER curve for a non-coherent demodulation scheme, but the filter demodulation has a performance with 3 dB degradation for higher E_b/N_0.

The BER performance shown in Figura 6.6 is the same for any modulation configuration, like data rate and modulation index, where it can be seen two curves overlapping one another, for the filter FSK demodulator using h=0.5 and h=1 and also both curves for correlator FSK demodulator, overlapping with FSK Theorical BER. The VHDL result presented in Figura 6.5 suffers degradation when compared to the algorithm implemented in Matlab, which can be explained by the fact that HDL implementation is quantized and that the modem scheme uses a resampling in the receptor, which was not implemented in Matlab. The resampling can affect demodulation, since it reduces symbol oversampling. Moreover, VHDL simulation is time consuming, to overcome that, fewer Eb/N0 values were used and only one simulation was executed for each of these values, in contrast with Matlab curves, that used the mean BER value between ten simulation, for the same Eb/N0.

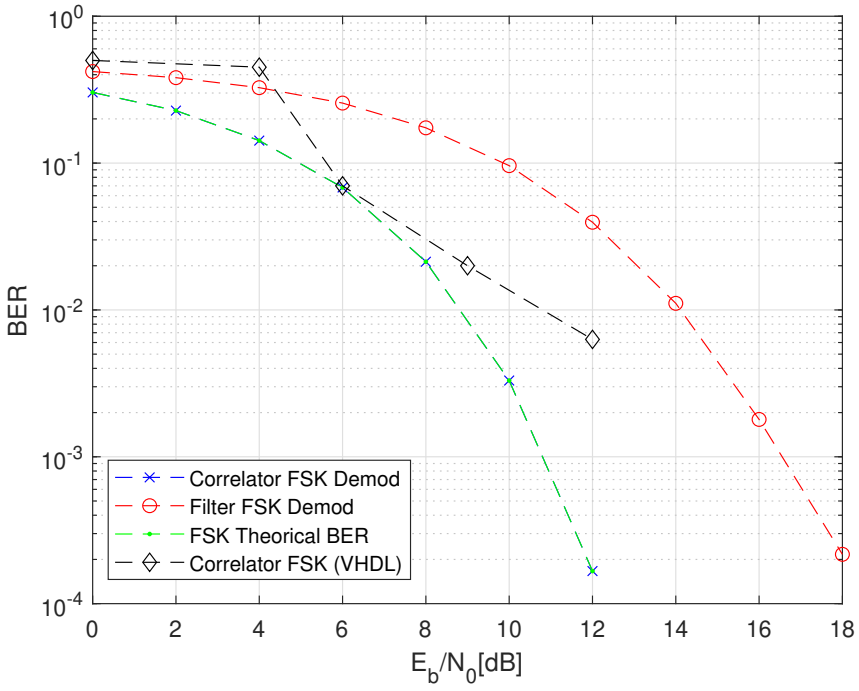


Figura 6.5 – 2FSK BER curve for Correlation demodulation, Filter demodulation, Theoretical curve and VHDL Correlation demodulation.

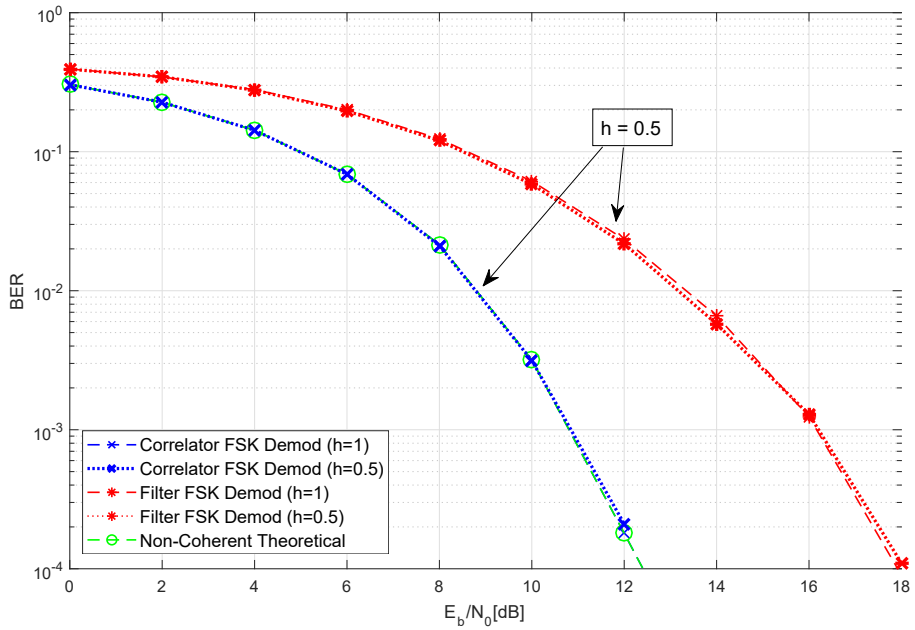


Figura 6.6 – Comparison between 2FSK BER curve for correlator and filter demodulator using modulation index (h) of 1 and 0.5.

6.2.2 GFSK

Gaussian Frequency Shift Keying is the mandatory signal modulations for the MR-FSK modem. Demodulations techniques are compared using AWGN channel. GFSK bit error probability is the same as FSK, for non-coherent demodulation, considering a modulation index higher than 0.5, as explained in (LUQUE; MORÓN; CASILARI, 2012), which is the case of the parameters defined by the norm for 2GFSK demodulation. Therefore, equation 6.3 gives the target performance for 2GFSK demodulation. There are also references curves of other types of GFSK demodulator showed in (YU; YANG; CHONG, 2011).

For Bit error rate analysis, synchronous and asynchronous demodulation are compared with the theoretical curve for a non-coherent demodulation, in Figura 6.7. With 4dB difference, asynchronous demodulation achieves a worst error probability for same signal to noise error. Once it is understood that GFSK pulses shift towards f_0 and f_1, with a smooth phase derivation, it can be accepted that fixed filters demodulation (asynchronous demodulation) has a worst performance than phase derivation (synchronous demodulation). The asynchronous demodulation, also known as filtered demodulation, for GFSK, is consistent with the result presented in Figura 6.7 and in (XIA et al., 2003).

The results of this works implementation for the synchronized method, that can also be classified as a classical phase unwrapping, is slightly better than the one showed in (YU; YANG; CHONG, 2011), comparing the result with modulation index of 1,

which is the case of the result obtained here.

Figura 6.7 show results for VHDL implementation of synchronous demodulation, compared to results obtained with Matlab. Hardware implementation comes with limitation whereas precision is inversely proportional to hardware area, also, as mentioned in Section 6.2.1, VHDL result take in consideration the use of Resampler block, not implemented in Matlab.

Matlab implementation of baseband (Synchronous GFSK demodulation) and intermediary frequency (Asynchronous GFSK demodulation), can vary depending on data rate and modulation index (h), as can be seen in Figura 6.8, that uses data rate of 200 kHz, but differ in modulations index (1 and 0.5), as indicated. It can be notice a 3dB decrease in the synchronous demodulation. Comparing Figures 6.7 and 6.8, it can be seen a difference in performance due to different data rate used (100 kHz and 200 kHz, respectively). Therefore, GFSK performance can vary considerably, with change in modulation parameters, as data rate and modulation index.

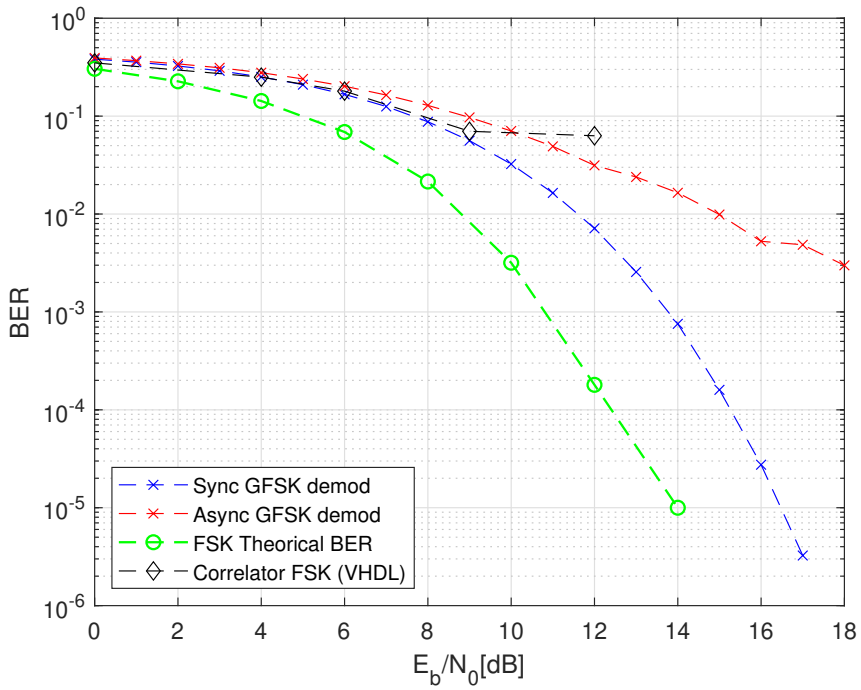


Figura 6.7 – 2GFSK BER curve for Synchronous demodulation, filter demodulation, theoretical curve and VHDL implementation of Synchronous demodulation.

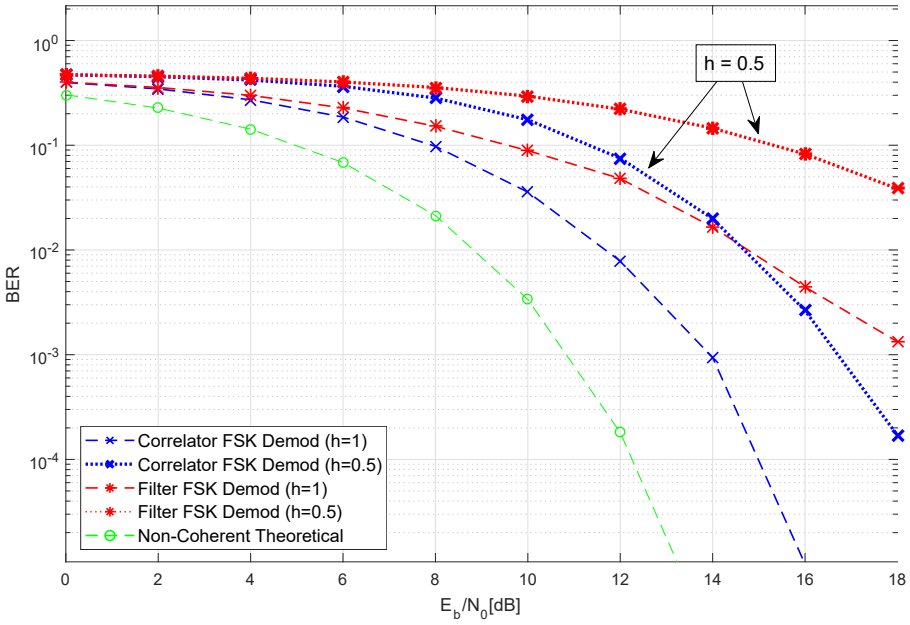


Figura 6.8 – Comparison between 2GFSK BER curve for correlator and filter demodulator using modulation index (h) of 1 and 0.5.

CONCLUSION

This work focuses on implementing a SUN-devoted MR-FSK PHY compliant to IEEE 802.15.4g, which integrates all modules for all operation modes used in worldwide frequencies. The total die area is 884400.0 μm. The transceiver's total power consumption is 63.17 mW. This work is part of a project that integrates all PHYs covered by the IEEE802.15.4g standard to produce a transceiver compliant to SUN applications. This work covers all design flow since the standard's study through model and hardware implementation. Standard definitions are not always clear, which can cause implementation difficulties. One of them was explained in Section 6, related to payload decodification. In the time of this work, no similar papers that could provide fair result comparison were found, as explained in Section 2.

In the early stages of this work, the same demodulation approach was used for FSK and GFSK signals. The filter-based demodulation, used for intermediary frequency signals, a well-known FSK signal demodulation technique, is also used to validate the GFSK modem. The study of MR-FSK transceiver showed that, for support all data rates previewed at the standard, baseband demodulation would be more suitable, so the correlation and synchronous scheme were used for FSK and GFSK demodulation, which resulted in a better performance for FSK signal demodulation and, for GFSK, in most of the cases. As explained in Section 6, GFSK performance results may vary with data rate and modulation index, which is not the case for FSK demodulation.

Matlab implementation of baseband FSK modem showed a BER result compatible with the theory of non-coherent 2FSK demodulation, which did not occur with filter based demodulation and VHDL implementation of correlation demodulation (baseband), due to hardware limitations, introduced to filter coefficient and inherent to VHDL implementation. For GFSK, a referenced paper shows that for the cases covered by the standard, the same non-coherent theoretical BER curve can be used as a reference, but our Matlab implementation did not present a compatible result, due to filter coefficients limitation, both in the filter and synchronous demodulation, which also affects VDHL implementation.

For future work, the implementation of a 4-level FSK and GFSK modulator and demodulator will demand the study of demodulation techniques, preferable using the already implemented demodulator. For area and code maintainability improvement, a second CORDIC could be utilized at correlator demodulator VHDL implementation in order to achieve correlation multiplication. That would remove variable multipliers from implementation, which are area consuming. Some low-power codification techniques

can be applied to reduce power consumption. In addition, wireless networks bring security and privacy challenges, making that an important topic to be covered in future works.

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