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Mateus Pinheiro Dias

DC bus Power Electronic Conditioner for Electric Aircraft System

Condicionador Eletrônico de Potência para Barramento de Tensão CC em Sistema Elétrico Aeronáutico

Campinas

2020

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Supervisor: Prof. Dr. José Antenor Pomilio

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Prof. Dr. José Antenor Pomilio (Presidente, FEEC/UNICAMP)

Dr. João Inácio Yutaka Ota (FEEC/UNICAMP)

Prof. Dr. Flávio Alessandro Serrão Gonçalves (Unesp)

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I dedicate this work to my family.

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"fede portai al glorioso offizio,
tanto ch'i' ne perde'li sonni e 'polsi"
Inferno-Canto XIII
Dante alighieri

Abstract

This project deals with the Electric Power Quality (PQ) in aeronautical environments. The More Electric Aircraft (MEA) concept focuses in the replacement of pneumatic and hydraulic actuators by electromechanical actuators and increases the electric power demand in the aircraft. The master project aims to the study and the implementation of a Power Electronic Conditioner (PEC) to mitigate the unwanted effects found in the DC aircraft internal feeders. The PEC must deal with the current unbalance between the positive and negative poles of the DC bus to comply with the standards. The specific objectives are the development of a mathematical dynamic model for the current redistributor used as PEC and the study of control strategies for this aircraft electrical environment. Digital control solutions, with DSPs, FPGAs were studied along the project development. The appendixes provide the paper published in Cobep/Spec 2019 and experimental Setup.

Keywords: Power Electronic Conditioner; More Electric Aircraft; DC redistributor.

Resumo

Este projeto trata sobre a qualidade de energia em ambientes aeronáuticos. O conceito More Electric Aircraft-MEA é baseado na substituição de atuadores pneumáticos ou hidráulicos por atuadores eletromecânicos, a qual ocasiona o aumento do consumo de energia elétrica do avião. Este projeto de mestrado foca no estudo e na implementação de um Condicionador eletrônico de Potência (CEP) para mitigar os efeitos indesejados encontrados nos alimentadores do barramento CC. Este CEP deve mitigar o desbalanço de corrente entre os alimentadores do barramento CC para a adequação com as normas de qualidade de energia. Os objetivos específicos deste trabalho são o desenvolvimento matemático do modelo dinâmico do redistribuidor de corrente usado como CEP e o estudo de técnicas de controle para este ambiente elétrico aeronáutico. Soluções digitais de controle com DSPs, FPGAs ou outros microcontroladores também foram estudadas durante este trabalho. Os Apêndices mostram o artigo publicado no Cobep/spec 2019 e os experimentos.

Palavras-Chaves: Condicionador eletrônico de Potência; Sistemas Aeronaúticos; Redistribuidor de Corrente cc.

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1 Introduction

This chapter presents a literature review on application of dc currents redistributors. Firstly, a brief historic review of grownth on aircraft transportation and its global impacts is presented. The chapter discusses the aircraft standards regarding electrical power quality, more specifically the MIL-STD-704F and the standard RCTA-DO106F.

1.1 Research Background

In Brazil, Revenue passenger Kilometres (RPK) has increased by 85% from 2008 to 2017 and maintained a steady growth of 7.1% per year. Only in the last ten years, the amount of domestic passengers has increased 67%. Comparing the regular transport service between different states, aviation represented 67.5% while road sector only represented 32.5% [1].

The global energy use balance shows that transport sector has been the biggest and fastest growing sector in energy consumption and accounted for 34 % in 2014, the highest share of world final consumption [2]. Transport sector consumed almost 2500 million tonnes (Mtoe) of total oil consumption, and it emitted almost a quarter (24 %) of carbon dioxide (CO_2) global emissions in 2018 [3],[4]. Due to the economical advances and the search for a sustainable future, the aircraft sector has been dealing with power electronics solutions for more reliable equipment.

Figure 1.1 shows a modern aircraft electric system , which has an electrical grid consisting of many subsystems. There are several different voltage levels and frequencies, including dc buses[5], [6], [7], [8].

There are a main ac voltage bus of 230 V with variable frequency (360-800 Hz) , ac voltage bus of 115 V with variable frequency and ac bus 230V fixed frequency. Furthemore , there are different dc voltage buses such as 28 V, 270 V and 540 V [9], [10].

The electrical energy consumption has increased in the commercial aircraft mainly due to the replacement of hydraulic and pneumatic actuators by electromechanical devices. Figure 1.2 shows this trend.

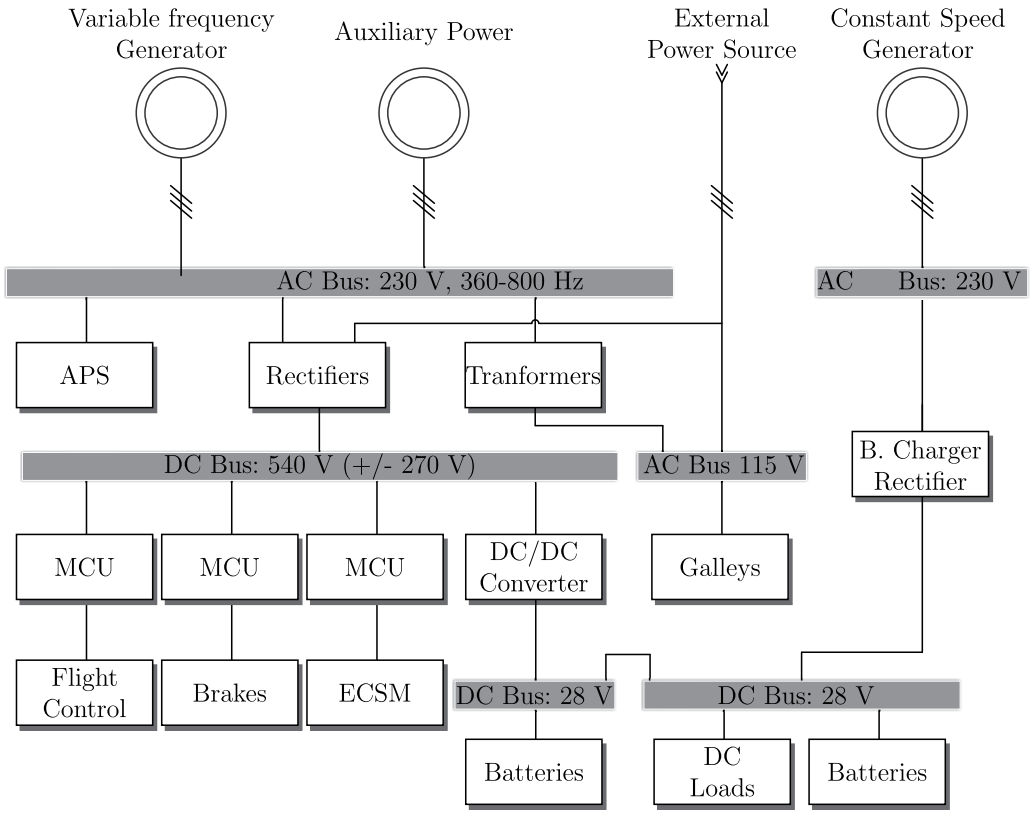


Figure 1.1 – A typical architecture of a modern MEA .

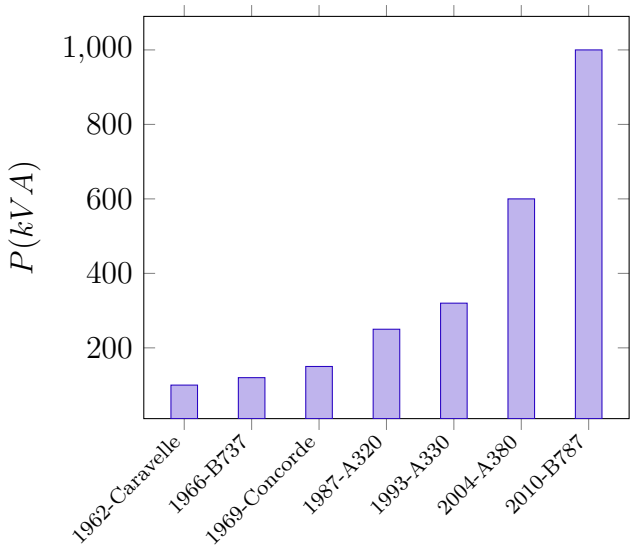


Figure 1.2 – Increase of power consumption in commercial aircraft.

This trend has been called as the More Electric Aircraft (MEA) [5], [11], [12], and it contributes for decreasing aircraft mass and the fuel consumption. Furthermore, this advancement has motivated several research in power electronics field for more reliable, less maintenance and more efficient equipment[13][14][15], which include power distribution, power generation, engine gearbox, ice protection systems etc [16]. Power electronics devices have an important contribution for the development of a new Power

Distribution Systems (PDS), with protection devices like circuit breaker and fault circuit breaker [17],[18].

1.2 Aircraft Standards

The first generation of ac aircraft grids works at a fixed frequency (400 Hz 115/200 V)[11]. This solution is also used in medium-sized aircraft including, for example, the EMB190 and EMB195 (Embraer). The second generation, with variable frequency (230/400 V 360-800 Hz) include Boeing 787, Airbus A380 and A350 [5]. Both ac and dc grids must comply with Power Quality (PQ) standards.

The MIL-STD-704F[19] standard establishes the limits for voltage in dc and ac buses and for the spectral distortion among other characteristics. The aim is to guarantee compatibility between the aircraft electric system, external power, and airborne utilization equipment.

The design of the aircraft electric power system must ensure that the electric power complies with the requirements during the operation modes defined by the standard.

For a normal operation, the voltage shall be in range shown in the Table 1.1.

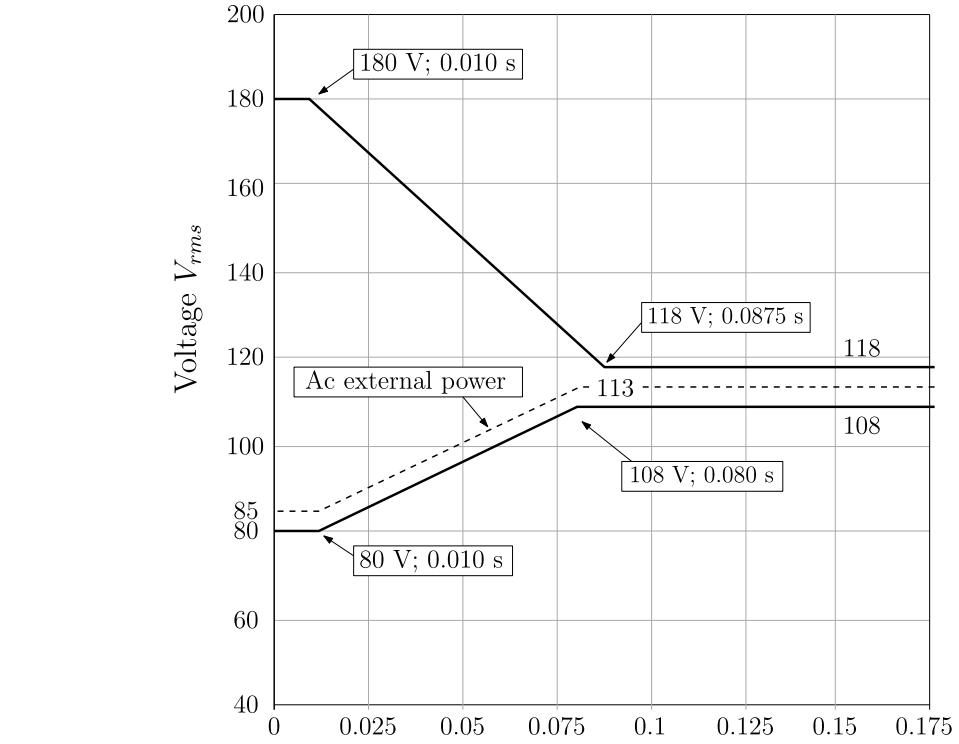
Table 1.1 – Normal operation characteristics for ac and dc voltages.

DC BUS	
28-V-system steady state	22 to 29 V
28-V-system ripple amplitude	1.5 V
270-V-system steady state	250 to 280 V
270-V-system ripple amplitude	6 V
AC BUS	
System steady state - phase voltage	108 to 118 V, RMS
Variable Frequency	360 to 800 Hz

Figure 1.3a shows the ac limits of a voltage transient and figure 1.3b shows the maximum distortion spectrum of 400 Hz and variable frequency ac voltage.

Figure 1.4a shows the dc limits of a voltage transient and figure 1.4b shows the maximum distortion spectrum of 400 Hz for the 270-V dc system.

Conversely, the standard RCTA-DO106F [20] describes the procedures for testing equipment or loads that will be installed in the airplane. As an example, table 1.2 shows the the current harmonic limits for a single-phase equipment and Table



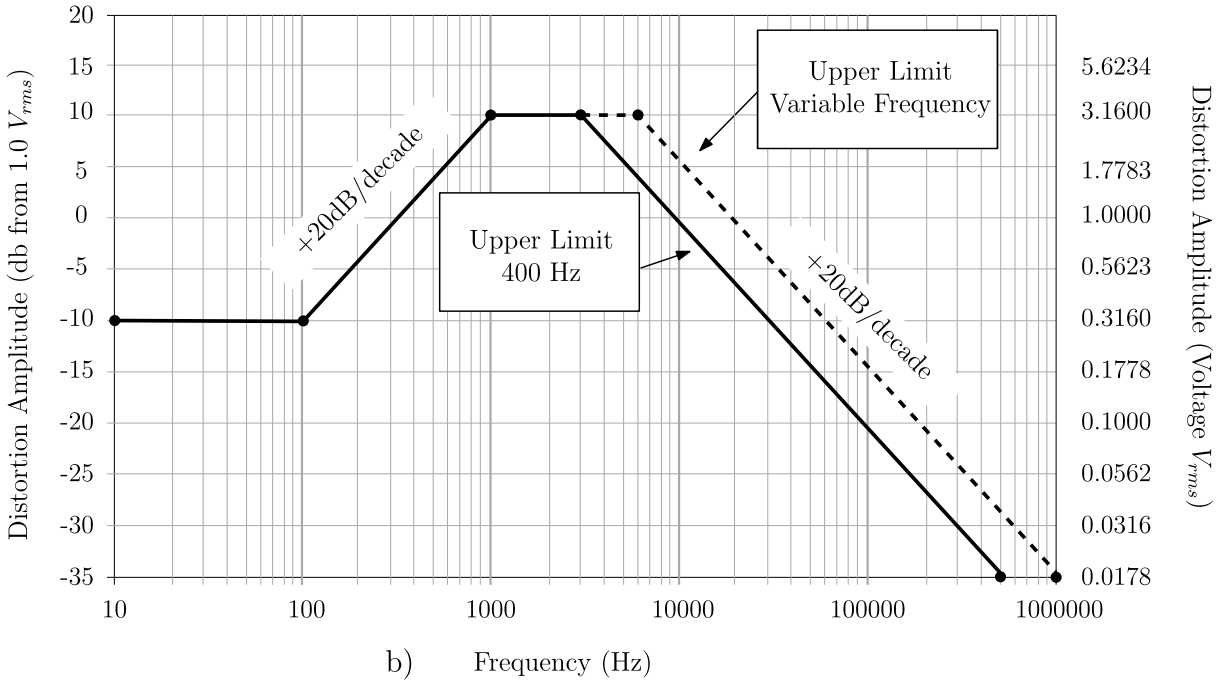


Figure 1.3 – ac limits: a) Envelope of 400 Hz and the variable frequency ac voltage transient; b) Maximum distortion spectrum of 400 Hz and the variable frequency ac voltage ;

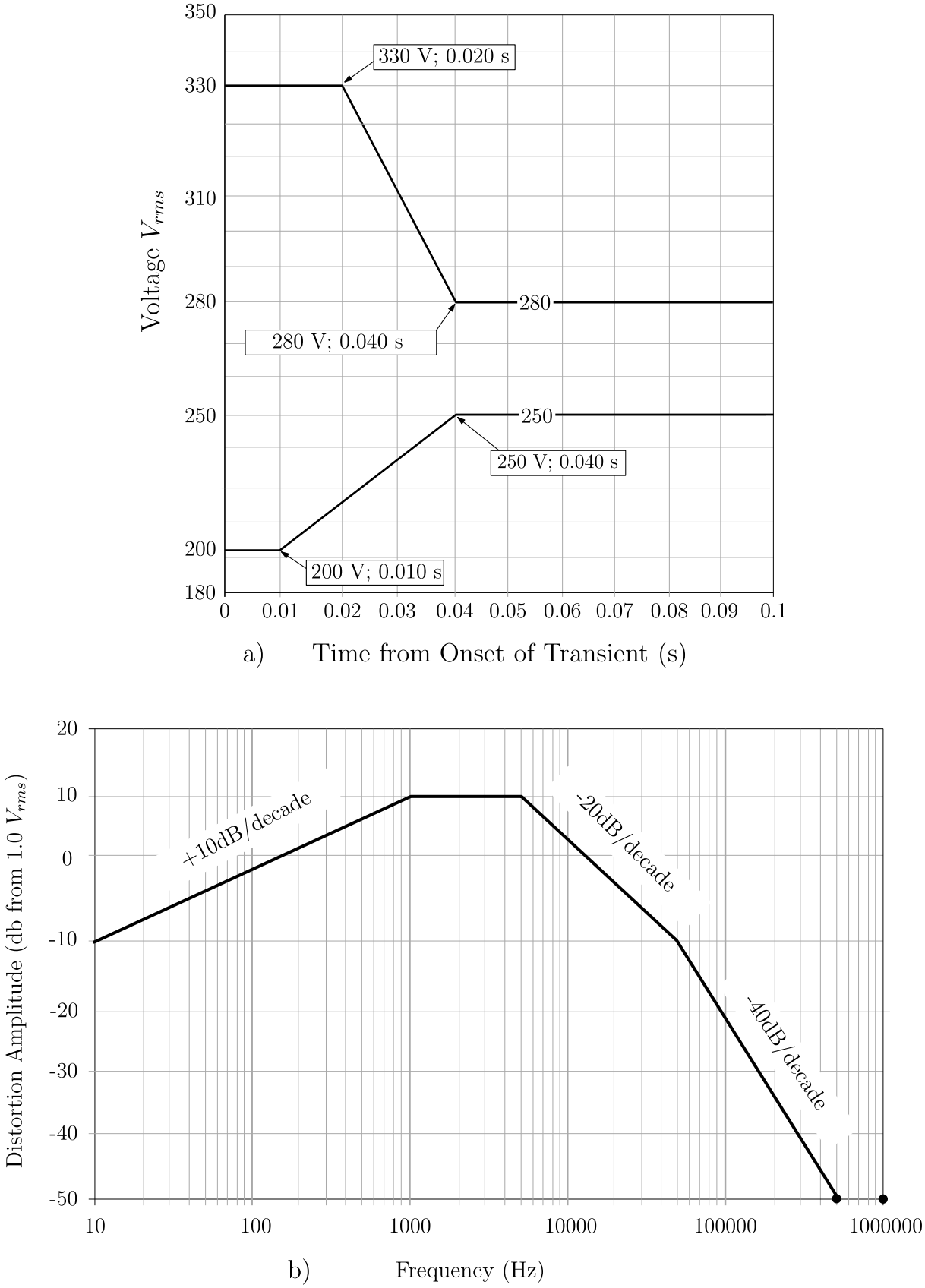


Figure 1.4 – dc limits: a) Envelope of normal voltage transient for 270 V dc system; b)Maximum distortion spectrum of 400 Hz for 270 V dc system ;

1.3 shows the current harmonic limits for a Balanced three-phase equipment. The test conditions established in this standard foresees that the equipment be tested in more severe conditions than those guaranteed by the STD-704F standard, with the objective of ensuring the proper functioning in any situation considered acceptable for the internal bus

Table 1.2 – Current Harmonic Limits for Single-phase Electrical Equipment.

Harmonic Order	**Limits**
Odd Non Triplen Harmonics (5, 7, 11, 13,. . . , 37)	$I_H = 0.3 * I_1/h$
Odd Triplen Harmonics (3, 9, 15, 21, ..., 39)	$I_H = 0.15 * I_1/h$
Even Harmonics 2 and 4	$I_H = 0.01 * I_1/h$
Even Harmonics > 4 (6, 8, 10, ..., 40)	$I_H = 0.0025 * I_1$

Table 1.3 – Current Harmonic Limits for Balanced Three-phase Electrical Equipment.

Harmonic Order	**Limits**
3^{th},5^{th},7^{th}	$I_3 = I_5 = I_7 = 0.02 * I_1$
Odd Triplen Harmonics (9, 15, 21, ..., 39)	$I_H = 0.1 * I_1/h$
11^{th}	$I_{11} = 0.1 * I_1$
13^{th}	$I_{13} = 0.08 * I_1$
Odd Non Triplen Harmonics 17, 19	$I_{17} = I_{19} = 0.04 * I_1$
Odd Non Triplen Harmonics 23, 25	$I_{23} = I_{25} = 0.03 * I_1$
Odd Non Triplen Harmonics 29, 31, 35, 37	$I_H = 0.3 * I_1/h$
Even Harmonics 2 and 4	$I_H = 0.01 * I_1/h$
Even Harmonics > 4 (6, 8, 10, ..., 40)	$I_H = 0.0025 * I_1$

1.3 Dissertation outline

With the implementation of MEA concept, the number of electric and electronic devices in aircraft architecture has grown significantly, and their dynamic interactions have become more complex [16] . As a consequence, complying with the power quality standards has become a challenge in MEA systems. Especially in the dc bus, current unbalance that occurs due to unbalanced loads can unbalance the voltage in bipolar dc bus. A dc redistributor is an electronic device that shall be able to mitigate unbalanced currents restoring the voltage balance [21], [22].

This thesis objective is the study of bipolar dc buses under unbalanced loads at the aircraft environment. The bipolar dc buses shall be able to comply with the aircraft Standards. The specific objectives are the development of a mathematical dynamic model

for the current redistributor used as Power Electronic Conditioner (PEC), the study of control strategies for this aircraft electrical environment and the validation by simulation.

This PEC is based on a dc-dc bidirectional converter and must deal with the current unbalance between the positive and negative poles of the DC bus to comply with the standards. A mathematical dynamic model and control of PEC were simulated in the software PSIM™ for validation.

Sadly, the experimental validation was compromised due to the Corona pandemic. The general access to the School of Electrical and Computer Engineering (FEEC) was prohibited on march, 2020. Future experimental results shall be carried out and confirm the effectiveness of the current redistributor.

Chapter 2 introduces the aircraft electric dc bus, the Electric Power Conditioner and presents some dc Redistributors topologies and their differences and applications. Chapter 3 discusses the modeling, analysis of the dc Redistributor topology. Finally, Chapter 4 presents some control design and simulation results of the proposed redistributor and its interaction with dc bus unbalanced loads .

2 Dc Bus and Power Electronic Conditioner

The usual topology to generate the bipolar DC bus in a aeronautic electric power system is a Transformer Rectifier Unit (TRU) consisting of one or more diode multipulse (12 or more pulses) rectifiers due to the harmonics restrictions, mainly the 3th, 5th and 7th harmonic components [23], [24], [25], [26], [27].

Figure 2.1 shows a simplified model of the dc bus [22]. This model has the presence of lumped loads in the bipolar dc bus. If unbalanced loads are present on the bipolar dc bus, the effective cancellation of the 5th and 7th harmonic components on the the rectifier ac side will not occur due to the current unbalance in the TRU.

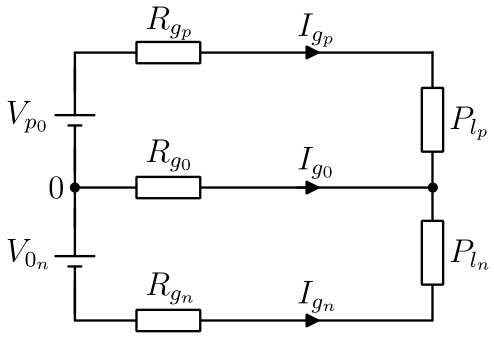


Figure 2.1 – Simplify Circuit of dc bus with lumped power loads.

For the 540 V dc bus, with +/- 270V symmetric voltages, a 12-pulse diode rectifier can be a reasonable solution once it has no-actives elements, simple structure and an ac harmonic content that can be limited to comply with the standard. Although, it does not allow the dc voltage regulation [23] [28]. While it is relatively simple to calculate a dc filter to achieve compliance with standards from a constant frequency ac input, it does not hold true with variable frequency input, which makes it more complex or even impossible to properly regulate the dc voltage [29].

The PWM-rectifiers are an alternative solution due to their high efficiency[30], [31], high power factor and low harmonic content [22]. Although the control system is more complex [25], [32], [33], [34] .

Figure 2.2 shows a 270-V bipolar dc bus consisting of a 12-pulse rectifier system with LC output filter built by the series connection of two 6-pulse diode rectifier [23], [35] to generate the +/- 270 V symmetric voltages. The transformer that feeds the rectifier

has two secondary windings, one star connected and the other a delta connected [36]. This effective cancellation of the 5th and 7th harmonics under balanced loads and equal currents in each bridge is an advantage of such implementation. However, unbalanced dc loads will result different currents at each bridge, and the effective cancellation of the 5th and 7th harmonies does not occur on ac side of the rectifier and may lead to the violation of the standard DO160F.The ac inductances are determined for reducing the high order harmonics, to achieve compliance with the standard.

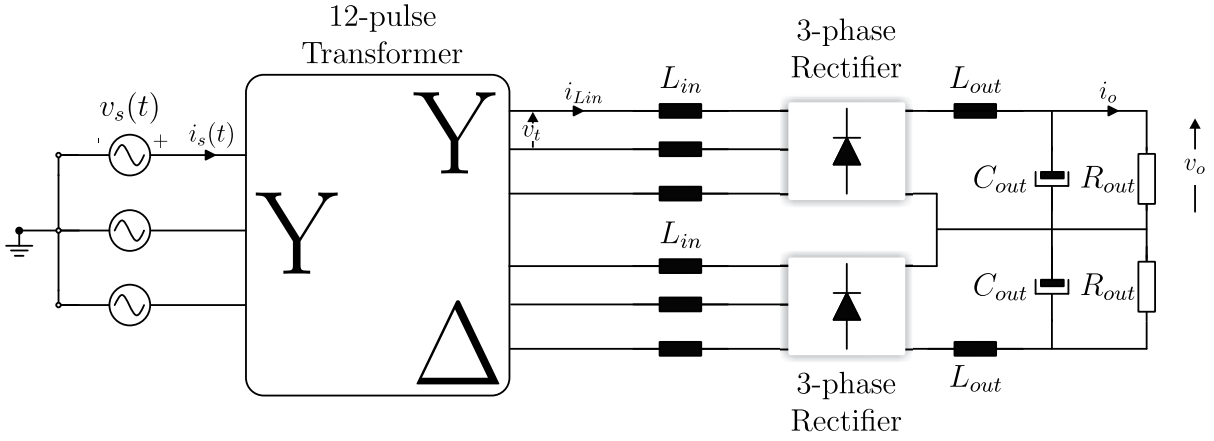


Figure 2.2 – 12-pulse transformer system with LC output filter.

Figure 2.3 shows a PWM-rectifier with double dc output [37]. This PWM rectifier is based on a three-phase controlled bridge. The control of individual dc voltages is necessary in case of unbalanced loads. Due to the aircraft standards, both the ac side (center of the star) and the dc side (intermediate potential) must be connected to the aircraft structure that it offers as a "ground reference" [38],[37]. This converter is able to control the total dc voltage, but not each one of the bipolar outputs. In case of unbalanced load, the dc capacitor voltages change proportionally to the inverse of its respective dc power output, while the converter guarantees the sum of both voltages.

The main drawback in case of unbalanced dc loads is the is that the attempt to balance the voltages leads to the appearance of a dc level in the currents on the ac side, with an unacceptable impact on the operation of the entire ac system, especially on the airplane's generator.

Although the dc current may not propagate when multipulse diode rectifiers are deployed, PWM rectifiers in aircraft systems do not include an isolation transformer due to its excessive weight. Therefore, there is no way to block the propagation of such a dc level to the generator. It is concluded that such an imbalance has to be eliminated at

its origin, what means, at the dc side. [37].

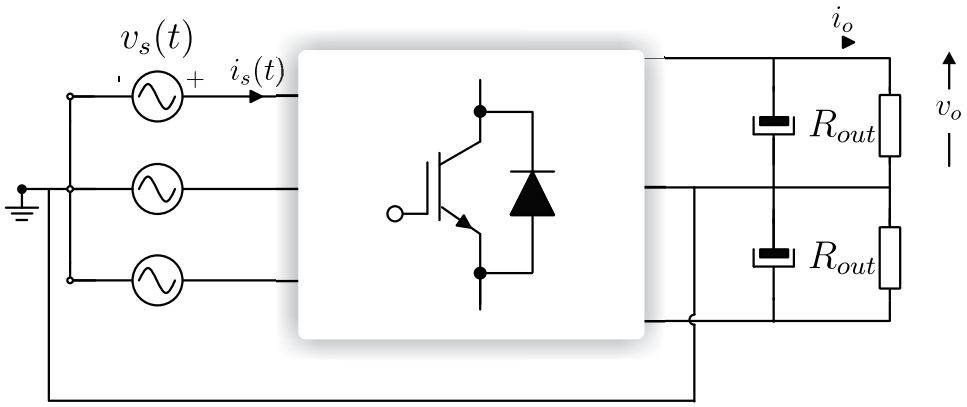


Figure 2.3 – PWM rectifier with double dc output.

2.1 The presence of CPL in the Aircraft system

The aircraft electric system has become more complex and larger with multiple actuators, loads and bus geometries [39] due to the inclusion of power electronics converters in the MEA concept.

This presence of multiple power converters in the grid, with the respective control structures, impacts the stability of the complete grid. Many of these converters behave as constant power loads (CPL), which means they absorb a higher current when the input voltage decreases and vice-versa. The result is a dynamic characteristic expressed by an incremental negative resistance[39].

Figure 2.4 shows the ideal CPL curve and its characteristic as a negative resistance. Therefore, the study of the system stability is necessary to guarantee the stable operation.

Figure 2.5 shows an example of CPL, a dc/dc voltage regulator feeding electrical loads. The input power of the dc/dc converter is constant due to the output voltage regulation for each operating point.

Figure 2.6 shows another example of CPL, a dc/ac converter feeding a Permanent Magnetic Synchronous Motor (PMSM), under speed control. In steady state, the controller regulates the speed of the PMSM at a given operating point. Thus, the torque is constant and the system behave as a CPL.

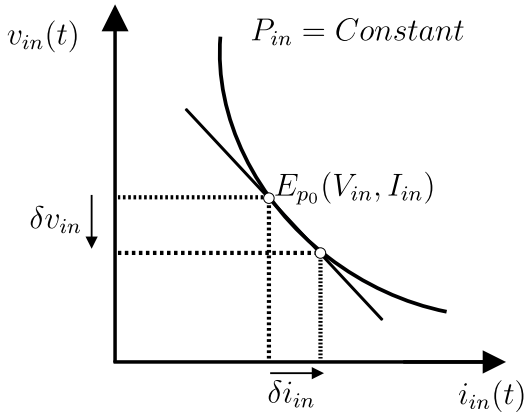


Figure 2.4 – Ideal CPL characteristic curve.

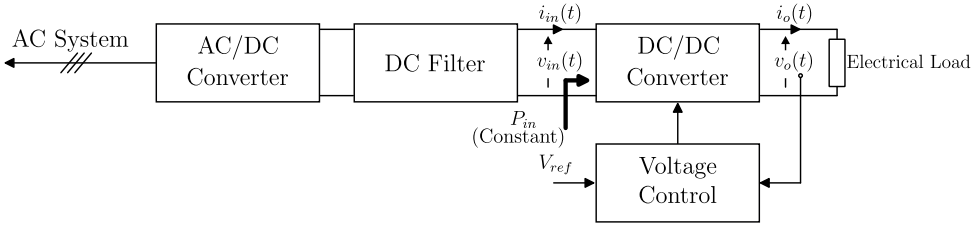


Figure 2.5 – A dc regulator operating as a CPL to the ac System.

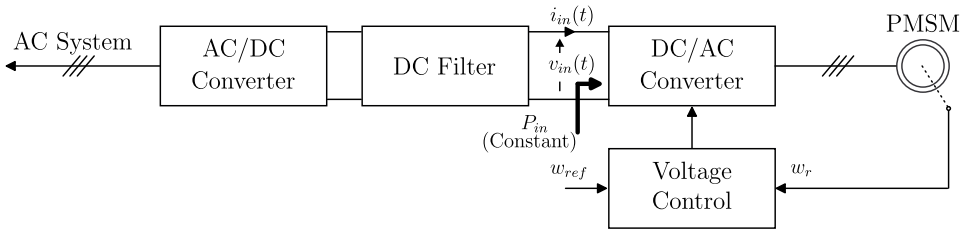


Figure 2.6 – A dc/ac converter operating as a CPL to the ac System.

The ideal CPL in steady state can be represented as a controlled current source, as shown in figure 2.7 [40]. The stability analysis is based in the interacting of the DC filter output impedance and the input impedance of CPL. The negative dynamic behavior shall cause oscillation and instability of the system [20]. Therefore, the impedance ratio of Z_o and Z_i must have no roots in the right half-plane.

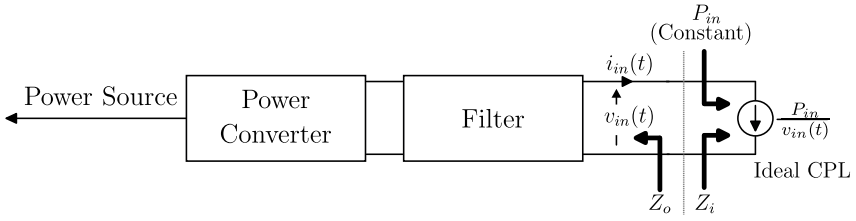


Figure 2.7 – Ideal CPL in steady state operation.

2.2 Power Electronic Conditioners

A Power Electronic Conditioner (PEC) is able to modify electrical characteristics of a power grid acting in its waveform of current or voltage. The purpose of using a PEC is the mitigation of voltage perturbation, the increase of the power capability and controllability [39],[41], and grid disturbances: blackouts, sags and harmonic distortion. Some examples of PECs topologies in the ac grid are: Static Var Compensator-SVC, STATCOM and Active Power Filter – APF [14],[15],[42],[43], [44].

2.2.1 DC Power Electronic Conditioner

The focus of this project is to investigate a PEC for dc bus in MEA. The dc PEC is called Current Redistributor Converter (CR). Figure 2.8 shows a CR, which is the structure chosen for balancing the bipolar currents, i_{g_p} and i_{g_n}, in the dc bus [30]. The CR is also known as current equalizer. The function of this PEC is to make the current at the positive and negative terminals equal, canceling the neutral current, regardless of the loads. A path is created through the PEC capable of making such a balance.

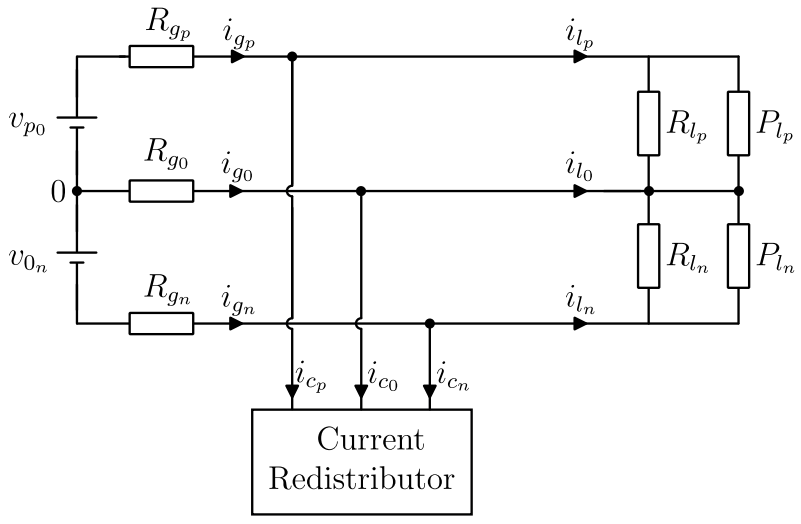


Figure 2.8 – Bipolar dc bus architecture including a CR and lumped loads.

Considering the multipulse rectifier and the PWM rectifier for the TRU topology, the CR is necessary for different reasons. For the 12-pulse diode rectifier, the dc voltages are balanced by the connection of the rectifiers. However, in case of unbalanced load the expected 5th and 7th harmonic cancellation is lost. For the PWM rectifier the main problem is the dc voltage unbalance, since the rectifier is able to regulate only the total voltage.

2.3 Basic dc Redistributor Topologies

The CR main aim is to equalize the currents on the positive and the negative dc outputs. Therefore, it is advantageous that the CR behaves as a controlled current source. As already explained, the current equalization allows a 12-pulse rectifier to comply with the ac side harmonic limitation. Considering the TRU based on the PWM rectifier, the equalization of the positive and negative branches currents balances the dc bus capacitor voltages. The dc-dc converters shown in figure 2.9 can operated as a CR. Additionally, it would be useful if the CR performs other functions as:

(i) Voltage regulation;

(ii) Active damping;

(iii) Absorbing regenerate energy from loads;

(iv) Interface with dc energy storage (battery bank and super-capacitors) [30] ;

(v) it can operate with loss of one dc line [30];

The simple bidirectional buck-boost converter topology shown in figure 2.9a is the simplest topology able to redistribute the current in the DC bus containing only one inductor and two transistors [22]. In case of PWM rectifier, voltage balancing is achieved simply by imposing a 50% duty cycle. The current (positive or negative) will flow in order to compensate for load imbalances. It is an arrangement that can, in principle, operate in open loop, although some type of overcurrent protection should be provided. The main drawback is the pulsed nature of the currents imposed on the dc bus, with potential problems with electromagnetic interference. In case of 12-pulse rectifier, in which there's no voltage unbalance, the goal is to equalize the currents. In this case the it's necessary to control the currents in order to null the neutral point current. Additionally, this topology is not capable of executing the other indicated characteristics, except for the last one, since, operating as a bidirectional buck-boost converter in continuous mode, it is possible to form one of the busbars.

The boost converter shown in 2.9b is able to perform not only the current balance but also the (i), (ii), (iii) functions in the dc bipolar network. The internal dc bus can operate with only a capacitor, which the control acts to regulate the voltage. This

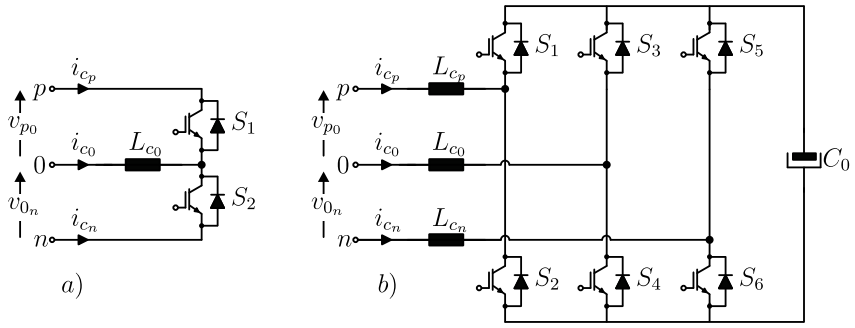


Figure 2.9 – dc-dc converters that can operated as a CR.

voltage is higher than the one at the dc bus due to the boost configuration. In this case, it isn't possible to inject active power in the external bus. However, if there is a source (such as a battery bank or a supercapacitor) in the inner dc bus, this topology may inject power or absorve power from the external bus. Usually, an inductive filter is connected to the battery bank to reduce the current ondulation.

In this work, this boost converter is the chosen dc redistribuitor topology.

3 DC Redistributor topology: Modeling and analysis

This chapter shows the discussion of the theoretical model that have been proposed in [22].The converter works with pulse width modulation (PWM), and switching frequency, f_s. The duty cycles depend on the ratio of the internal dc voltage, V_0, and dc link voltage as shown by Eq. 3.1.

In steady state, with dc bus symmetrical voltages, $V_{p_0} = V_{0_n} = V_{p_n}/2$, as a boost converter, the internal dc voltage V_0, is higher than the maximum external voltage $V_{p_0} + V_{0_n}$. For higher V_0, The CR performs faster when compensating the disturbances on the dc bus. The central line duty cycle is chosen arbitrary $D_o = 1/2$, and the upper and lower line duty cycles are represented by Eq. 3.2 and Eq. 3.3 and their variation is around the 0.5. Eq. 3.4 shows their relation.

$$D_\delta = \frac{V_{p_n}}{2V_0} \tag{3.1}$$

$$D_p = \frac{1}{2} + D_\delta \tag{3.2}$$

$$D_n = \frac{1}{2} - D_\delta \tag{3.3}$$

$$D_p - D_0 = D_0 - D_n = D_\delta = \frac{V_{p_n}}{2V_0} \tag{3.4}$$

3.1 Current model

Figure 3.1 shows the equivalent model of the dc redistributor topology. The transistors and diodes can be represented as single switches with two positions. In the following equations, the subscript x represents either p, 0 or n. Eq. 3.5 and Eq. 3.6 show the commutation function $s_x(t)$ and the voltage between the switches and the reference

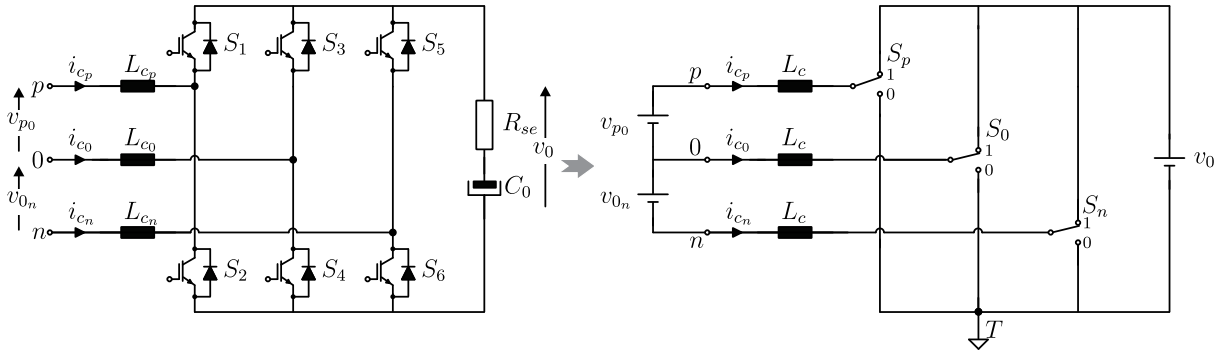


Figure 3.1 – The chosen dc redistributor topology.

T. When $s_x = 1$ (S_x is in position 1) the voltage v_{x_T} assumes v_o, when $s_x = 0$ (S_x is in position 0) the voltage v_{x_T} assumes 0.

$$s_x(t) = \begin{cases} 1, & S_x \text{ is on} \\ 0, & S_x \text{ is off} \end{cases} \tag{3.5}$$

$$v_{xT} = s_x v_o \tag{3.6}$$

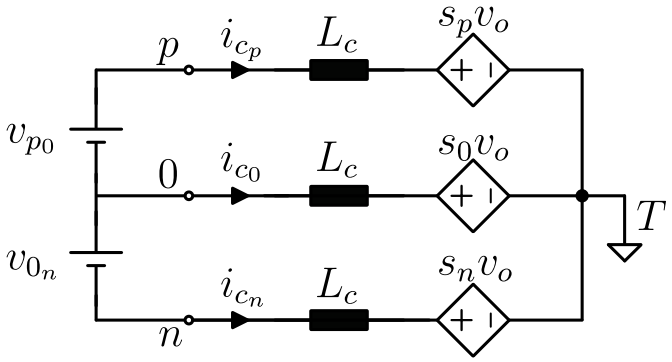


Figure 3.2 – Model for instantaneous values.

Applying the quasi-instantaneous average definition, Eq. 3.7, in the model variables and linearizing, it is obtained the equilibrium point model shown in Figure 3.3. Figure 3.4 shows the steady state operation point of the converter.

Eq. 3.8 shows the quasi-instantaneous value of the commutation function known as duty cycle. It is composed by the D_x, steady state value, and the perturbation $\hat{x}$, as shown in Eq. 3.9.

$$\bar{x} = \langle x \rangle_{T_s} = \int_{\tau - T_s}^{\tau} x(t)dt \tag{3.7}$$

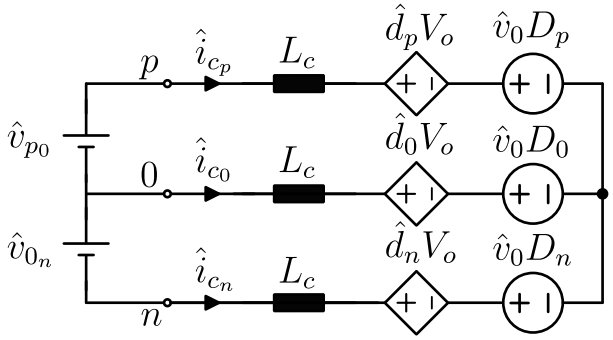


Figure 3.3 – Equilibrium point model

$$d_x = \langle s_x(t) \rangle_{T_s}, \qquad 0 \leq d_x \leq 1 \tag{3.8}$$

$$\begin{cases} d_0 = D_0 + \hat{d}_0 \\ d_p = D_p + \hat{d}_p \\ d_n = D_n + \hat{d}_n \end{cases} \tag{3.9}$$

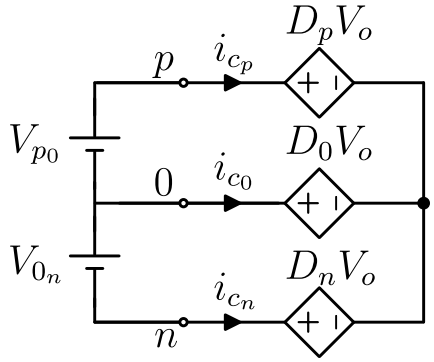


Figure 3.4 – Steady state operation point.

Applying Kirchhoff law in the figure 3.3, the voltages $\hat{v}_{p_0}$ and $\hat{v}_{0_n}$ are describe in the Eq. 3.10 and Eq. 3.11.

$$\begin{aligned} \hat{v}_{p_0} &= v_{L_c} + \hat{d}_pV_o + \hat{v}_0D_p - \hat{v}_0D_0 - \hat{d}_0V_o - v_{L_c} \\ &= V_o(\hat{d}_p - \hat{d}_0) + \hat{v}_0(D_p - D_0) \end{aligned} \tag{3.10}$$

$$\begin{aligned} \hat{v}_{0_n} &= v_{L_c} + \hat{d}_0V_o + \hat{v}_0D_0 - \hat{v}_0D_n - \hat{d}_nV_o - v_{L_c} \\ &= V_o(\hat{d}_0 - \hat{d}_n) + \hat{v}_0(D_0 - D_n) \end{aligned} \tag{3.11}$$

The $\hat{i}_{c_p}$ and $\hat{i}_{c_n}$ currents are dependent due to the inductor in the central leg. If this inductance were zero, the current through the positive or negative grid would depend only on the respective inductances. However, with the presence of inductance in the central branch, there is an interaction between both currents, changing the total voltage in the mesh and, consequently, making them dependent on each other. A decoupling method is then applied to allow independent control of the redistributor currents.

3.1.1 Current decoupling method

In a dc symmetrical bus, one of the independent duty cycles can be chosen arbitrary, as mentioned before. To obtain the decoupling system, the superposition method must be apply.

Let $\hat{d}_p \neq 0$, $\hat{d}_n = 0$ and $\bar{\hat{i}}_{c_n} = 0$. Figure 3.5 shows the equivalent circuit obtained from it. To satisfy $\bar{\hat{i}}_{c_n} = 0$, the central leg duty cycle must follow Eq. 3.12.

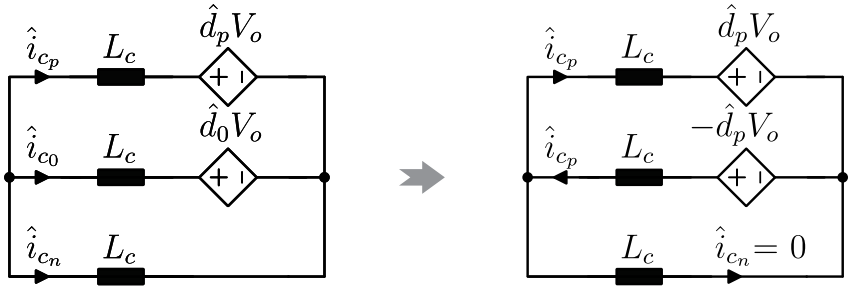


Figure 3.5 – Upper leg decoupling circuit.

$$\hat{d}_0 = -\hat{d}_p \tag{3.12}$$

Now, let $\hat{d}_n \neq 0$, $\hat{d}_p = 0$ and $\bar{\hat{i}}_{c_p} = 0$. Figure 3.6 shows the equivalent circuit obtained from it. To satisfy $\bar{\hat{i}}_{c_p} = 0$, the central leg duty cycle must follow Eq. 3.13.

$$\hat{d}_0 = -\hat{d}_n \tag{3.13}$$

The perturbation is the result of the superposition. Therefore, Eq. 3.14 shows the pattern of perturbation.

$$\hat{d}_0 = -\hat{d}_p - \hat{d}_n \tag{3.14}$$

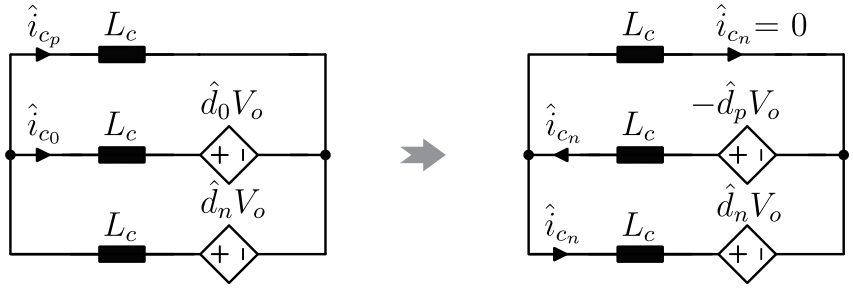


Figure 3.6 – Lower leg decoupling circuit.

Using the Eq. 3.14, d_0 can be described as shown in Eq. 3.15.

$$d_0 = (D_p + D_n + D_0) - d_p - d_n \tag{3.15}$$

Replacing $\hat{d}_0$ in Eq. 3.10 and Eq. 3.11, the voltages $\hat{v}_{p_0}$ and $\hat{v}_{0_n}$ can be described in the Eq. 3.16 and Eq. 3.17. Figure 3.7 shows the decoupling circuit.

$$\hat{v}_{p_0} = V_o(2\hat{d}_p + \hat{d}_n) + \hat{v}_0(D_p - D_0) \tag{3.16}$$

$$\hat{v}_{0_n} = V_o(-\hat{d}_p - 2\hat{d}_n) + \hat{v}_0(D_0 - D_n) \tag{3.17}$$

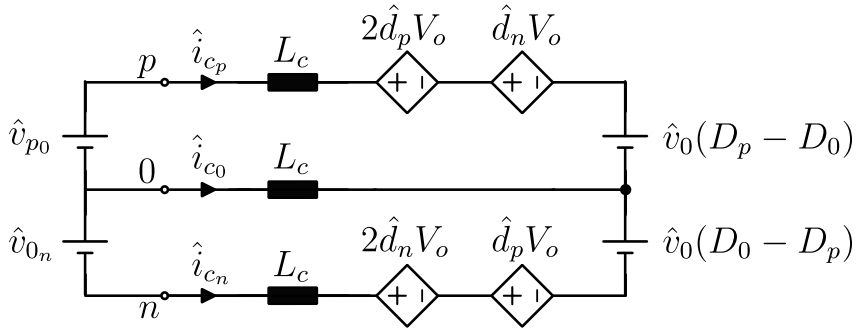


Figure 3.7 – Decoupling circuit.

Considering the bus voltage as perturbation, the transfer function of the upper leg $\hat{i}_{c_p}$ and lower leg $\hat{i}_{c_n}$ are described in Eq. 3.18 e Eq. 3.19, respectively [22].

$$G_{i_{c_p}}(s) = \frac{\hat{i}_{c_p}}{\hat{d}_p} = -\frac{V_o}{sL_c} \tag{3.18}$$

$$G_{i_{c_n}}(s) = \frac{\hat{i}_{c_n}}{\hat{d}_n} = -\frac{V_o}{sL_c} \tag{3.19}$$

3.2 Voltage model

The voltage model of the dc redistributor topology is evaluated in an equivalent way as the current model described in Section 3.1, as shown in Figure 3.8.

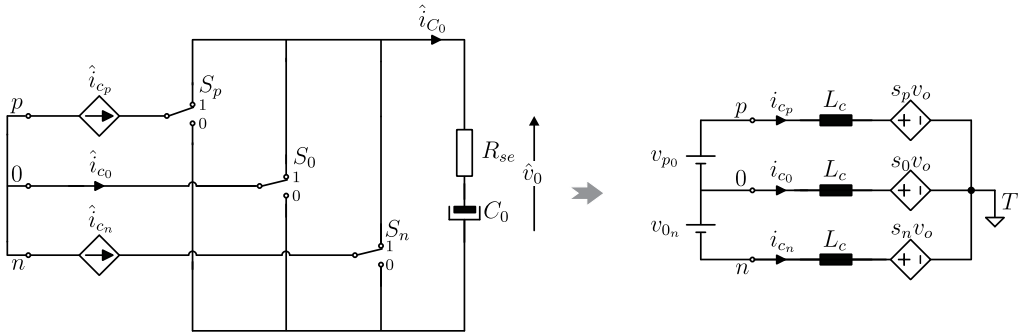


Figure 3.8 – Equivalent voltage model.

Owning to the linear relationship of the dc redistributor currents, $\hat{i}_{c_0}$ can be described as shown in Eq. 3.20 .

$$\hat{i}_{c_0} = \hat{i}_{c_p} - \hat{i}_{c_n} \tag{3.20}$$

Eq. 3.21 evaluates $\hat{i}_{cC_0}$:

$$\begin{aligned} \hat{i}_{cC_0} &= \hat{i}_{c_p} D_p + (-\hat{i}_{c_p} - \hat{i}_{c_n}) D_0 + \hat{i}_{c_n} D_n \\ &= (D_p - D_0)\hat{i}_{c_p} - (D_0 - D_n)\hat{i}_{c_n} \\ &= D_\delta(\hat{i}_{c_p} - \hat{i}_{c_n}) \end{aligned} \tag{3.21}$$

Simplifying the circuit shown in Figure 3.8, the figure 3.9 shows the final circuit.

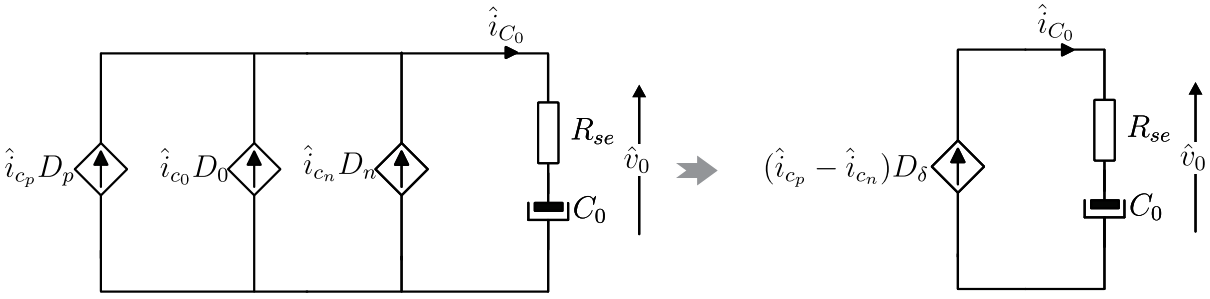


Figure 3.9 – Simplified circuit.

The voltage v_o, shown in Eq. 3.22, is evaluated from the circuit on the right-hand side of Figure 3.9 . Expanding the Eq. 3.22, considering only the perturbation component, the Eq. 3.23 shows the voltage $\hat{v}_o$.

$$\hat{v}_o = \hat{i}_{c_0} Z_c \tag{3.22}$$

$$\hat{v}_o(s) = \frac{V_{p_n}}{2V_o} \frac{(sC_0R_{se}+1)}{sC_o} (\hat{i}_{c_p} - \hat{i}_{c_n}) \tag{3.23}$$

Let the dc differential current be defined by Eq. 3.24 and the dc common mode current be defined by Eq. 3.25.

$$\hat{i}_{c_{dm}} = \frac{\hat{i}_{c_p} - \hat{i}_{c_n}}{2} \tag{3.24}$$

$$\hat{i}_{c_{cm}} = -\frac{\hat{i}_{c_p} + \hat{i}_{c_n}}{2} \tag{3.25}$$

Applying Eq. 3.24 in Eq. 3.23, the transfer function of the voltage model is described in Eq. 3.26.

$$G_v(s) = \frac{\hat{v}_o}{\hat{i}_{c_{dm}}} = \frac{V_{p_n}}{2V_o} \frac{(sC_0R_{se}+1)}{2sC_o} = \frac{D_\delta(sC_0R_{se}+1)}{2sC_o} \tag{3.26}$$

3.3 Conclusion

In this chapter, the current model and the voltage mode of the CR were developed. Firstly, an equilibrium point model was developed to describe the system. Therefore, a current decoupling method was applied due to the dependency of the positive feeder current, $\hat{i}_{c_p}$, negative feeder and $\hat{i}_{c_n}$ currents. Finally, the voltage model of the CR was presented as transfer function of the V_o, and the dc differential current $\hat{i}_{c_{dm}}$. The aim of the chapter was to show a mathematical dynamic model suitable to control the CR. Now, we are able to propose a control system and simulate the dc bus under unbalanced loads.

4 Control system and simulation results

4.1 Control System

Figure 4.16 shows the dc current redistributor proposed control. The references are the current central branch current i^*_{g0}, that must be zero, and the dc bus redistributor voltage v^*_0. The result of the inverse transformation of common and differential mode, ${T_c}^{-1}$, are the upper and lower current references. Next, the decoupling method described in Eq. 3.15 takes place and the duty cycles for the PWM switching are obtained.

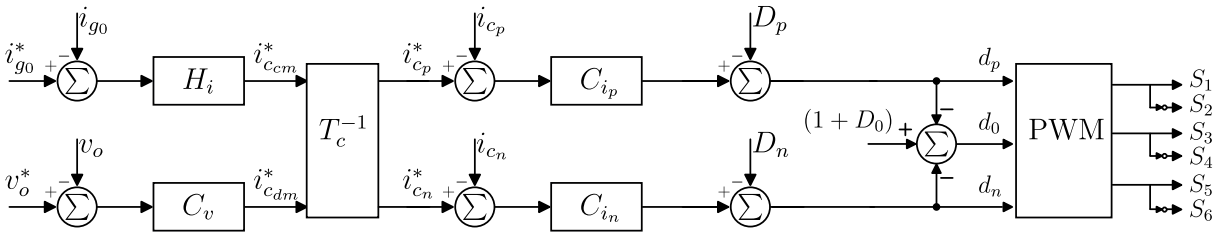


Figure 4.1 – Block Diagram of propose control.

The blocks C_v, C_{i_p}, C_{i_n} correspond to the voltage, upper and lower current controllers, respectively. These controllers are proportional integrator (PI) obtained from the SISOTOOL MATLAB.

4.2 Simulation results

The dc bus voltages are selected to be 270 V.Additionally, the dc redistributor bus voltage is selected to be 800 V. Applying 3.1, 3.2 and 3.3, the central line duty cycle, upper and lower line duty cycles are:

$$D_\delta = \frac{V_{pn}}{2V_0} = \frac{270}{800} = 0.3375 \tag{4.1}$$

$$D_p = \frac{1}{2} + D_\delta = 0.5 + 0.3375 = 0.8375 \tag{4.2}$$

$$D_n = \frac{1}{2} - D_\delta = 0.5 - 0.3375 = 0.1625 \tag{4.3}$$

The input filter resistance R_g, the input filter inductor L_g and the capacitor C_g are selected to be 70 uΩ, 100 uH and 3700 uF. For the simulation, the capacitor C_o is selected to be 2491 uF because the SEMIKRON IGBT module stack available at the laboratory has this internal capacitance.

The switching frequency (f_s) is 10 kHz, which is suitable for this dc bus application. The current cut-off frequency (f_c) should be at least two times lower than the switching frequency in order to achieve the Nyquist criteria. Therefore, the f_c is selected to be 980 Hz, more than ten times lower than the switching frequency.

Table 4.1 shows the basics parameters used for these simulation in PSIM. Fig. 4.2 shows the circuit diagram for the simulation of the aircraft system containing the dc bus, the dc current redistributor and the unbalanced loads, including CPL. The CPL is emulated by an ideal controlled current source.

Table 4.1 – Simulation parameters for dc redistributor.

Parameters	Value
dc bus voltages ($V_{p_0} = V_{0_n}$)	270 V
dc redistributor bus voltage(V_0)	800 V
Positive feeder Load (R_{lp1})	20 Ω
Negative feeder Load (R_{ln1})	20 Ω
Additional negative feeder Load (R_{ln2})	40 Ω
Additional positive feeder Load (R_{ln3})	40 Ω
Power rating of Ideal CPL (w_q)	2000 W
Switching frequency (f_s)	10 kHz
dc redistributor Capacitor (C_o)	2.49 mF
Redistributor Inductor (L_c)	2 mH
Current cut-off frequency (f_c)	998 Hz
Current controller time constant (T_{c_i})	1/1116
Current controller gain (K_{c_i})	0.011156
Voltage controller time constant (T_{c_v})	1/3.721
Voltage controller gain (K_{c_i})	0.41623
Voltage cut-off frequency (f_{c_2})	100 Hz

4.2.1 Dc bus under balanced and unbalanced resistive loads

For these initial simulation results the CR is disable. We want to evaluate the current balancing without the CR. Fig. 4.3 shows the simulation results for a balance load configuration. The dc bus feeds a 20 Ω in the positive and the negative feeder. The top waveform represent the dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}. The middle waveform

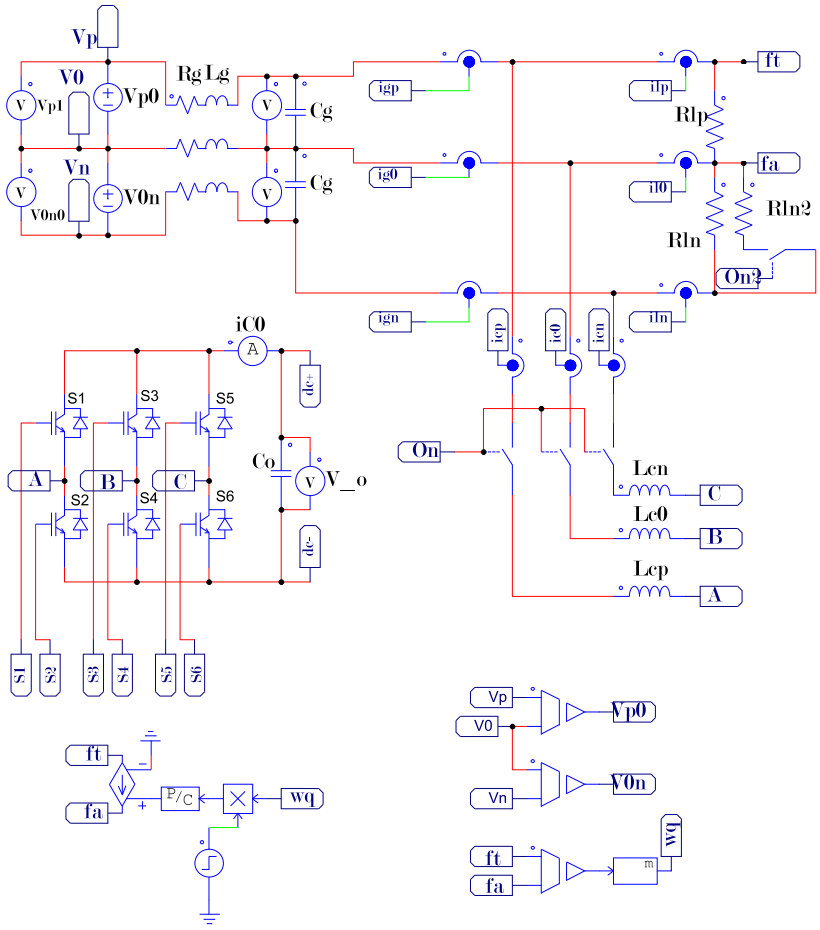


Figure 4.2 – Diagram of the power circuit in PSIM.

represents the positive feeder voltage V_{p0l} at the capacitor C_g and the bottom waveform represents the negative feeder voltage V_{n0l} at the capacitor C_g.

In this situation, the CR is disable and the current flowing in the dc bus grid is balanced, i. e. i_{g_0} is zero and $i_{g_p} = -i_{g_n}$. The positive feeder voltage V_{p0l} and the negative feeder voltage V_{n0l} are both 270 V.

Fig. 4.4 shows the simulation results for a configuration with unbalanced load from t = 1.5s on the negative branch.

Before $t = 1.5\,\mathrm{s}$, the dc bus feeds a $20\,\Omega$ balance load. At $t = 1.5\,\mathrm{s}$, a $40\,\Omega$ load is added in parallel to the negative branch. In this situation, the system is unbalanced. i_{g_0} is different from zero and the relationship between the positive and the negative dc currents, $i_{g_p} = -i_{g_n}$, is not valid. The positive feeder voltage V_{p0l} and the negative feeder voltage V_{n0l} oscillates around 270 V. As said before, the current unbalancing may cause several problems at the overall system. Note that, as the average voltages do not change, the assumption is that the TRU (which forms the +/- 270 V bus) is a 12 pulse diode

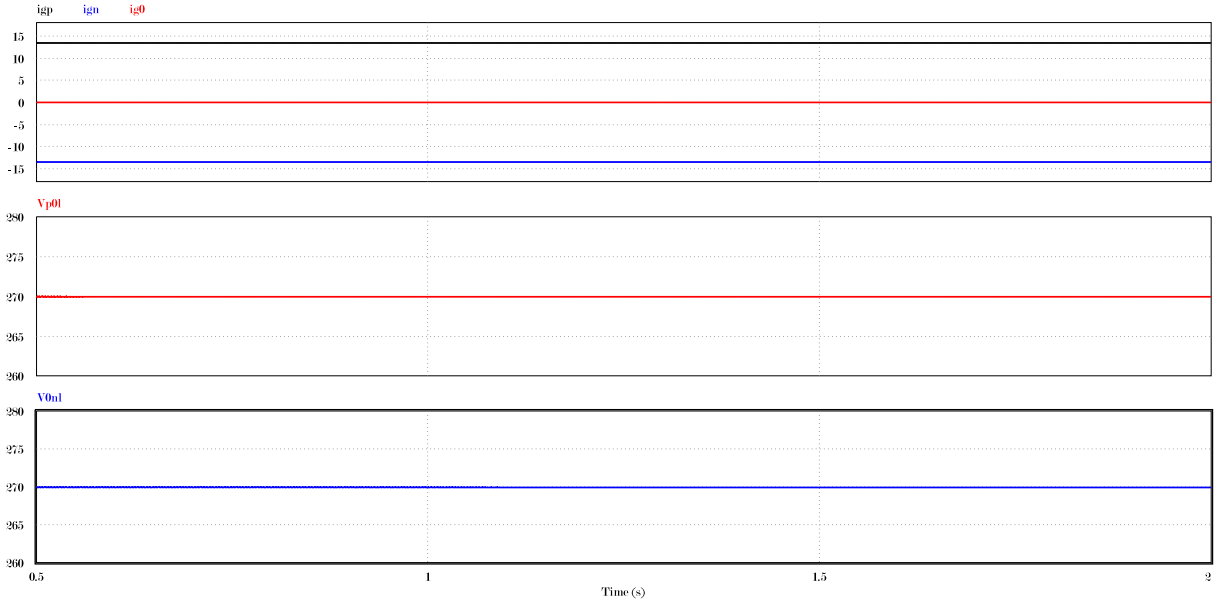


Figure 4.3 – Simulated results from balanced load with the CR disable.

rectifier. For this rectifier, as mentioned, the effective cancellation of fifth and seventh harmonics occurs only in case of equal currents in the positive and negative buses.

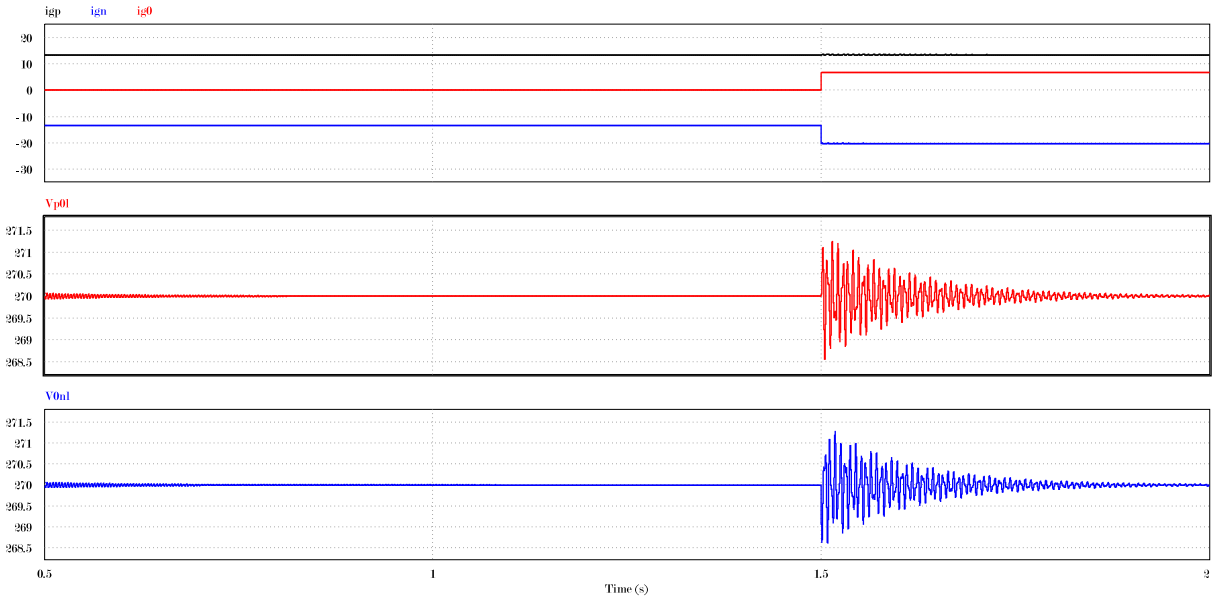


Figure 4.4 – Simulated results from a unbalanced negative feeder load.

Fig. 4.5 shows the simulation results for a configuration with unbalanced load at t=1.5s on the positive branch.

Before $t = 1.5\,\mathrm{s}$, the dc bus feeds only a $20\,\Omega$ balance load. At $t = 1.5\,\mathrm{s}$, a $40\,\Omega$ load is added to the positive branch. In this situation, the system is unbalanced. i_{g_0} is different from zero and the relationship between the positive and the negative dc currents, $i_{g_p} = -i_{g_n}$, is not valid. The positive feeder voltage V_{p0l} and the negative feeder voltage

V_{n0l} oscillates around 270 V.

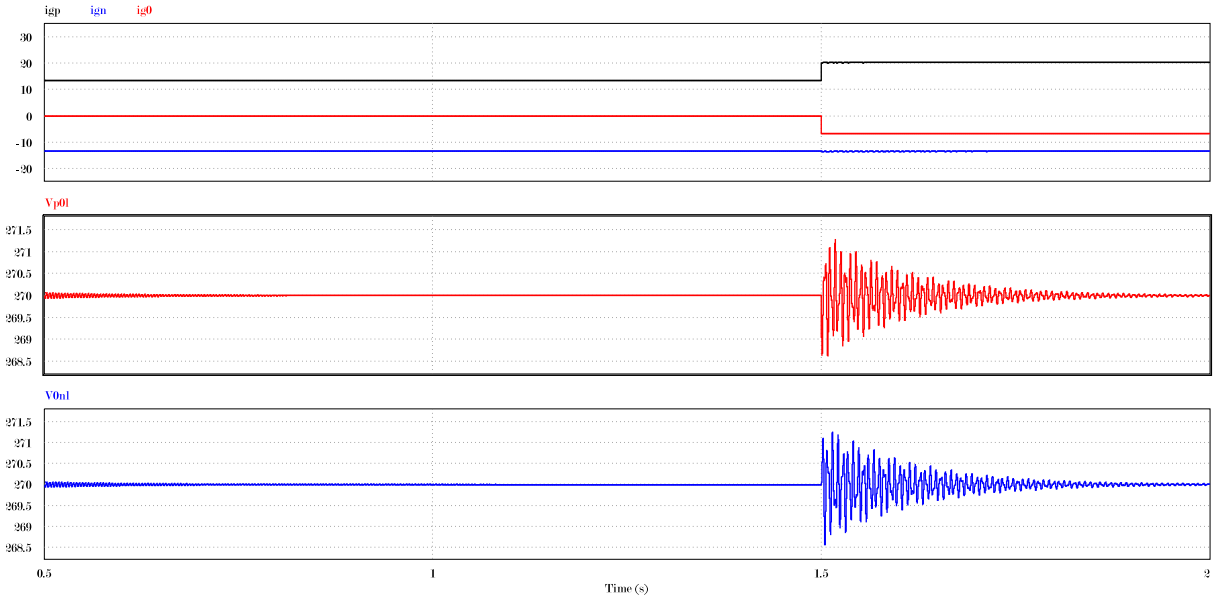


Figure 4.5 – Simulated results from a unbalanced positive feeder load.

Fig. 4.6 shows the simulation results for a series of load step changes occurring on both negative and positive branch. Before $t = 0.6\,\mathrm{s}$, the dc bus feeds only a $20\,\Omega$ balance load. At $t = 0.6\,\mathrm{s}$, a $40\,\Omega$ load is added to the negative branch. In this situation, the system is unbalanced. As said before, i_{g_0} is different from zero and the relationship between the positive and the negative dc currents, $i_{g_p} = -i_{g_n}$, is not valid. At $t = 1.2\,\mathrm{s}$, a $20\,\Omega$ load is added to the positive branch. At $t = 1.8\,\mathrm{s}$, a $30\,\Omega$ load is added to the 570 V dc bus not changing the i_{g_0} current.

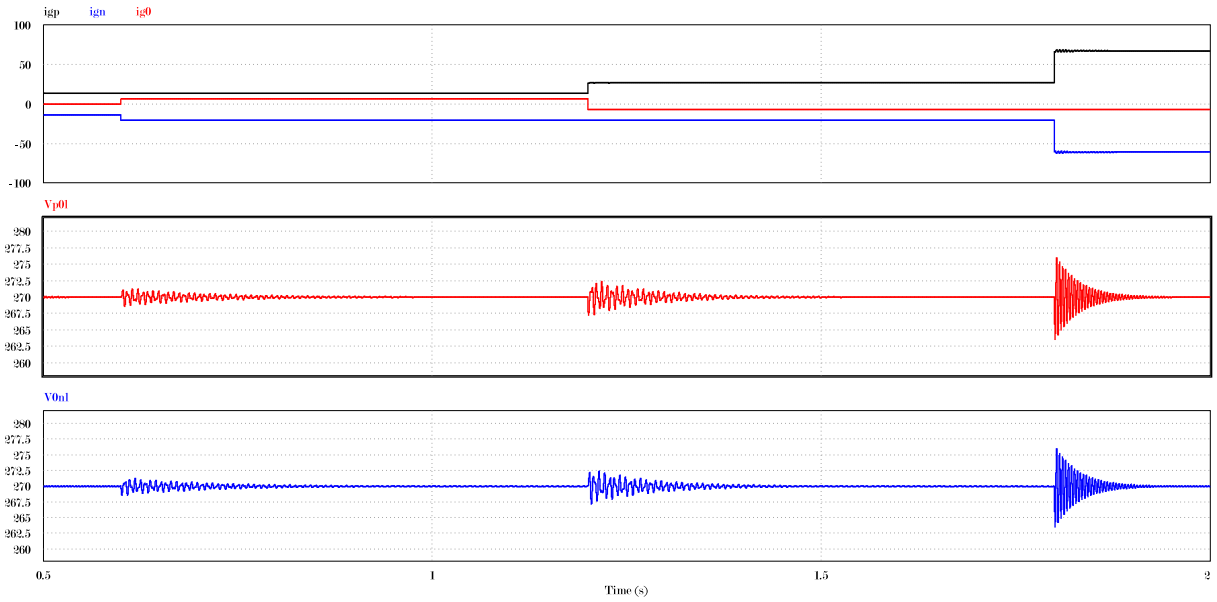


Figure 4.6 – Simulated results from am unbalanced positive and negative feeder loads.

Now, we will analyse the system with the CR. As said before, the CR must deal with this current unbalancing in the system.

4.2.2 Dc bus and CR simulation

Fig. 4.7 shows the simulation results for a configuration with unbalanced load at t=2 s and t=3 s on the negative branch. The top waveforms represent the dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}. The middle waveforms represent the dc CR inner voltage V_0 and its reference, V_{0ref}. The bottom waveforms represent the positive feeder voltage V_{p0l} at the capacitor C_g and the negative feeder voltage V_{n0l} at the capacitor C_g.

Before $t = 2\,\mathrm{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates. At $t = 2\,\mathrm{s}$, a $40\,\Omega$ load is added to the negative branch. In this situation the system has unbalanced loads connected, however the dc redistributor adjusts the current flowing in the dc bus grid. i_{g_0} remains zero and i_{g_p} and i_{g_n} are balanced, i.e. $i_{g_p} = -i_{g_n}$. At $t = 3$ s, an extra $20\,\Omega$ parallel load is added to the negative branch. The dc redistributor keeps the balance between i_{g_p} and i_{g_n}. At both $t = 2\,\mathrm{s}$ and $t = 3\,\mathrm{s}$, the voltage controller keeps v_0 to its reference.

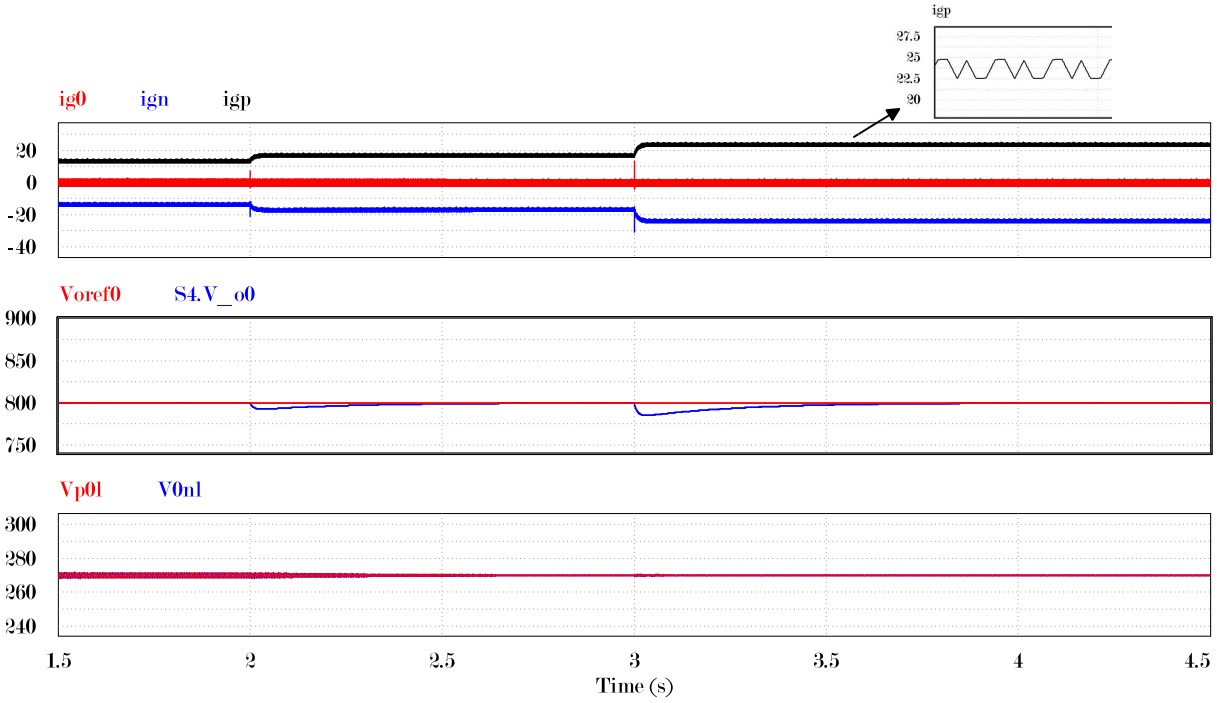


Figure 4.7 – Simulated results from different loads

Fig. 4.8 shows the simulation results for a configuration with unbalanced load at t=2.5 s and t=3.5 s on the positive branch.

Before $t = 2.5\,\text{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates. At $t = 2.5\,\text{s}$, a $40\,\Omega$ load is added to the positive branch. In this situation the system has unbalanced loads connected, however the dc redistributor adjusts the current flowing in the dc bus grid [21]. i_{g_0} remains zero and $i_{g_p} = -i_{g_n}$. At $t = 3.5$ s, an extra $20\,\Omega$ parallel load is added to the positive branch. The dc redistributor keeps the balance between i_{g_p} and i_{g_n}. At both $t = 2.5\,\text{s}$ and $t = 3.5\,\text{s}$, the voltage controller keeps v_0 to its reference.

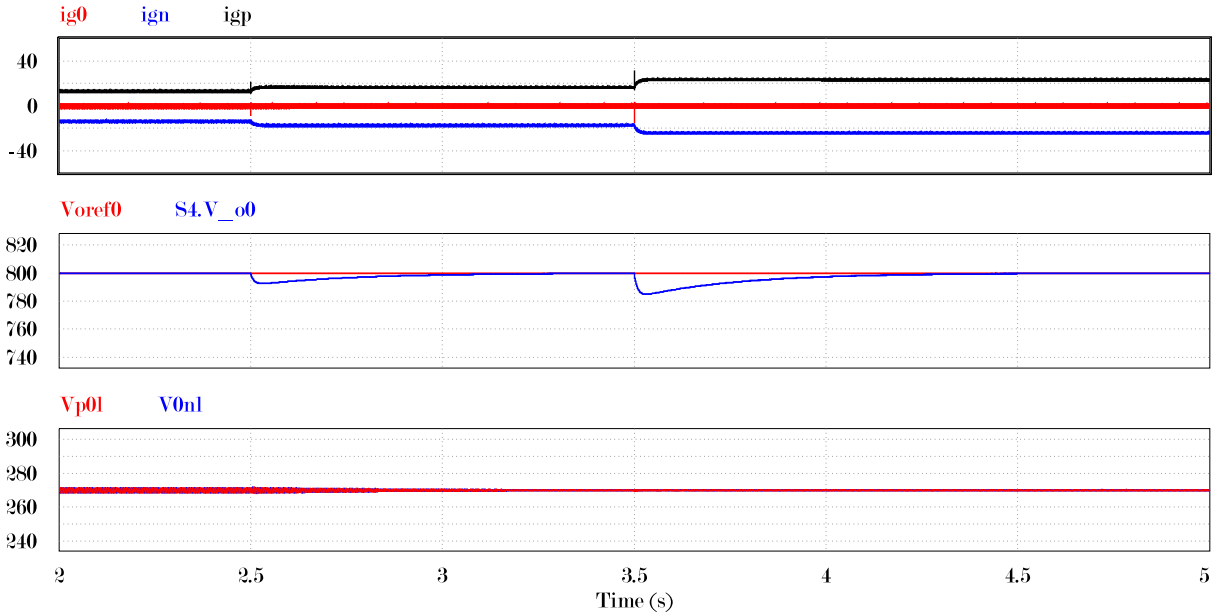


Figure 4.8 – Simulated results from different positive unbalanced loads

We can also evaluate the CR capability of regulating the dc capacitor voltage under a change of reference. Fig. 4.9 shows the simulation results for a step change on the inner voltage reference under balanced loads at the system. At $t = 5\,\text{s}$, the dc capacitor voltage reference changes to $750\,\text{V}$ and at $t = 5.5\,\text{s}$, the inner voltage reference returns to $800\,\text{V}$. The dc CR is able to regulate the inner CR voltage at its new reference.

Additionally, the capability of the CR to regulate its dc capacitor voltage when loads are unbalanced at the positive and negative branches of the dc bus.. Fig. 4.10 shows the simulation results. Before $t = 3.5\,\text{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates. At $t = 3.5\,\text{s}$, a $40\,\Omega$ load is added to the negative branch. The dc redistributor adjusts the current flowing in the dc bus grid. i_{g_0} remains zero and $i_{g_p} = -i_{g_n}$. Moreover, at $t = 5\,\text{s}$, the inner voltage reference goes to $750\,\text{V}$ and at $t = 5.5\,\text{s}$, the inner voltage reference goes to $800\,\text{V}$.

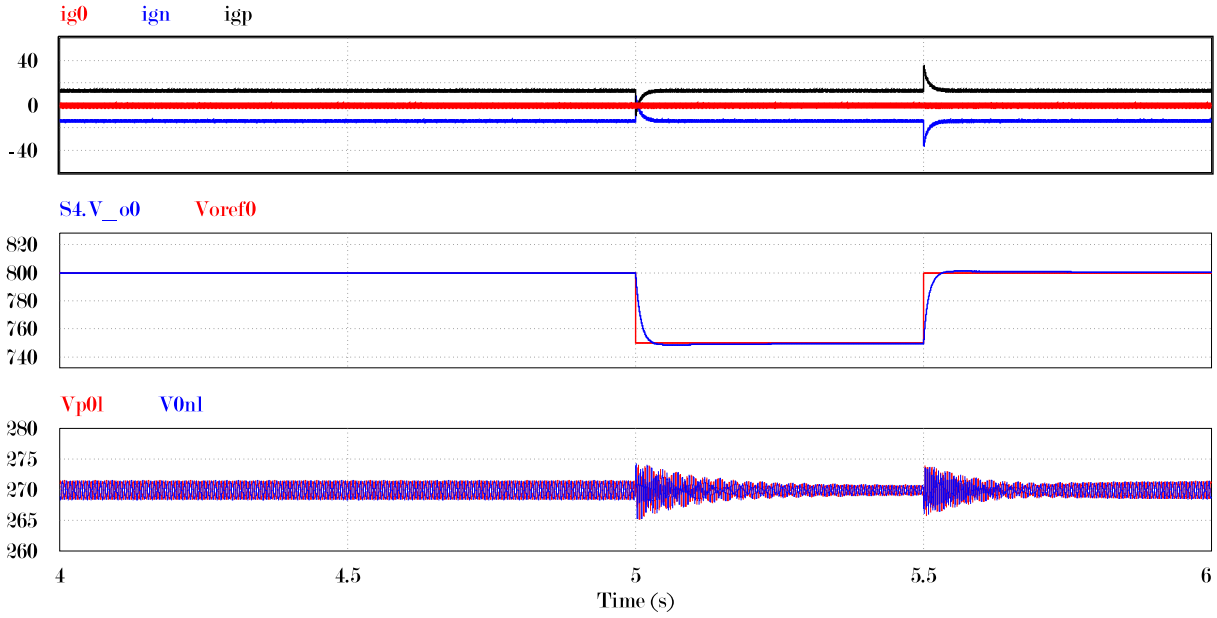


Figure 4.9 – simulation results for a step at the inner voltage reference under balanced loads at the system.

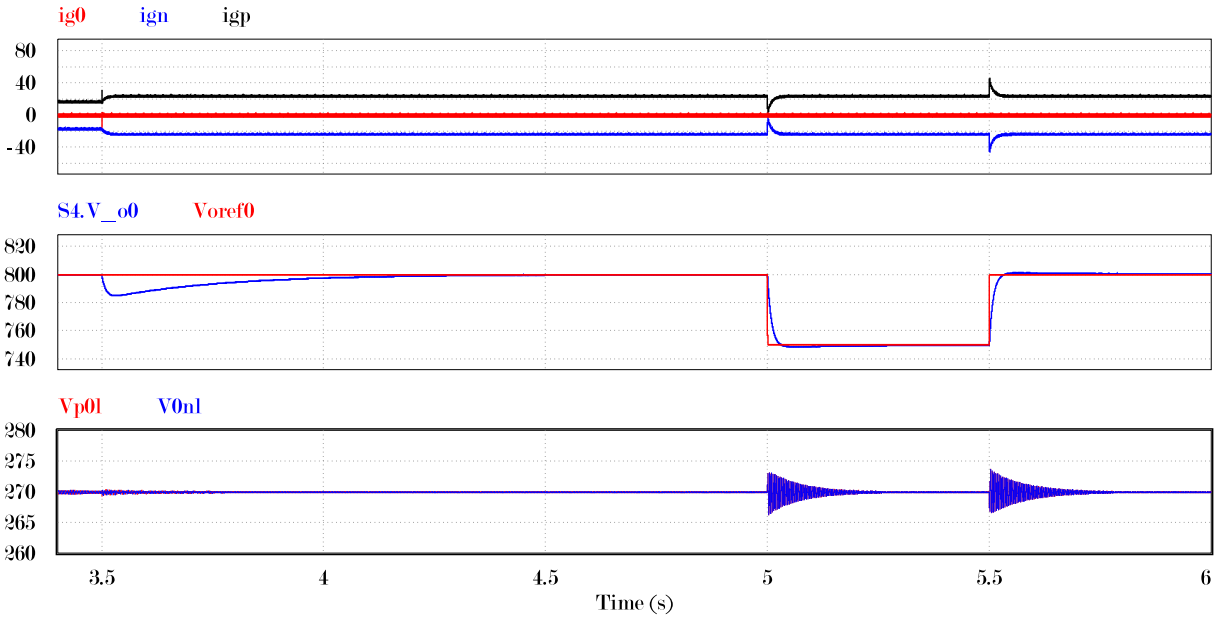


Figure 4.10 – simulation results for a step at the inner voltage reference under unbalanced loads at the system.

4.2.3 Dc bus and CR simulation under balanced and unbalanced resistive loads and CPLs

In this section, CPL will be add to the system and the CR must be able to compensate any unbalanced loads.

Fig. 4.11 shows the simulation results for a configuration for different loads. Before $t = 1.5\,\mathrm{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates.

At $t = 1.5\,\mathrm{s}$, a 500 W CPL load is added to the positive branch. Even with the CPL, The dc redistributor keeps the balance between i_{g_p} and i_{g_n}. At $t = 2.5\,\mathrm{s}$, a $40\,\Omega$ load is added to the positive branch. The dc redistributor adjusts the current flowing in the dc bus grid and guarantees that i_{g_0} remains zero and $i_{g_p} = -i_{g_n}$.

At $t = 4\,\mathrm{s}$, another 500 W CPL load is added to the positive branch and at $t = 4.5\,\mathrm{s}$, another 500 W CPL load is added to the positive branch. Now, The system has a 1500 W CPL load, 5400 W resistive load, and the dc redistributor is still able to guarantee the current balancing. At these situations, the voltage controller keeps v_0 to its reference.

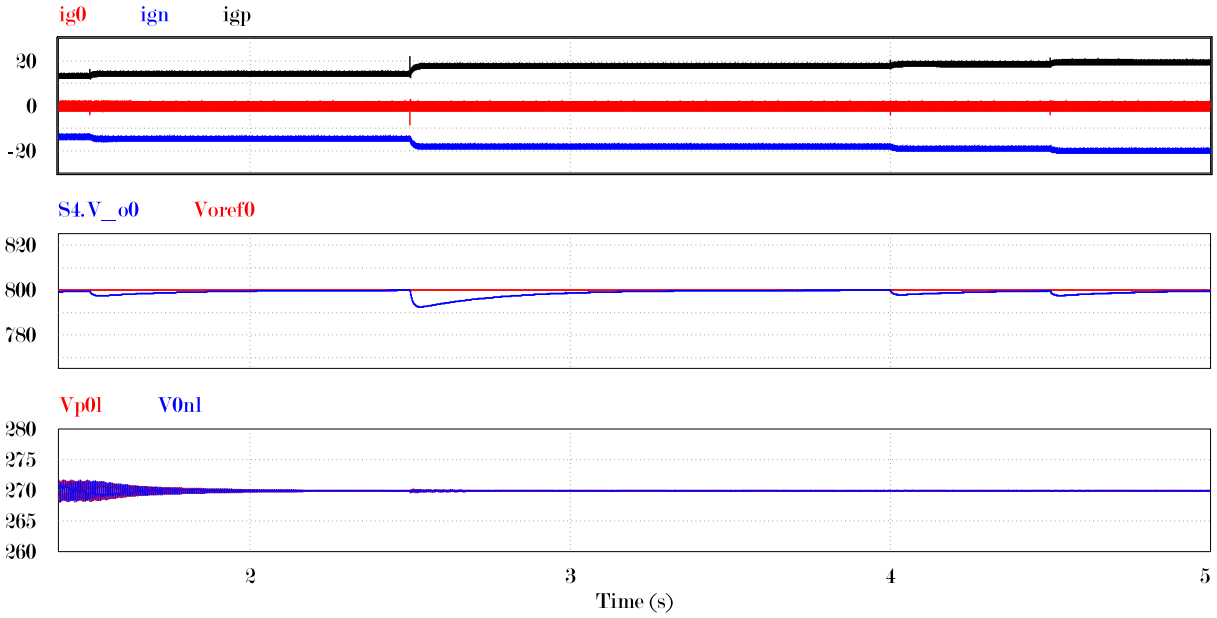


Figure 4.11 – Simulated results from CPL and positive unbalanced loads

Fig. 4.12 shows the simulation results for a configuration for different loads. Before $t = 1.5\,\mathrm{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates. At $t = 1.5\,\mathrm{s}$, a 500 W CPL load is added to the negative branch. Even with the CPL, The dc redistributor keeps the balance between i_{g_p} and i_{g_n}. At $t = 2.5\,\mathrm{s}$, a $40\,\Omega$ load is added to the negative branch and the dc redistributor adjusts the current flowing in the dc bus grid.

At $t = 4\,\mathrm{s}$, another 500 W CPL load is added to the negative branch and At $t = 4.5\,\mathrm{s}$, another 500 W CPL load is added to the negative branch. Over again, The system has a 1500 W CPL load and the dc redistributor is still able to guarantee the current balancing. At these situations, the voltage controller keeps v_0 to its reference.

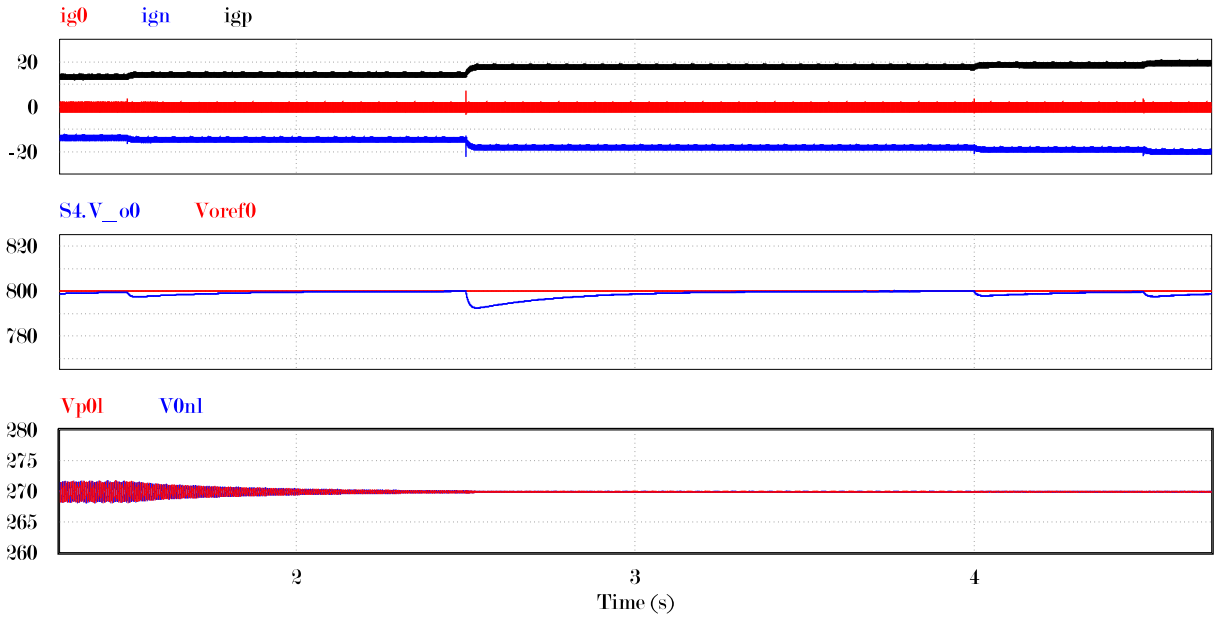


Figure 4.12 – Simulated results from CPL and negative unbalanced loads

Fig. 4.13 shows the simulation results for a configuration for different loads. Before $t = 1.75\,\text{s}$, the dc bus feeds a $20\,\Omega$ balance load and the dc redistributor operates. At $t = 1.75\,\text{s}$, a $40\,\Omega$ load is added to the negative branch. As shown in the figure, the dc redistributor adjusts the current flowing in the dc bus grid. At $t = 3.75\,\text{s}$, a 1000 W CPL load is added to the negative branch. In this configuration, the dc redistributor keeps the balance between i_{g_p} and i_{g_n}. At $t = 4.25\,\text{s}$, a 500 W CPL load is added to the positive branch. Even with the resistance load and CPL unbalanced, the dc redistributor is able to keep the balance between i_{g_p} and i_{g_n}.

At these events, the voltage controller was able to keep v_0 to its reference.

At the beginning of the simulation, with balanced loads, an undamped oscillation is observed in the voltages of the positive and negative busbars. The oscillation is due to the behavior of the bus LC filter. Although the control loops are active, as there is no neutral current, the control of the converter is not able to act to prevent this oscillation. When a load imbalance occurs and the currents are effectively controlled by the converter, this oscillation tends to disappear. This checks the ability of the converter to act by dampening the oscillations produced by the filter.

After the first actuation of the converter, with the significant reduction of the oscillation in the voltages, even if the loads are balanced again, the ability to minimize this oscillation is maintained, as shown in the figure 4.14.

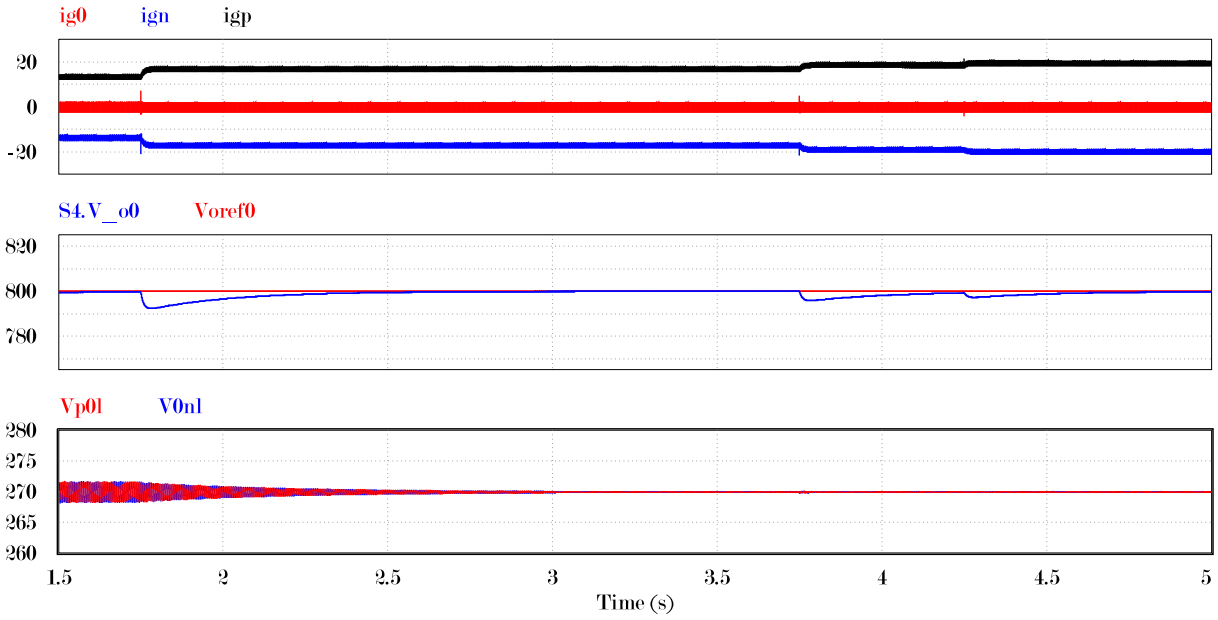


Figure 4.13 – Simulated results from different loads.Top: dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}; Bottom: dc CR inner voltage V_0 and its reference, V_{0ref} .

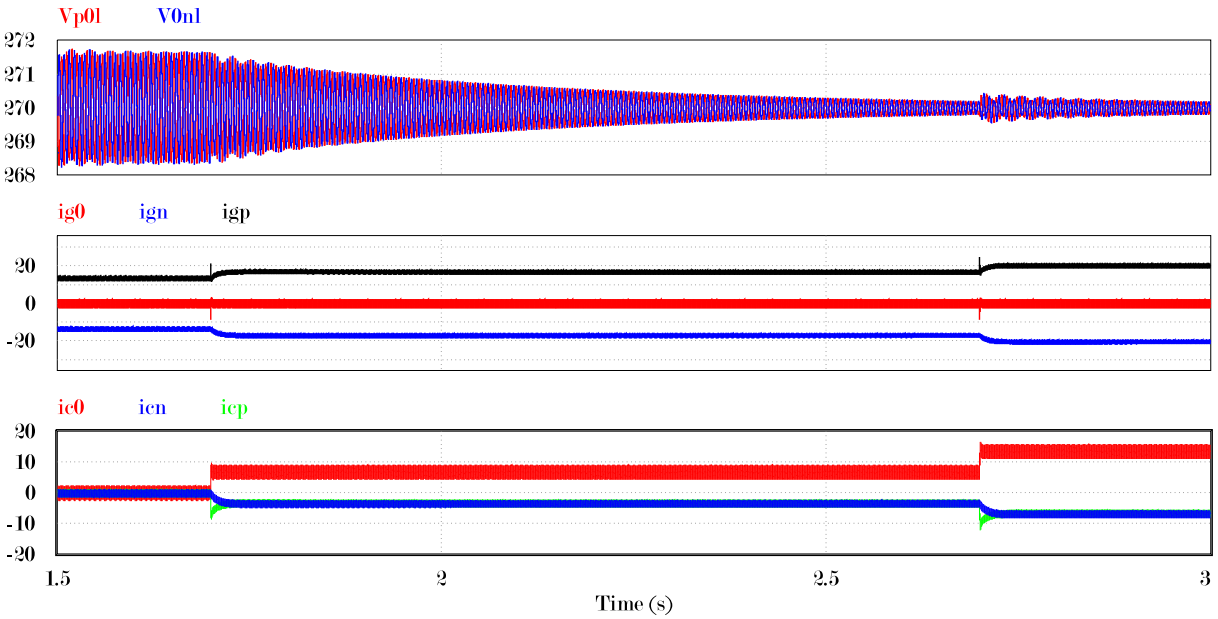


Figure 4.14 – Simulated results from different loads.Top: dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}; Bottom: dc CR inner voltage V_0 and its reference, V_{0ref} .

4.3 CR as a dc bus forming converter

We can also evaluate if the CR is able to operate with a loss of the dc lines and interface with an emergency dc energy storage. For this case, the CR must keep the voltage at the levels described at the MIL-STD-704F. So, it's necessary a different control structure at this emergency situation.

4.3.1 Proposed control system

The MIL-STD-704F [19] standard defines Abnormal operation when a malfunction in the electric system occurs and the protective devices of the system are operating to deal with this event. Regarding the emergency operation, this standard defines it as the occurrence of the loss of the main generating equipment. The system works with power reduced and selected equipment to maintain flight and personnel safety.

Figure 4.15 shows the dc limits of a undervoltage or overvoltage transient for the 270 volts busbars.

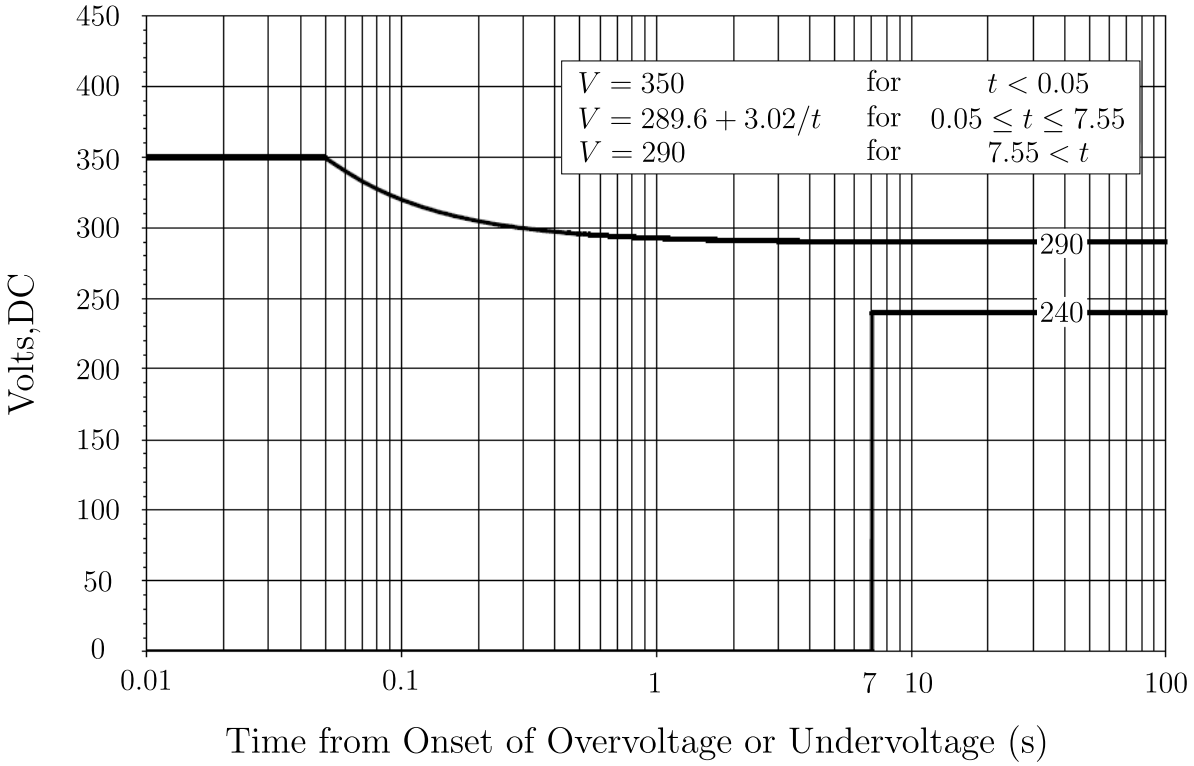


Figure 4.15 – Limits for dc overvoltage or undervoltage for 270 volts dc system.

Figure 4.16 shows the dc current redistributor proposed control for the emergency situation. We have a feedforward technique applied at the upper and lower legs of the CR, the output of the dc bus redistributor voltage PI is added at the upper and the lower legs duty cycles. For the central leg, the reference of the current central branch current i^*_{g0} is zero.

The blocks C_v, C_{i_0}, voltage and central current controllers, respectively, are PI obtained from the SISOTOOL MATLAB.

Table 4.2 – Simulation parameters for emergency situation.

Parameters	Value
Current controller time constant (T_{c_i})	0.01
Current controller gain (K_{c_i})	0.01
Voltage controller gain (K_{c_v})	0.005

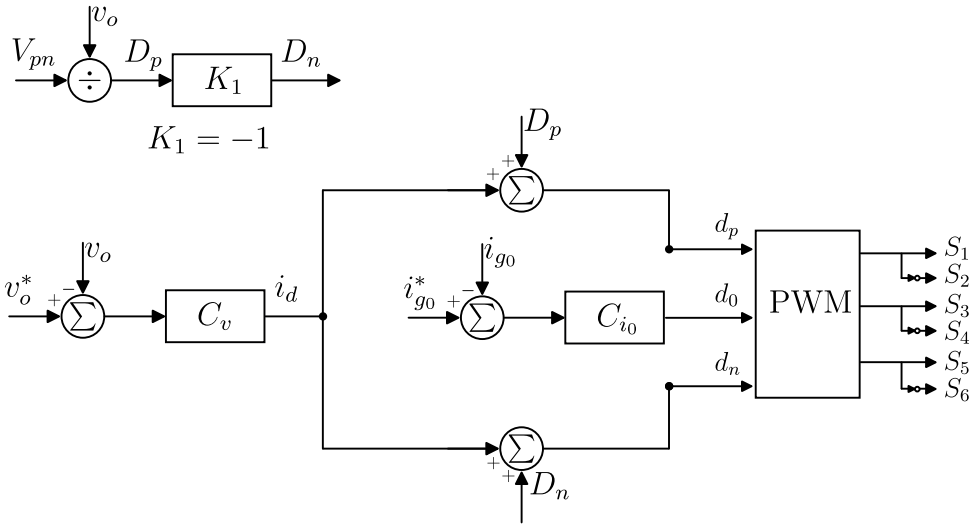


Figure 4.16 – Block Diagram of the propose control for operate with a loss of the dc lines.

4.3.2 Simulation results

We can also evaluate if the CR at the configuration of 12 pulse rectifier with series connection is able to operate with a loss of the dc lines and interface with an emergency dc energy storage. Fig. 4.17 shows the circuit diagram for the simulation of the aircraft system containing the dc bus and the bidiretional switch which emulates the loss of the dc lines.

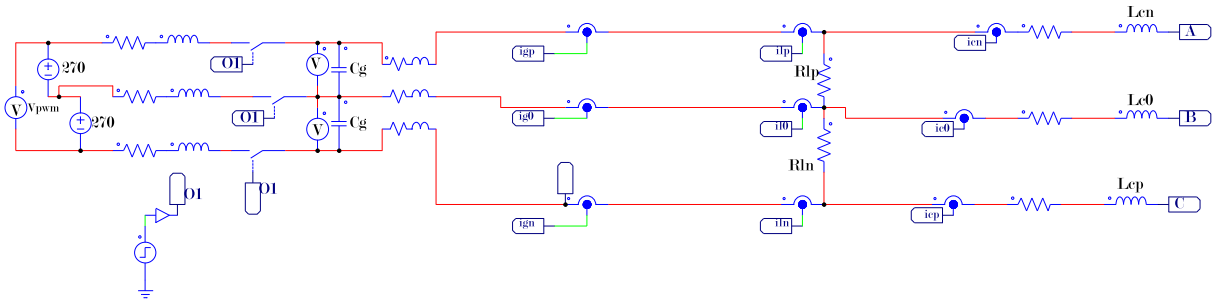


Figure 4.17 – Diagram of the TRU power circuit in PSIM.

Fig. 4.18 shows the simulation results for a loss of the dc lines, i.e. an abnormal situation or emergency situation. Before $t = 0.1\,\text{s}$, the dc bus feeds unbalance loads and the dc redistributor guarantees the neutral current at zero. At $t = 0.1\,\text{s}$ occurs the loss of the dc lines, and the dc voltages start to decrease. An emergency battery system is

connected to the CR 20 ms later. Now, the CR must keep the dc voltages bus at 270 V to guarantee the power supply. The CR maintains the dc voltage at the levels established at the Figure 4.15.

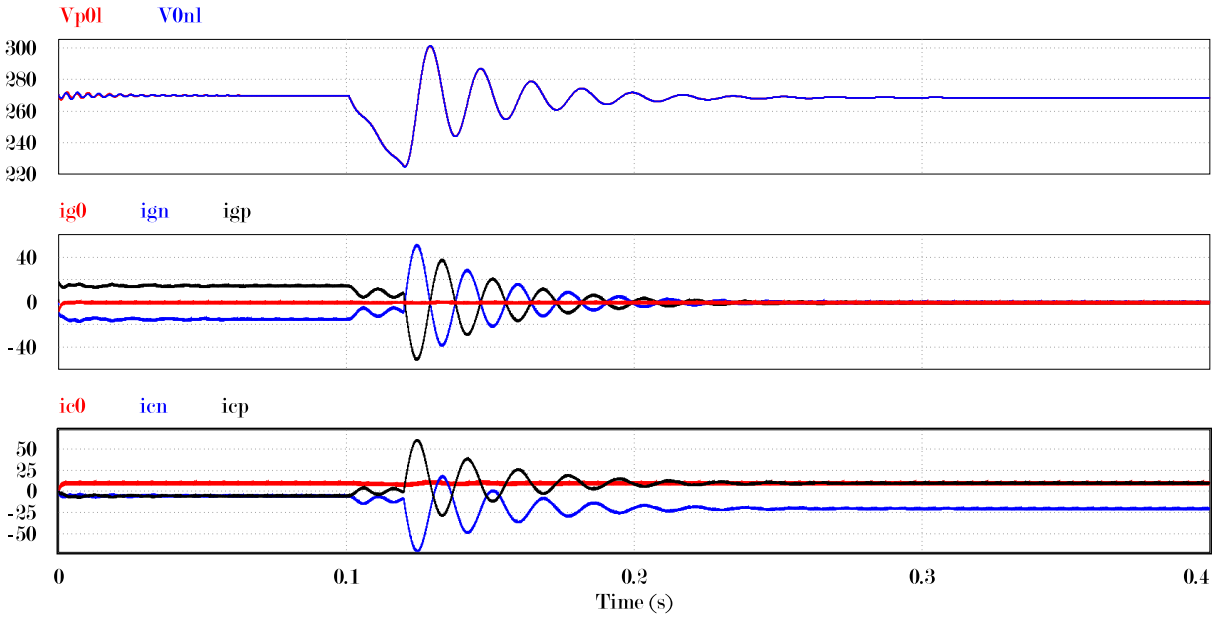


Figure 4.18 – Interaction with the emergency energy storage with considering a 12 pulse rectifier with series connection

For a TRU composed by a PWM rectifier, the neutral reference is created depending upon the topology and the dc link circuit. Its operation guarantees a total bus of 540 V and the neutral is created by a capacitive divider. In this case, unbalanced loads on positive and negative branches lead to a change on the voltage on the common point, which is the neutral point of the dc bus.

In this case, the role of the CR changes to that of ensuring the balance of voltages. However, by ensuring that the neutral current is canceled, the effect is to equalize the currents in both outputs, even with unbalanced loads, resulting in the balance of DC voltages.

Fig. 4.19 shows the simulation results for unbalanced loads. The positive feeder load is 13.5 Ω and the negative feeder load is 27 Ω. The dc redistributor adjusts the current flowing in the dc bus grid ensuring that the neutral current goes to zero. So, even with unbalanced loads, the CR maintains the dc voltages at 270 V. At this situation, the voltage controller keeps v_0 to its reference.

Finally, we will evaluate the CR as a grid emergency forming system considering a PWM rectifier. Fig. 4.20 shows the circuit diagram for the simulation of the aircraft

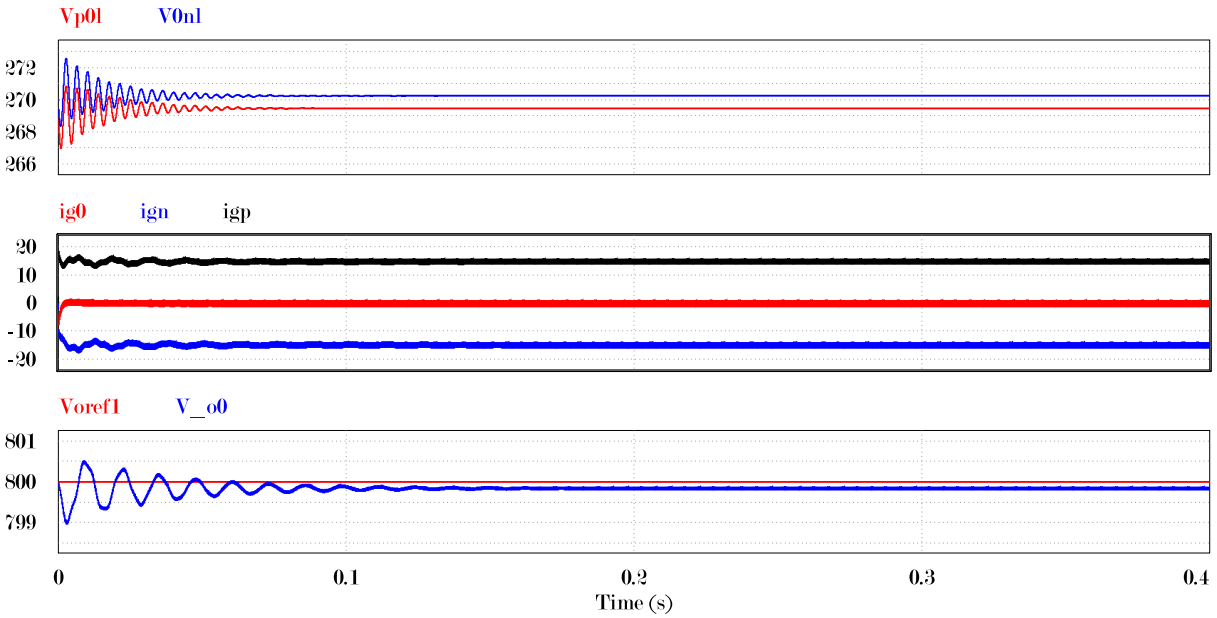


Figure 4.19 – Balancing of the dc voltages busbars considering a PWM Rectifier

system.

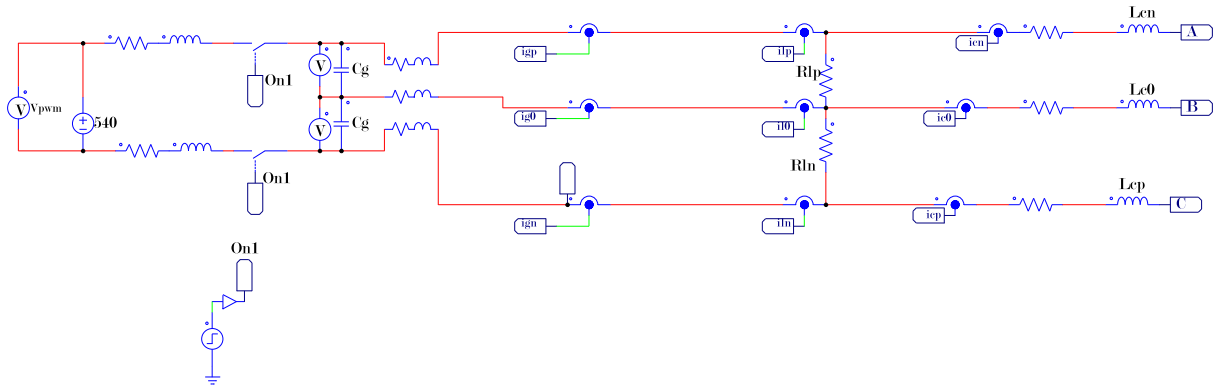


Figure 4.20 – Diagram of the PWM power circuit in PSIM.

Fig. 4.21 shows the simulation results for a loss of the dc lines. Before $t = 0.2\,\text{s}$, the dc bus feeds unbalance loads and the dc redistributor operates canceling the neutral current. At $t = 0.2\,\text{s}$ occurs the loss of the dc lines, and the dc voltages start to decrease. An emergency battery system is connected to the CR 20 ms later. Now, the CR must keep the dc voltages bus at 270 V to guarantee the power supply. A voltage transient at the dc voltage can be observed. However, the CR maintains the dc voltage at the levels established at the Figure 4.15. So, the CR is able to ensure the balance and maintenance of the voltages.

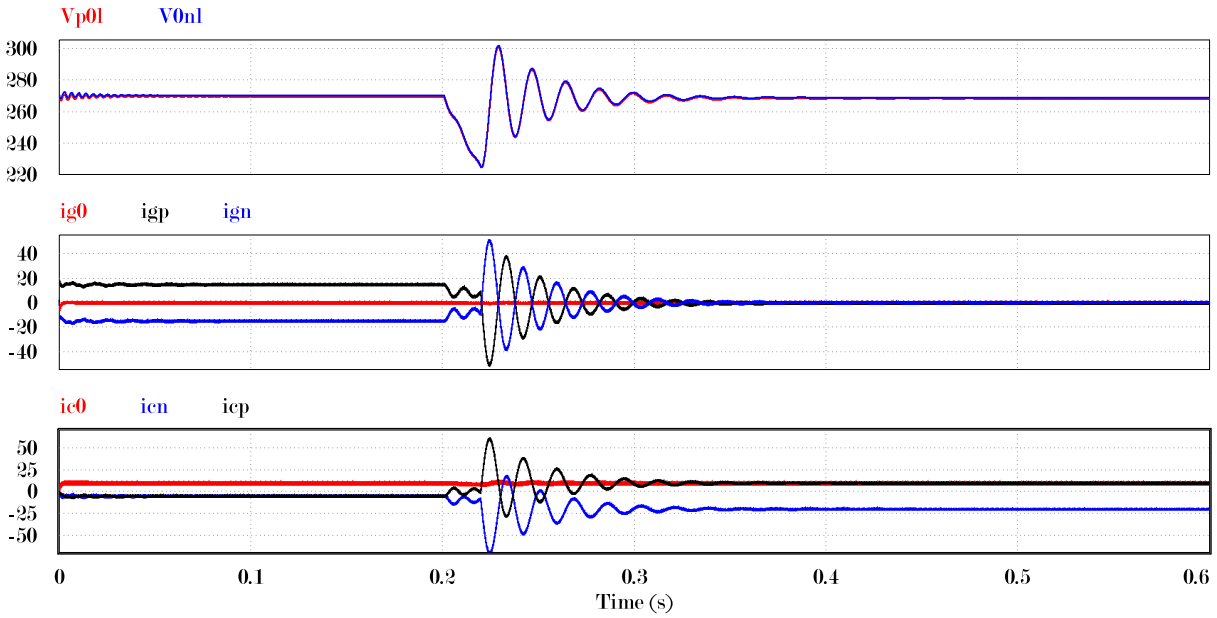


Figure 4.21 – Interaction with the emergency energy storage with considering a PWM Rectifier

5 Conclusion

In this work, power electronic solutions are investigated for assure the Electric Power Quality in aeronautical environments. Nowadays, the electrical energy consumption has increased in the aircraft electric system. This increase has lead several research in power electronics and the More Electric Aircraft (MEA) concept was proposed. This trend is based on replacement of hydraulic and pneumatic actuators by electromechanical devices.

Firstly, the aircraft system is introduced along with the MEA trend and a dc current redistributor (CR) is proposed to mitigate the unwanted effects found in the dc aircraft internal feeders. The CR must deal with the current unbalance between the positive and negative poles of the dc bus to comply with the standards.

At chapter 3, this thesis discussed the procedure to developed a dynamic model of the CR. The dc internal currents are dependents due to the output inductor in the central lag. So, a decoupling was applied to control independently these variables. The current model and the voltage mode of the CR were shown.

The simulation results were presented in chapter 4. The dc bus was subjected to different load configurations. It was shown that, the CR was able to keep the balance between the dc bus currents and the inner voltage at its reference even with unbalanced loads composed by a resistive load and a CPL. Additionally, the CR was able to operate with a loss of the dc lines and interface with an emergency dc energy storage.

This work proposed a dc-dc converter working as a current redistributor that was able to deal with the current unbalancing at the internal feeder of a aircraft system under several load configurations. This proposed CR is a potential power electronics solution to operate at this aircraft system.

5.1 Published Paper

This master work resulted in a 6-page full paper accepted, included in appendix A, for the joint conferences SPEC (Southern Power Electronics Conference) and COBEP (Brazilian Power Electronics Conference), which are the most important events

for researchers in power electronics in the southern hemisphere. The COBEP is the most important and traditional Brazilian forums for researchers in power electronics. The SPEC is a initiative of serving power electronics conferences society to southern hemisphere.

5.2 Future work

- Experimental verification of the downscale prototype (limited to 1 kVA), which is describe in Appendix B, to validate the modelling and simulation results published in COBEP/SPEC 2019;
- Modeling focusing in CPL and dynamic interactions with dc bus and the redistributor with several unbalanced loads;

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APPENDIX A – Published paper at COBEP/SPEC 2019

DC Current Redistributor for Electric Aircraft System

Mateus P. Dias, Hildo Guillardi Jr., Joel F. Guerreiro,
João I. Y. Ota, José A. Pomilio
School of Electrical and Computer Engineering
University of Campinas
Campinas, Brazil
{mateuspinheirodias, hildogjr, joel.engeletrica}@gmail.com;
{yutaka, antenor}@fee.unicamp.br

Paolo Mattavelli
Dept. of Management and Engineering
University of Padova
Vicenza, Italy
paolo.mattavelli@unipd.it

***Abstract*—The More Electric Aircraft (MEA) concept focuses on the replacement of pneumatic and hydraulic actuators by electromechanical actuators and increases the electric power demand in the aircraft. This article aims to the study and the implementation of a Power Electronic Conditioner (PEC) to mitigate the unwanted effects found in the dc aircraft internal feeders. The PEC must deal with the current unbalance between the positive and negative poles of the dc bus to comply with the standards. A mathematical dynamic model and control of PEC were simulated in the software PSIM®.**

***Index Terms*—More Electric Aircraft; DC Current Redistributor; Power Electronic Conditioner.**

I. Introduction

The electrical power consumption in commercial aircrafts has increased during the years, mainly due to the replacement of hydraulic and pneumatic actuators by electromechanical devices. This replacement has been called as the More Electric Aircraft (MEA) [1], [2], and it contributes for decreasing aircraft weight and the fuel consumption. The MEA purpose is to minimize losses in the system and to be able to comply with the ac and dc grids standards. Furthermore, this advancement has motivated researches in power electronics for more reliable, less maintenance effort and more efficient equipment [3]–[6], which include power distribution, power generation, engine gearbox etc. Power electronics devices have an important contribution for the development of a new Power Distribution Systems (PDS), including protection devices like circuits breaker and fault circuits breaker [7], [8].

Fig. 1 shows a modern commercial aircraft based on the MEA concept, which has an electrical grid consisting of many subsystems including different ac and dc voltage grids [1].

The first generation of ac grids on airplanes works at a fixed frequency (400 Hz 115/200 V) [9], including, for example, the EMB190 and 195 (Embraer). The second generation, with variable frequency (230/400 V 360-800 Hz) includes Boeing 787 [1]. Both ac and dc grids must comply with Power Quality (PQ) standards. The MIL-STD-704F [10] standard establishes the voltage limits in dc and ac buses and the spectral distortion. On the other hand, the standard RCTA-DO106F [11] describes the procedures for testing equipment or loads that will be installed in the airplane.

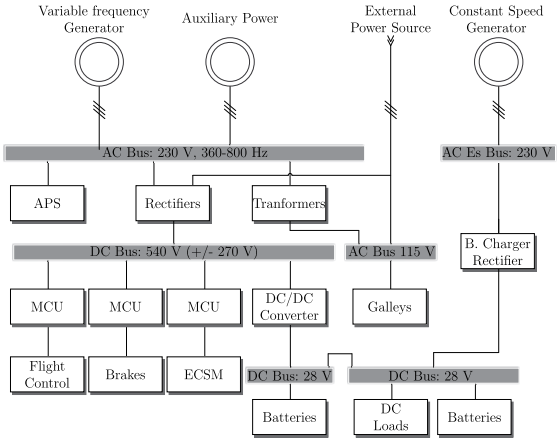

Fig. 1. A typical architecture of a modern MEA [1].

With the implementation of MEA concept, the number of electric and electronic devices in aircraft has grown significantly, and the dynamic interactions among them have become more complex. As a consequence, complying with the power quality standards has become a challenge in MEA systems. Especially in the dc bus, current unbalance due to unbalanced loads, may increase common-mode current on neutral wire. The increase of common-mode current may cause serious problems on the MEA system mainly to the ac generator since the neutral point of the symmetrical dc bus is tied to the ac three-phase generator neutral. A dc redistributor is an electronic device that shall be able to mitigate unbalanced currents, this minimizing common-mode current.

This article presents the study and implementation of a dc redistributor for a bipolar dc bus. The dc redistributor is based on a dc-dc converter, which is modeled and simulated for unbalanced load conditions of the dc bus grid.

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II. Bipolar dc Bus

The usual topology to supply energy through a bipolar dc bus is a Transformer Rectifier Unit (TRU) with multipulse diode rectifiers due to the harmonics restrictions, mainly the 3th, 5th and 7th harmonic components. For the $540\,\mathrm{V}$ dc bus, with +/- $270\,\mathrm{V}$ symmetric voltages, the 12-pulse diode rectifier appears as a simple solution once it has no-actives elements, simple structure and low harmonic content. However, it does not allow the dc voltage regulation [12]. The PWM-rectifier is an alternative due to their high efficiency [13]–[15], high power factor, low harmonic content [16], output dc voltage regulator, since it is an controlled rectifier. For the purpose of this paper, the rectifier topology is not important. The relevant aspects are the availability of the symmetrical dc bus and the unbalanced dc loads on the rectifier.

Consider a 12-pulse rectifier, built by the series connection of two 6-pulse diode rectifier. The transformer that feeds the rectifier has two secondary windings, one star connected and the other a delta connected. Unbalanced loads will result different currents at each bridge, and the effective cancellation of the 5th and 7th harmonies will not happen at the transformer primary side.

For the PWM rectifier, the issue is the zero sequence current component that, in case of unbalanced dc load will flow through the neutral wire, which is tied to the neutral point of the ac generators, both at the ground reference. Common mode current affects the magnetizing flux of the generator, increasing losses and reducing the quality of the generated voltages.

Fig. 2 shows a simplified model of the dc bus, including ideal dc sources, positive and negative; the feeder resistances (positive, negative, and neutral), and the positive and negative loads.

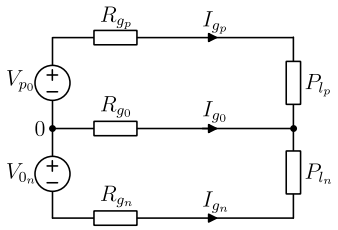

Fig. 2. Simplified Circuit of dc bus [16].

This article investigates a PEC for the dc bus aimed to compensate unbalanced loads. Fig. 3 shows a Current Redistributor Converter (CR), the structure for balancing the bipolar currents, i_{g_p} and i_{g_n} [13]. The CR is also known as current equalizer.

A. DC-DC converters as Current Redistributor

The main function of the Current Redistributor (CR) is to guarantee that the neutral current, i_{g_0}, is null. Fig. 4 shows the dc-dc converters which can operate as a CR.

The CR can do other functions, such as:

1) Voltage dynamic regulation;

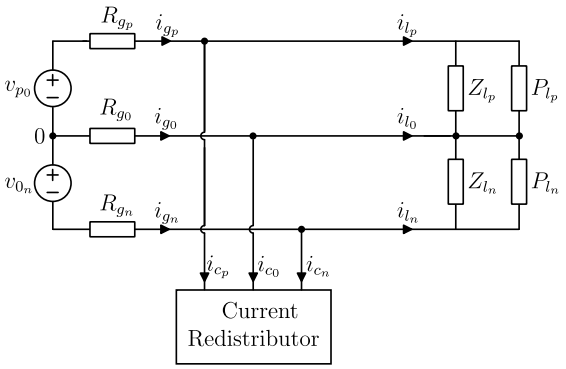

Fig. 3. Bipolar dc bus architecture including a CR and lumped loads.

2) Active damping;
3) Absorbing regenerate energy ;
4) Interface with dc energy storage (battery bank and super-capacitors) and being able to operate with loss of one dc line [17];

Fig. 4a shows a bidirectional buck converter, which is the simplest topology able to redistribute the current in the dc bus. It contains one inductor and two transistors, however the currents in the positive and negative feeders are not filtered and none of the other functions can be implemented [16].

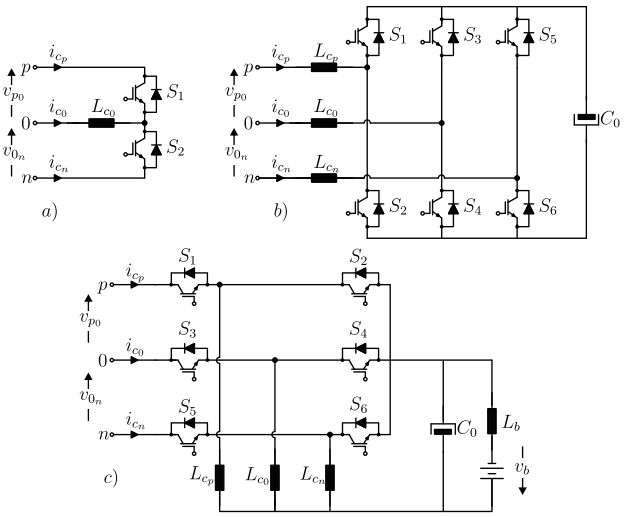

Fig. 4. DC-DC converters that can operated as a CR.

Fig. 4b shows a bidirectional boost converter, which is able to perform not only the current balance but also the functions 1, 2, 3 in the dc bipolar network. This topology enables active power injection if the inner dc bus voltage is higher than the voltage of the dc bus. This converter is the chosen dc redistributor topology in this study.

Fig. 4c shows a bidirectional buck-boost converter, which is able to perform the current balance and the function 4 in the dc bipolar network. However, the input currents in the upper and lower dc-side are not filtered, introducing high frequency disturbance in the dc bus.

III. System description

The presence of multiple power converters in the grid, with the respective control structures, requires the study of the stability of the complete grid. Many of these converters behave as constant power loads (CPL), which means that they will absorb a higher current when the input voltage decreases and vice-versa. The result is a dynamic characteristic expressed by a negative resistance, affecting the system stability [17].

An example of CPL is a dc-dc voltage regulator feeding resistive load. The input power of the dc-dc converter is constant due to the output voltage regulation. Other example is a dc-ac converter feeding a motor, under a speed control. In steady state, a controller regulates the speed at a given operating point. Thus, the torque is constant and the system behaves as a CPL.

Fig. 5 shows a block diagram of a power converter that feeds an ideal CPL. The load is modeled as a controlled current source. The system stability can be analysed using the Nyquist Criterium, based on the ratio between the CPL input impedance (Z_i) and the converter output impedance (Z_o) [18].

Fig. 6 shows that the Current Redistributor Converter, associated with the dc loads can work as a CPL. In this sense, the CR dynamic model must be developed.

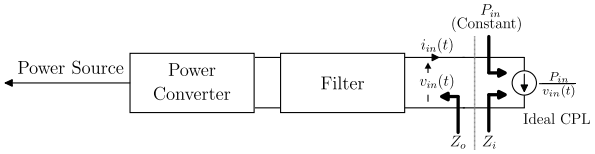

Fig. 5. Ideal CPL [18].

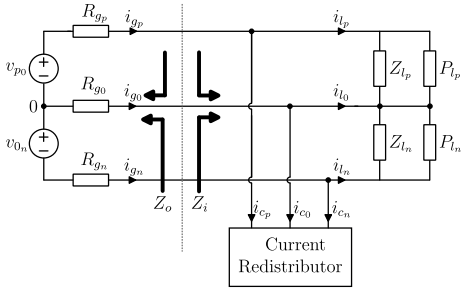

Fig. 6. Bipolar dc Bus architecture including a CR.

IV. Current and Voltage Models

This section shows the development of the CR model proposed in [16]. The converter uses pulse width modulation (PWM), with a switching frequency f_s. The duty cycles are based on the ratio of dc bus voltage,V_{pn}, and dc inner voltage, V_o, that can be obtained by (1), D_δ.

With dc bus symmetrical voltages, $V_{p0} = V_{0n} = V_{pn}/2$, the duty cycle of the switch connected to the central line is chosen $D_o = 1/2$. The upper, D_p, and lower, D_n, line duty cycle switches are represented by (2) and (3). Equation (4) shows their relation.

$$D_\delta = \frac{V_{pn}}{2V_0} \tag{1}$$

$$D_p = \frac{1}{2} + D_\delta \tag{2}$$

$$D_n = \frac{1}{2} - D_\delta \tag{3}$$

$$D_p - D_0 = D_0 - D_n = D_\delta = \frac{V_{pn}}{2V_0} \tag{4}$$

A. Current model

Fig. 7 shows the circuit of the dc redistributor. The transistors S_1 to S_6 can be represented as a single switch with two positions. In the following equations, the index x represents either p, 0 or n. Equations (5) and (6) show the commutation function $s_x(t)$ and the voltage between the switches and the reference T. When $s_x = 1$ (S_x is in position 1) the voltage v_{xT} assumes v_o, when $s_x = 0$ (S_x is in position 0) the voltage v_{xT} assumes 0.

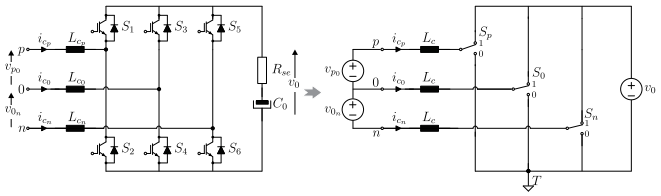

Fig. 7. The chosen dc redistribuitor topology.

$$s_x(t) = \begin{cases} 1, & S_x \text{ is on} \\ 0, & S_x \text{ is off} \end{cases} \tag{5}$$

$$v_{xT} = s_x v_o \tag{6}$$

Fig. 8 shows the equilibrium-point obtained applying the quasi-instantaneous average definition, (7), in the model variables and linearizing. Fig. 9 shows the steady state operation point of the converter.

Equation (8) shows the quasi-instantaneous value of the commutation function, known as duty cycle. It is composed by the D_x, steady state value, and the perturbation $\hat{x}$, as shown in (9).

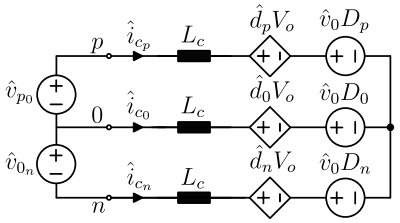

Fig. 8. Equilibrium point model

$$\bar{x} = \langle x \rangle_{T_s} = \int_{\tau - T_s}^{\tau} x(t)dt \tag{7}$$

$$d_x = \langle s_x(t) \rangle_{T_s}, \qquad 0 \leq d_x \leq 1 \tag{8}$$

$$\begin{cases} d_0 = D_0 + \hat{d}_0 \\ d_p = D_p + \hat{d}_p \\ d_n = D_n + \hat{d}_n \end{cases} \tag{9}$$

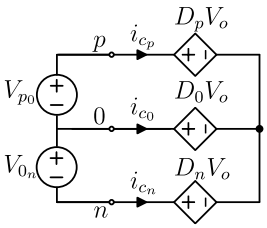

Fig. 9. Steady state operation point model.

The voltages $\hat{v}_{p_0}$ and $\hat{v}_{0_n}$ are describe in (10) and (11).

$$\hat{v}_{p_0} = V_o(\hat{d}_p - \hat{d}_0) + \hat{v}_0(D_p - D_0) \tag{10}$$

$$\hat{v}_{0_n} = V_o(\hat{d}_0 - \hat{d}_n) + \hat{v}_0(D_0 - D_n) \tag{11}$$

B. Current decoupling method

In the dc circuit, one of the duty cycles can be chosen arbitrarily, as mentioned before. To obtain a decoupled system, the superposition method can be applied.

Let $\hat{d}_p \neq 0$, $\hat{d}_n = 0$ and $\bar{i}_{c_n} = 0$. Fig. 10 shows the equivalent circuit. To satisfy $\bar{i}_{c_n} = 0$, the central leg duty cycle must follow (12).

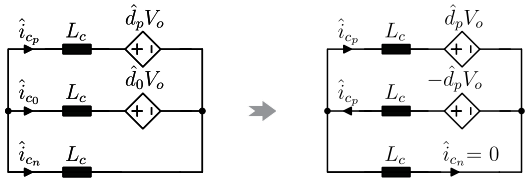

Fig. 10. Upper leg decoupling circuit.

$$\hat{d}_0 = -\hat{d}_p \tag{12}$$

Let $\hat{d}_n \neq 0$, $\hat{d}_p = 0$ and $\bar{i}_{c_p} = 0$. Fig. 11 shows the equivalent circuit. To satisfy $\bar{i}_{c_p} = 0$, the central leg duty cycle must follow (13).

$$\hat{d}_0 = -\hat{d}_n \tag{13}$$

The perturbation is the result of the superposition. Therefore, (14) shows the pattern of perturbation.

$$\hat{d}_0 = -\hat{d}_p - \hat{d}_n \tag{14}$$

Rewriting (14), (15) shows the pattern of perturbation.

$$\hat{d}_0 = (D_p + D_n + D_0) - d_p - d_n \tag{15}$$

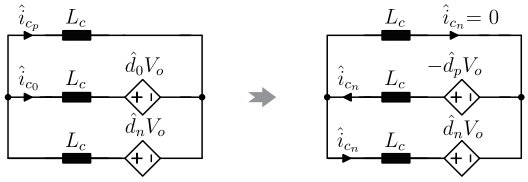

Fig. 11. Lower leg decoupling circuit.

Replacing $\hat{d}_0$ in (10) and (11), eq. (16) and (17) describe the voltages $\hat{v}_{p_0}$ and $\hat{v}_{0_n}$. Fig. 12 shows the decoupled circuit.

$$\hat{v}_{p_0} = V_o(2\hat{d}_p + \hat{d}_n) + \hat{v}_0(D_p - D_0) \tag{16}$$

$$\hat{v}_{0_n} = V_o(-\hat{d}_p - 2\hat{d}_n) + \hat{v}_0(D_0 - D_n) \tag{17}$$

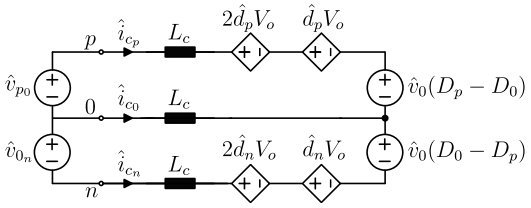

Fig. 12. Decoupled circuit.

Considering the bus voltage as a perturbation, eq. (18) and (19) show the transfer function of the upper leg current $\hat{i}_{c_p}$ and lower leg current $\hat{i}_{c_n}$ [16].

$$G_{i_{c_p}}(s) = \frac{\hat{i}_{c_p}}{\hat{d}_p} = -\frac{V_o}{sL} \tag{18}$$

$$G_{i_{c_n}}(s) = \frac{\hat{i}_{c_n}}{\hat{d}_n} = -\frac{V_o}{sL} \tag{19}$$

C. Voltage model

Fig. 13 shows the voltage model of the dc redistribuitor, which is evaluated following the same procedure.

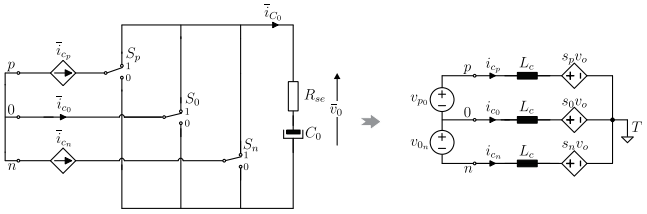

Fig. 13. Equivalent voltage model.

Owning to the linear relationship of the dc redistributor currents, eq. (20) describes $\bar{i}_{c_0}$.

$$\bar{i}_{c_0} = \bar{i}_{c_p} - \bar{i}_{c_n} \tag{20}$$

Eq. (21) evaluates $\bar{i}_{C_0}$:

$$\begin{aligned}\bar{i}_{C_0} &= \bar{i}_{c_p} D_p + (-\bar{i}_{c_p} - \bar{i}_{c_n}) D_0 + \bar{i}_{c_n} D_n \\ &= D_\delta (\bar{i}_{c_p} - \bar{i}_{c_p})\end{aligned} \tag{21}$$

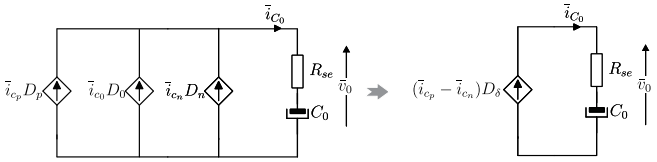

Fig. 14. Simplified circuit.

Fig. 14 shows the simplified circuit. The voltage v_o is evaluated from the circuit on the right-hand side. Expanding (22), considering only the perturbation component, (23) shows the voltage $\hat{v}_o$.

$$\bar{v}_o = \bar{i}_{C_0} Z_c \tag{22}$$

$$\hat{v}_o(s) = \frac{V_{p_n}}{2V_o} \frac{(sC_o R_{se} + 1)}{sC_o} (\hat{i}_{c_p} - \hat{i}_{c_n}) \tag{23}$$

Eq. (24) and (25) describe the dc differential current and the dc common-mode current, respectively.

$$\hat{i}_{c_{dm}} = \frac{\hat{i}_{c_p} - \hat{i}_{c_n}}{2} \tag{24}$$

$$\hat{i}_{c_{cm}} = -\frac{\hat{i}_{c_p} + \hat{i}_{c_n}}{2} \tag{25}$$

Eq. (26) and (27) describe the dc positive current and the negative current, respectively.

$$\hat{i}_{c_p} = \hat{i}_{c_{dm}} - \hat{i}_{c_{cm}} \tag{26}$$

$$\hat{i}_{c_n} = -\hat{i}_{c_{dm}} - \hat{i}_{c_{cm}} \tag{27}$$

Applying (24) in (23), eq. (28) shows the transfer function of the voltage model.

$$\begin{aligned}G_v(s) = \frac{\hat{v}_o}{\hat{i}_{c_{dm}}} &= \frac{V_{p_n}}{2V_o} \frac{(sC_0 R_{se} + 1)}{2sC_o} \\ &= \frac{D_\delta (sC_0 R_{se} + 1)}{2sC_o}\end{aligned} \tag{28}$$

V. CR Control System

Fig. 15 shows the propose control of the dc current redistributor. The references are the neutral grid current $i^*_{g_0}$, that must be zero, and the dc bus redistributor voltage v^*_0. ${T_c}^{-1}$ represents the inverse transformation of common and differential modes into the positive and negative current references, which are represented in (26) and (27). Next, the decoupling method described in (15) takes place and the duty cycles for the PWM switching are obtained.

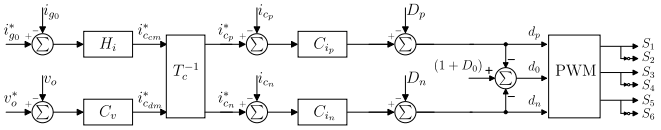

Fig. 15. Block Diagram of propose control.

The blocks C_v, C_{i_p}, C_{i_n} correspond to the voltage, upper and lower current controllers, respectively. These controllers are proportional integrator (PI) obtained from the SISOTOOL MATLAB®.

VI. Simulation Results

Table I shows the parameters used for this simulation in PSIM®. Fig. 16 shows the circuit diagram for the simulation of the aircraft system containing the dc bus, the dc current redistribuitor and the unbalanced loads, including CPL. The CPL is emulated by an ideal controlled current source.

TABLE I
Simulation parameters for DC redistribuitor.

Parameters	Value
dc bus voltages ($V_{p_0} = V_{0_n}$)	270 V
dc redistributor bus voltage(V_0)	800 V
Positive feeder Load (R_{lp1})	20 Ω
Negative feeder Load (R_{ln1})	20 Ω
Additional negative feeder Load (R_{ln2})	10 Ω
Power rating of Ideal CPL (w_q)	2000 W
Switching frequency (f_s)	10 kHz
dc redistributor Capacitor (C_o)	1 mF
Redistributor Inductor (L_c)	2 mH
Current cut-off frequency (f_c)	998 Hz

Fig. 17 shows the simulation results for different loads configurations. The top waveforms represent the dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}. The bottom waveforms represent the dc CR inner voltage V_0 and its reference, V_{0ref}.

Before $t = 1.5$ s, the dc bus feeds a 20 Ω balance load and the dc redistributor operates. At $t = 1.5$ s, a 2000 W CPL load is added to the positive branch. The dc redistribuitor adjusts the current flowing in the dc bus grid, therefore i_{g_0} remains zero and i_{g_p} and i_{g_n} are balanced, i.e. $i_{g_p} = -i_{g_n}$. At $t = 2.5$ s, an extra 40 Ω parallel load is added to the negative branch. The dc redistribuitor keeps the balance between i_{g_p} and i_{g_n}. At both $t = 1.5$ s and $t = 2.5$ s, the voltage controller keeps v_0 to its reference.

At $t = 3.5$ s, the inner voltage reference goes to 850 V. Even with this step in voltage reference, the dc CR is able to regulate the inner CR voltage at its new reference.

VII. Conclusion

This work presents the modeling and simulation of a power electronics converter, working as a current equalizer, applied to the symmetrical dc bus of the electric network boarded in an aircraft. The equalization of the currents between the positive and negative buses is necessary to guarantee correct operation of the rectifier, in order to comply with aeronautical power quality standards. The bidirectional boost converter is chosen due to its capacity to perform the current balance

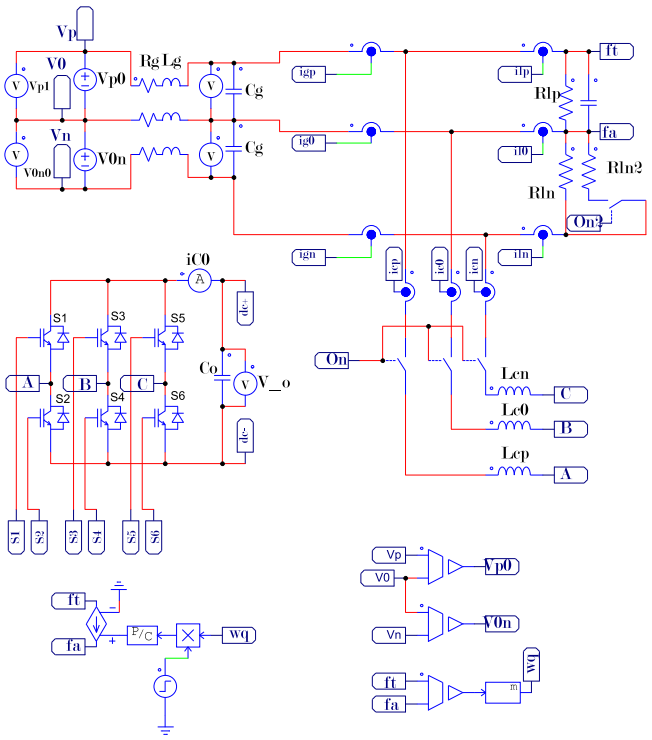

Fig. 16. Diagram of the power circuit in PSIM.

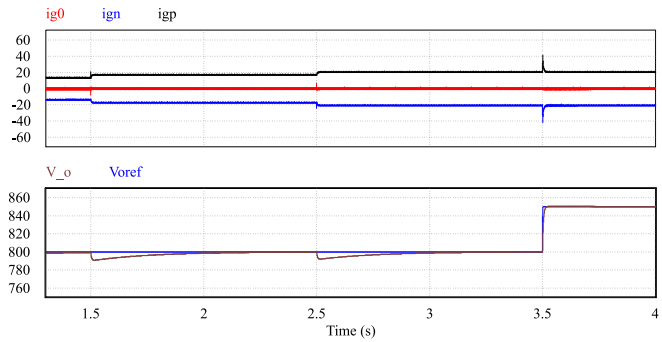

Fig. 17. Simulated results from different loads.Top: dc bus grid currents, i_{g_0}, i_{g_p} and i_{g_n}; Bottom: dc CR inner voltage V_0 and its reference, V_{0ref} .

between the positive and negative buses, active damping, regeneration of energy and dc energy storage interaction. From the dynamic model of the bidirectional boost converter, the current controllers as well as the internal dc voltage regulator can be designed. Simulation results show that the converter is capable of balancing the currents and maintaining its dc voltage regulated in situations of load variation, whether they are resistive or have a constant power (CPL) behavior. In conclusion, the topology chosen is a potential and suitable candidate for the current redistributor applied in More Electric Aircraft environment. Future experimental results shall be carried out and confirm the effectiveness of the proposed current redistributor.

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APPENDIX B – Experimental Setup

B.1 FPGA Boards and DSP microcontrollers

DSP microcontrollers and FPGA boards were studied to determine the best digital control device.

Figure B.1 shows the Altera's Cyclone V 5CEBA4F23C7N Device. The theoretical approach to program and to understand the FPGA was based on the book "Digital Control of High-Frequency Switched-Mode Power Converters"[45].

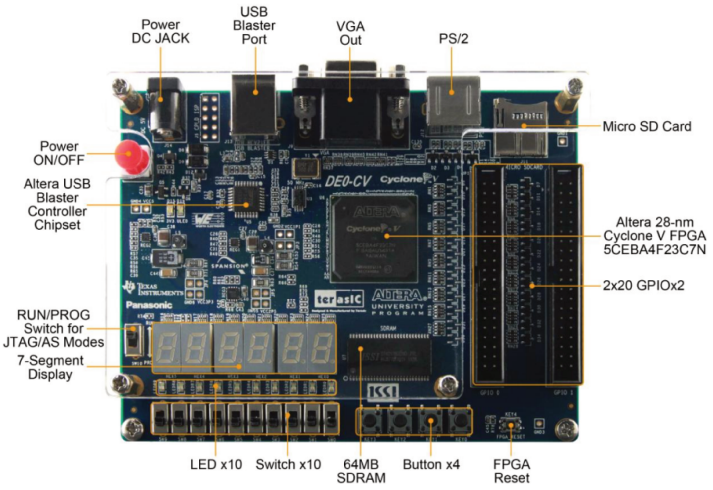

Figure B.1 – Altera's Cyclone V 5CEBA4F23C7N DE0-CV2.

Figure B.2 shows the chosen control device Texas Instruments' TMS320F28335 Experimenter Kit DSP Device. The theoretical approach to program and to understand the DSP is based on the technical documentation "TMS320x2833x DSP Device."

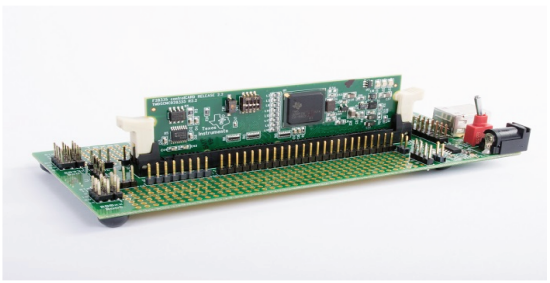

Figure B.2 – Texas Instruments' TMS320F28335 Experimenter Kit DSP.

B.2 Control and Acquisition Board and Experimental Assembly

Figure B.3 shows the experimental setup assembled in the LCEE. The Prototype is in tests period. Figure B.4 shows the electrical board used for the control and switching of the mosfets and the data acquisition. The author is very thankful for the help of Dr. Hildo Guillardi, who designed the electrical board.

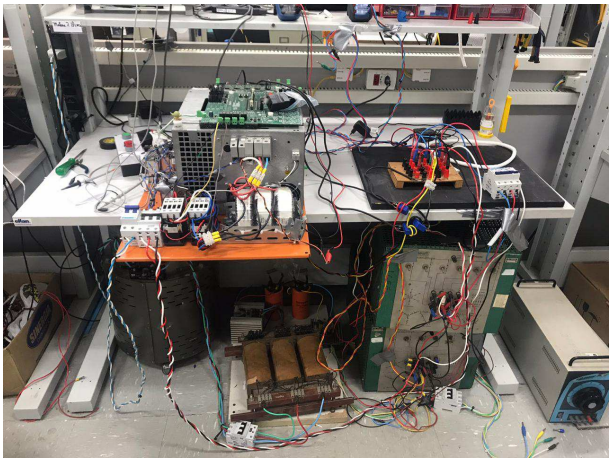

Figure B.3 – Experimental prototype assembled in LCEE.

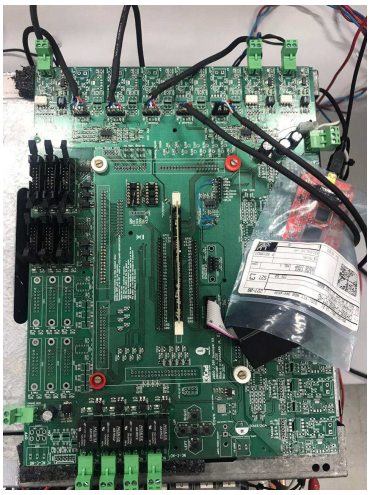

Figure B.4 – Control and acquisition Board.