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Faculdade de Engenharia Elétrica e de Computação

Rafael Oliveira Nunes

Study of Electromigration in Integrated Circuits at Design Level

Estudo da Eletromigração em Circuitos Integrados na Fase de Projeto

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“And without faith it is impossible to please God, because anyone who comes to him must believe that he exists and that he rewards those who earnestly seek him.”

(Hebrews 11:6)

Abstract

Electromigration damage in interconnects is a well-known bottleneck of integrated circuits, because it causes reliability problems. Operation at high temperatures and current densities accelerates the damage, increasing the interconnect resistance and, therefore, reducing the circuit lifetime. This issue has been accentuated with the technology downscaling. To guarantee the interconnect reliability and, as a consequence, the integrated circuit reliability, traditional methods based on the so-called Blech Effect and on the maximum allowed current density are implemented during interconnect design. These methods, however, do not take into account the impact of the electromigration on the circuit performance.

In this work the traditional approach is extended and a method to evaluate the effect of the electromigration in an integrated circuit performance is developed. The method is implemented in a tool which identifies the critical interconnect lines of an integrated circuit and suggests the proper interconnect width based on different criteria to mitigate the electromigration damage and to increase the reliability. In addition, the variation of performance parameters of the circuit as an interconnect resistance changes is determined. The tool is incorporated into the design flow of the integrated circuit and uses the data from design kits and reports directly available from the design environment.

An accurate analysis of the temperature distribution on the interconnect structure is essential to a better assessment of the interconnect reliability. Therefore, a model to compute the temperature on each metallization level of the interconnect structure is implemented. The temperature distribution on the metallization layers of different technologies is investigated. It is shown that the temperature in the Metal 1 of the Intel 10 nm can increase by 75 K, 12 K higher than in the Metal 2. As expected, the layers that are closer to the transistors undergo a more significant temperature increase.

The tool is applied to evaluate the interconnects and the robustness of different circuits, namely a ring oscillator, a bandgap voltage reference circuit, and an operational amplifier, against electromigration. The operational amplifier, in particular, is thoroughly studied. The proposed methodology identifies critical interconnects which under electromigration cause large variations in the performance of the circuit. In a worst-case scenario, the cutoff frequency of the circuit varies by 65% in 5 years of operation. An interesting finding is that the proposed methodology identifies critical interconnects which would not be identified by the traditional criteria. These interconnects have current densities below the limit recommended by the design rules. Nevertheless, one of such an interconnect leads to a variation of 30% in the gain of the operational amplifier. In summary, the proposed

tool verified that from the 20% paths with a critical current density, only 3% degrades significantly the circuit performance.

This work brings the study of the reliability of the interconnects and of integrated circuits to the design phase, which provides the assessment of a circuit performance degradation at an early stage of development. The developed tool allows the designer to identify critical interconnects which would not be detected using the maximum current density criterion, leading to more accurate analysis of the robustness of integrated circuits.

Keywords: electromigration; interconnect; reliability; integrated circuit design.

Resumo

O dano por eletromigração nas interconexões é um gargalo bem conhecido dos circuitos integrados, pois causam problemas de confiabilidade. A operação em temperaturas e densidades de corrente elevadas acelera os danos, aumentando a resistência da interconexão e, portanto, reduzindo a vida útil do circuito. Este problema tem se acentuado com o escalonamento da tecnologia. Para garantir a confiabilidade da interconexão e, como consequência, a confiabilidade do circuito integrado, métodos tradicionais baseados no chamado Efeito Blech e numa densidade de corrente máxima permitida são implementados durante o projeto da interconexão. Esses métodos, no entanto, não levam em consideração o impacto da eletromigração no desempenho do circuito.

Neste trabalho, a abordagem tradicional é estendida e um método para avaliar o efeito da eletromigração no desempenho de circuito integrado é desenvolvido. O método é implementado em uma ferramenta que identifica as interconexões críticas em um circuito integrado e sugere larguras adequadas com base em diferentes critérios para mitigar os danos à eletromigração e aumentar a confiabilidade. Além disso, é determinada a variação dos parâmetros de desempenho do circuito conforme a resistência das interconexões aumenta. A ferramenta é incorporada ao fluxo de projeto do circuito integrado e usa os dados dos *kits* de projeto e relatórios diretamente disponíveis no ambiente de projeto.

Uma análise precisa da distribuição de temperatura na estrutura de interconexão é essencial para uma melhor avaliação da confiabilidade da interconexão. Portanto, é implementado um modelo para calcular a temperatura em cada nível de metalização da estrutura de interconexão. A distribuição de temperatura nas camadas de metalização de diferentes tecnologias é investigada. É mostrado que a temperatura no Metal 1 da tecnologia Intel 10 nm aumenta 75 K, 12 K mais alta que no Metal 2. Como esperado, as camadas mais próximas dos transistores sofrem um aumento de temperatura mais significativo.

A ferramenta é aplicada para avaliar eletromigração nas interconexões e na robustez de diferentes circuitos, como um oscilador em anel, um circuito gerador de tensão de referência tipo *bandgap* e um amplificador operacional. O amplificador operacional, em particular, é cuidadosamente estudado. A metodologia proposta identifica interconexões críticas que quando danificadas por eletromigração causam grandes variações no desempenho do circuito. No pior cenário, a frequência de corte do circuito varia 65% em 5 anos de operação. Uma descoberta interessante é que a metodologia proposta identifica interconexões críticas que não seriam identificadas pelos critérios tradicionais. Essas interconexões operam com densidades de corrente abaixo do limite recomendado pelas regras de projeto. No entanto, uma dessas interconexões leva a uma variação de 30% no ganho do amplificador operacional. Em resumo, a ferramenta proposta verificou que dos 20% de

caminhos com uma densidade crítica de corrente, apenas 3% degradam significativamente o desempenho do circuito.

Este trabalho traz o estudo da confiabilidade das interconexões e de circuitos integrados para a fase de projeto, o que permite avaliar a degradação do desempenho do circuito antecipadamente durante o seu desenvolvimento. A ferramenta desenvolvida permite ao projetista identificar interconexões críticas que não seriam detectadas usando o critério de densidade máxima de corrente, levando a uma análise mais ampla e precisa da robustez de circuitos integrados.

Palavras-chaves: eletromigração; interconexão; confiabilidade; projeto de circuito integrado.

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List of Abbreviations and Acronyms

ADE	Analog design environment
BEOL	Back-end-of-line
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
C.$\Delta R/R_0$	evaluation of the paths for the maximum resistance change
C.j	evaluation of the paths for the maximum current density
C.jL	evaluation of the paths for the Blech product
DRC	Design ruler checker
DUT	Device under test
EAD	Electrically aware design
EM	Electromigration
ESD	Electrostatic discharge
Fc	Cut-off frequency
FC	Flip chip
FreePDK45	Open-Access-based PDK for the 45nm technology node
FEM	Finite element method
FEOL	Front-end-of-line
GPDK	Generic process design kit
GPU	Graphics processing unit
HCI	Hot carrier injection
HDL	Hardware description languages
IC	Integrated circuit
IP	Intellectual property

ITRS	International Technology Roadmap for Semiconductors
JH	Joule heating
LPF	Lines prone to failure
LVS	Layout Versus Schematic
MTTF	Mean time-to-failure
NBTI	Negative bias temperature instability
PBTI	Positive bias temperature instability
PPF	Paths prone to failure
REF	Reference
SM	Stressmigration
SoC	System on a chip
SPICE	Simulation Program with Integrated Circuit Emphasis
ST	Settling time
TDDB	Time-dependent dielectric breakdown
TM	Thermomigration
TTF	Time-to-failure
UGF	Unit gain frequency
ULK	Ultra low-k dielectric
ULSI	Ultra large-scale integration
VBG	Voltage bandgap
VHDL	VHSIC Hardware Description Language
XFAB	X-FAB Silicon Foundries

List of Symbols

A	Corss-sectional area of the interconnect metal
A_b	Cross-sectional area of the barrier layer
A_{int}	Area occupied by the metals in a layer
A_m	Constant which comprises the material properties and the geometry of the interconnect
a_r	Aspect ratio, the average ratio of the length and the thickness of the interconnect lines
A_{via}	Area occupied by the vias in a layer
c	Concentration of atoms
D	Diffusivity
D_0	Pre-exponential factor dependent on the diffusion mechanisms
e	Elementary charge
E_a	Activation energy
F	Fraction of diffusing atoms for the various diffusion paths
f_c	Cutoff frequency
g_m	Transconductance
h	Thickness of the interconnect lines
h_0	BEOL total thickness
I	Electrical current
j	Current density
j_{acel}	Current density used in accelerated tests
j_{max}	Maximum current density
J_E	Flux of metal atoms due to EM
jL	Blech product

jL_c	Blech product threshold
k	Boltzmann's constant
k_i	Thermal conductivity of the insulator
k_m	Thermal conductivity of the metal
k_{eff}^{beol}	Effective thermal conductivity of the BEOL
k_{eff}^{int}	Effective thermal conductivity of the metal
k_{eff}^{via}	Effective thermal conductivity of the via
L	Length of the interconnect lines
L_n^{int}	Height of the interconnects for a particular layer n
L_n^{via}	Height of the vias for a particular layer n
l_v	Length of the void
m	Total number of interconnect layers
$MTTF_{acel}$	Interconnect lifetime considering the results obtained from accelerated tests
$MTTF_{use}$	Interconnect lifetime estimated for normal use conditions
n	Current density exponent
N_{via}	Number of vias
P_T	Power dissipated by transistors
T	Temperature
T_0	Reference temperature
T_{acel}	Temperature used in accelerated tests
T_{max}	Maximum temperature in the interconnect lines
t_b	Diffusion barrier thicknesses
v_{EM}	Atomic drift velocity due to the EM driving force
V_{int}	Volume fraction of the metal lines
V_{TH}	Threshold voltage

V_{via}	Volume fraction of the vias
w	Width of the interconnect lines
W_j	Calculated width of the metal lines for the maximum current density
W_{jL}	Calculated width of the metal lines for the Blech product
W_r	Calculated width of the metal lines for the maximum resistance change
w_{min}	Minimum width of the technology
W_{via}	Width of the vias
w_b	Width of the diffusion barrier
z	Distance in the BEOL from heat source
Z^*	Represents the sign and the magnitude of the momentum transfer between the conducting electrons and the metal atoms
α	Linear temperature coefficient of the metal
α_b	Linear temperature coefficient of the barrier layer resistivity
η	Dimensionless parameter used to estimate the k_{eff}^{int}
β	Dimensionless parameter used to estimate the k_{eff}^{int}
ΔR	Resistance variation
$\Delta R/R_0$	Resistance change ratio
$(\Delta R/R_0)_{crit}$	Critical resistance change ratio
Δt	Time variation
ΔT_{acel}	T_{acel} variation in relation to the reference temperature
ΔT_{PT}	temperature change in metallic layer due to the P_T
ΔT_{use}	T_{use} variation in relation to the reference temperature
Ω	Atomic volume
ϕ_{int}	Volume fraction of the metal layers
ϕ_{via}	Volume fraction of the via layers
ρ_b	Resistivity of the barrier layer

ρ	Resistivity of the interconnect metal
ρ_0	Resistivity at the reference temperature
σ_0	Initial stress in the metal line
σ_{th}	Maximum stress the metal line can withstand

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1 Introduction

In this chapter, the aspects that lead the electromigration (EM) to be a critical issue for integrated circuits (ICs) is presented. The increased importance of the EM with the technology development is described based on the International Technology Roadmap for Semiconductors (ITRS) reports. These reports have motivated the EM research resulting in an increased number of publications in leading IC magazines and conferences. As a consequence, the reliability analysis of ICs becomes more accurate at each new technology node.

1.1 Brief Overview of Integrated Circuits' Reliability

Reliability is the quality of being trustworthy or of performing consistently well [3]. The reliability evaluation of an IC is a complex task and should be taken into account during the design, fabrication, and test procedures. The continuous improvement of the failure rates to extend the chip lifetime intensifies the reliability evaluation complexity [4]. The semiconductor industry considers new procedures to maintain the IC reliability at each new technology node, as the EM effects and other issues become more relevant in a smaller chip with a higher density of devices [5–7].

Extreme environmental conditions of radiation, pressure and temperature affect the reliability of ICs and shorten the chip lifetime. In 2016, NASA engineers evaluated an IC under a temperature (460 °C) and a pressure (9.4 MPa) similar to Venus [8]. Figure 1.1 shows that the IC was significantly deteriorated after 521 hours, but still maintained its functionality at the end of the test. The success of the interplanetary expeditions is highly dependent on the reliability of ICs.

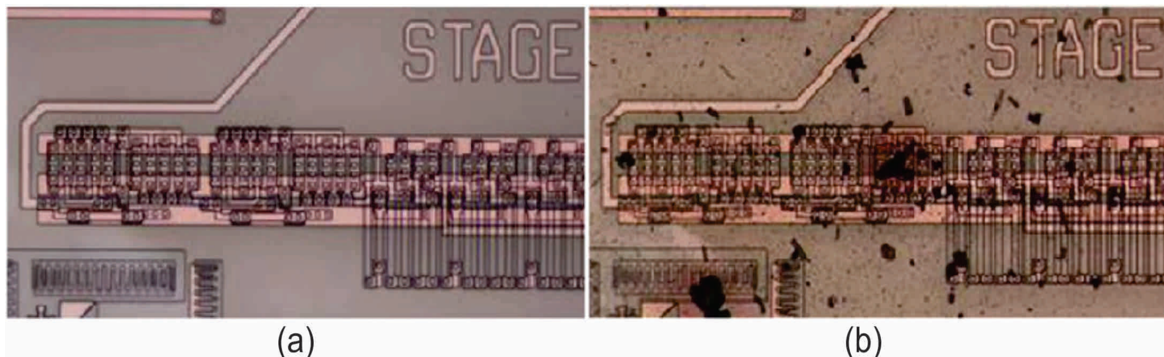

Figure 1.1 – Electronic circuit before (a) and after (b) be evaluated under harsh conditions similar to Venus [8].

Figure 1.2 shows the three typical stages of a reliability bathtub curve of a chip. At the infant mortality stage, the failure rate increases, reaches a maximum value and then decreases [9]. During the regular operation stage, the chip suffers random failures and the failure rate is normally insignificant. It is important to note that the regular phase is longer for military and space than for commercial applications. At the wearout stage, the failure rate increases due to the aging effects. With the introduction of new technology nodes, the wear-out failure curve moves to the left, which means earlier device degradation and reduced chip lifetime, as shown in Figure 1.3 [9].

The aging effects of a chip is a consequence of different stress sources, mainly mechanical, thermal, and electrical. Nevertheless, improvements in the fabrication and design methodology minimize these effects [10–12]. In the design phase, the designer analyzes the aging effects and adjust the circuit using electronic design automation (EDA) tools. In practice, these tools allow the designer to choose the devices, architectures, geometries of the interconnects and transistors and, most fundamentally, to simulate the voltage, current, temperature and other stimuli applied to the circuit during operation. As long as the EDA tools are systematically released to incorporate new methods and models, the IC designer considers different aging effects in the circuit analysis.

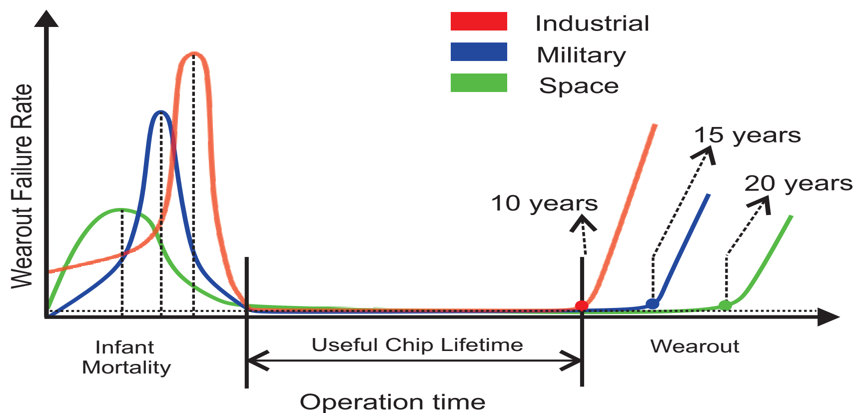

Figure 1.2 – Reliability bathtub curves of a chip for different applications [9].

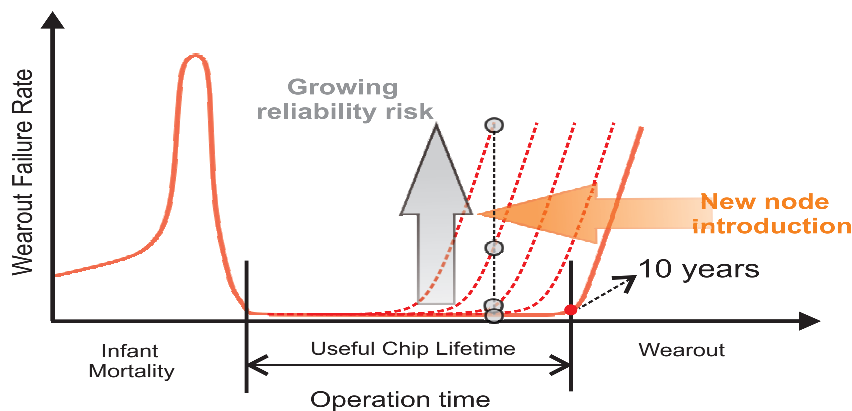

Figure 1.3 – Bathtub curve change with the introduction of a new technology node [9].

Although the cost of chip production, including the expenses with wafer, mask, test, and package increased with the technology downscaling, the relative cost to produce a transistor decreased. Figure 1.4 shows the chip cost per transistor evolution with the technology [13, 14]. Observe that the transistor cost in an advanced circuit, such as graphics processing unit (GPU), central processing unit (CPU), or system on a chip (SoC), reduced 12.5 times from 65 nm to 10 nm technology. The higher density of transistors in the new technologies compensates for the increased cost to create a new advanced circuit. As a result, the relation dollar per transistor, named relative cost, reduces in each new technology node.

The IC design corresponds to a significant percentage of the cost to create a new advanced circuit. Figure 1.4 shows the IC design evolution in four groups: software, verification, physical and other [13]. The group named other involves the prototype, validation, architecture, and intellectual property (IP) qualification. Note that the investment to design a chip depends on the technology used. While the cost to design in 40 nm is 37.7 million dollars, in 10 nm, this value increases to 174.4 million, 4.6 times more expensive. The increased investments are due to the need to guarantee the reliability of the circuits in modern technologies.

The number of publications in the leading microelectronic journals and conferences denotes the relevance of the research on IC reliability. Figure 1.5 shows the number of publications in the IC reliability field in three periods organized into three groups: device, interconnect, and the other, the latter referring to circuit-level reliability and electrostatic discharge (ESD) reliability, for example [15]. Together with the significant increase in the number of publications regarding IC reliability, the reliability of interconnects became the

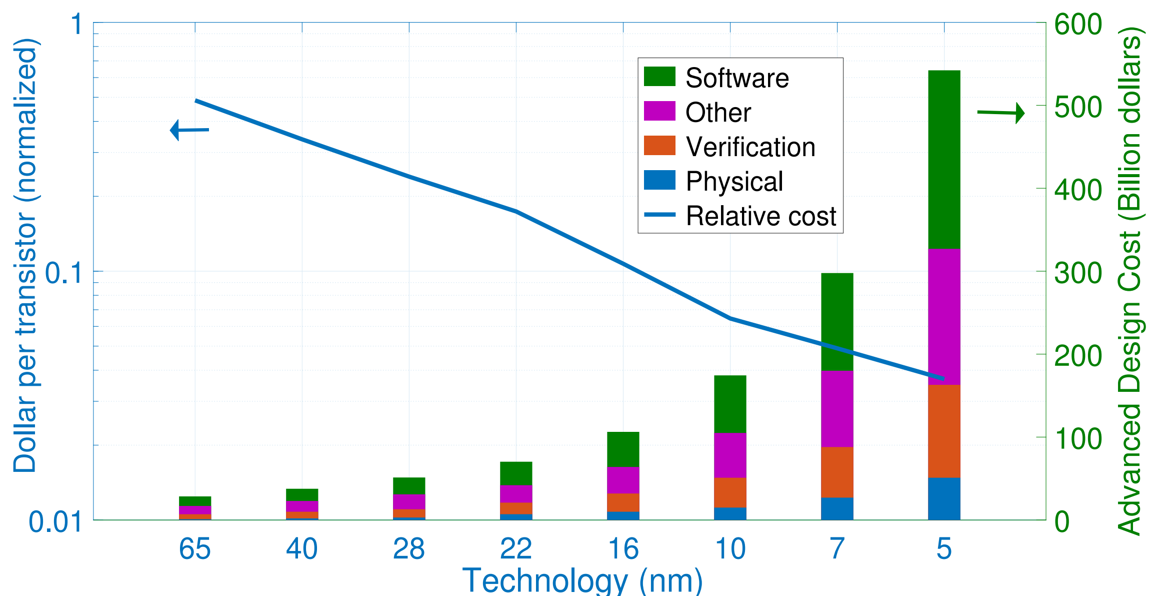

Figure 1.4 – Costs of transistors and EDA tools for different technology nodes [13, 14].

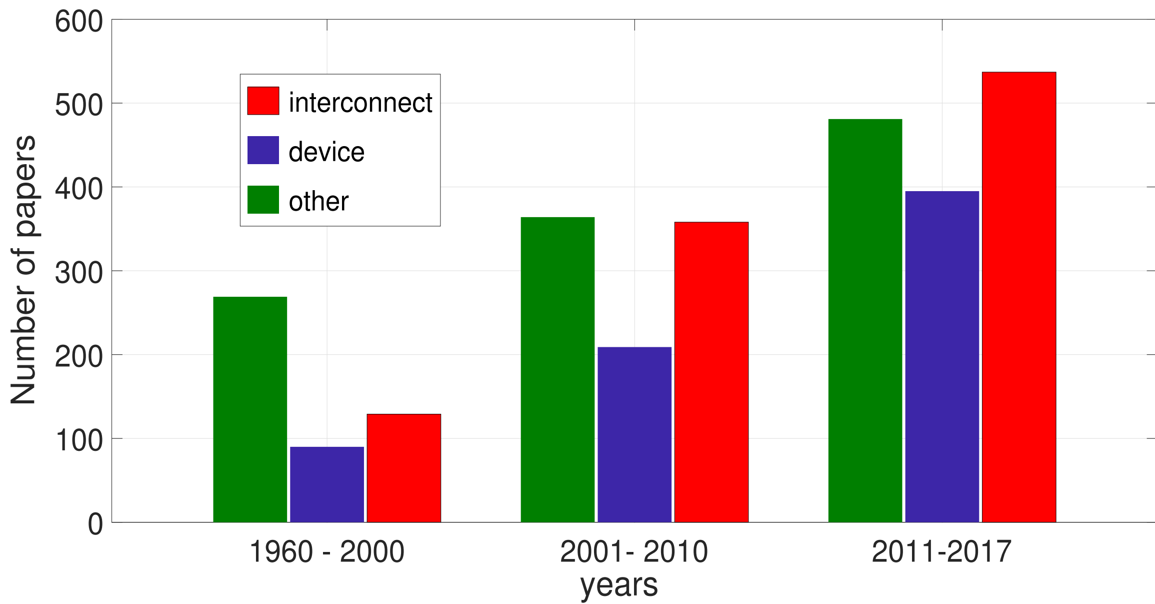

Figure 1.5 – Number of papers published in leading journal and conferences related to IC reliability [15].

most studied subject, with 38% of the publications in the period 2011 to 2017.

Hot carrier injection (HCI), negative bias temperature instability (NBTI), in addition to positive bias temperature instability (PBTI) and time-dependent dielectric breakdown (TDDB) are degradation effects that cause aging in the transistors. Below 90 nm, the analysis of these effects is a requisite for design flows targeting quality and reliability [16]. These reliability effects modify essential parameters, such as the threshold voltage and the mobility factor [17]. These changes affect timing delays, power, frequency, leakage, linearity, gain, and every possible specification that may appear in digital, analog, or RF design.

Electromigration, stressmigration, and thermomigration are aging effects in interconnects. Discovered by Gerardin in 1861, the electromigration became well-known in the 1960s, when on-chip aluminum (Al) interconnects were observed to fail in the presence of electric current [18, 19]. In the 1980s, the degradation of the interconnects due to the stress gradients became an important issue [20]. This failure mechanism, named stressmigration, is driven by the hydrostatic stress gradient generated in the lines and does not require electron flow to occur. In turn, the thermomigration is the failure mechanism due to the presence of a thermal gradient [21]. In general, the combinational effect of stressmigration, thermomigration, and electromigration cause line failure.

The semiconductor industry used different materials in the integrated circuit to boost circuit performance and reliability. Al lines were the industry standard until 1997, when IBM introduced the copper (Cu) interconnect technology [22]. With the reduction

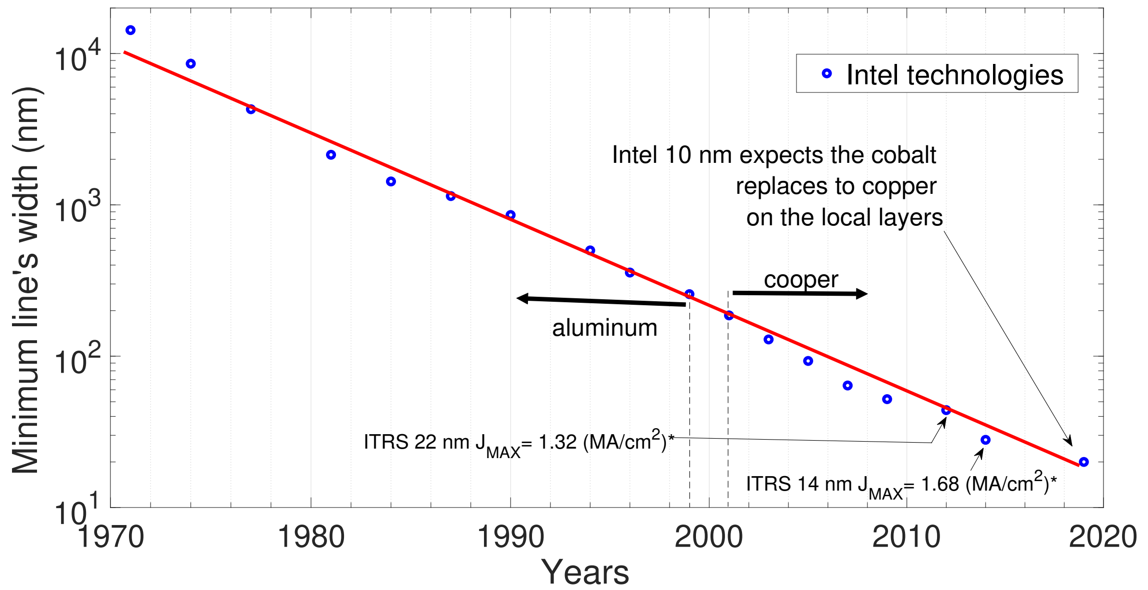

Figure 1.6 – Evolution of the minimum interconnect width in five decades based on Intel processors, from the 10 μm until the 10 nm technology node [24].

of the interconnect dimensions, Cu interconnects became more appropriate, since Cu is a better conductor than Al. Cu lines reduce the propagation delays and power consumption leading to ICs with better performance. The transition from Al to Cu leads to significant developments of the fabrication techniques, including the introduction of tantalum (Ta) and tantalum nitride (TaN) barrier metal layers to isolate the silicon from the Cu atoms [23].

Figure 1.6 shows the evolution of the minimum interconnect width in five decades based on Intel processors, from the 10 μm until the 10 nm technology node [24]. As the metal line width was reduced, the current density through them increased. The maximum current density estimated by ITRS was 1.32 MA/cm^2 for 22 nm technology. For 14 nm, the maximum current density increased to 1.68 MA/cm^2 [25]. Although the IC's became more compact with better performance, the interconnect shrinking resulted in a more severe EM, as the elevated current density accelerates the EM damage [26–28].

The high compatibility and gain of performance with the interconnect and transistor shrinking is better observed in advanced circuits, like microprocessors. Figure 1.7 illustrates the power, frequency and number of transistors in microprocessors with the technology evolution [29]. There are two interesting points to note. First, power and frequency change became flat after 2005, with the development of the multi-core processors, an essential condition to maintain a lower temperature and improve chip reliability. Second, the transistor count still follows the exponential growth line, following Moore's Law for five decades with some adjustments.

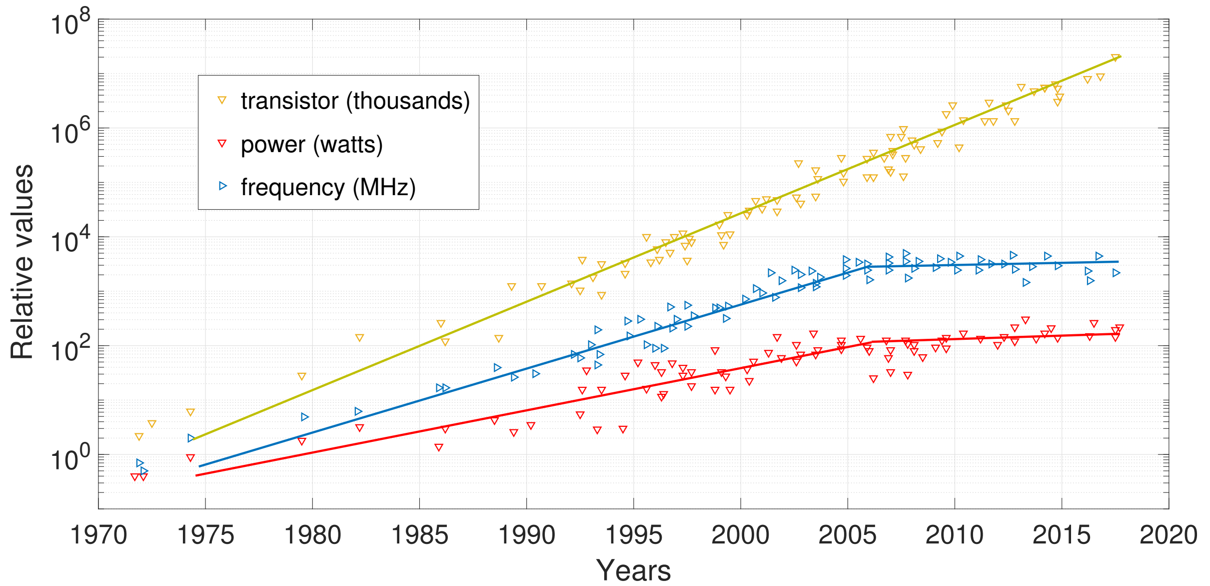

Figure 1.7 – Evolution of power, frequency and number of transistors in microprocessors with the technology evolution [29].

1.2 Integrated Circuit Scaling

The interconnect resistance increase with the metal line shrinking degrades the RC delay and the signal propagation. As the RC delay of the interconnect becomes longer than the gate delay for technologies below 100 nm, the reduction of the capacitance of the interconnects becomes a priority [30]. In order to reduce the capacitance and to achieve an RC delay target, the recent technologies employ insulators with lower dielectric constants. Ultra low-k (ULK) dielectrics applied in high-performance circuits below the 65 nm technology minimize the capacitance and, as a consequence, the RC delay and the cross-talk [31].

Besides the dielectric constant reduction, the attenuation of the RC delay increase includes the use of thinner barriers, the reduction of the line sheet resistance and the improvement in circuit design. A thinner barrier maximizes the copper volume and minimizes the line resistance increase. In turn, the use of copper alloy reduces sheet resistance in comparison to aluminum alloy. In terms of circuit design, the signal propagation along the line improves with the introduction of repeaters within the interconnects and the use of interconnect line shielding techniques [32].

1.3 Back-end-of-line and Front-end-of-line Structures

Figure 1.8 shows the front-end-of-line (FEOL) and back-end-of-line (BEOL) of a chip structure [33]. The BEOL composes the solder bump used for flip-chip (FC)

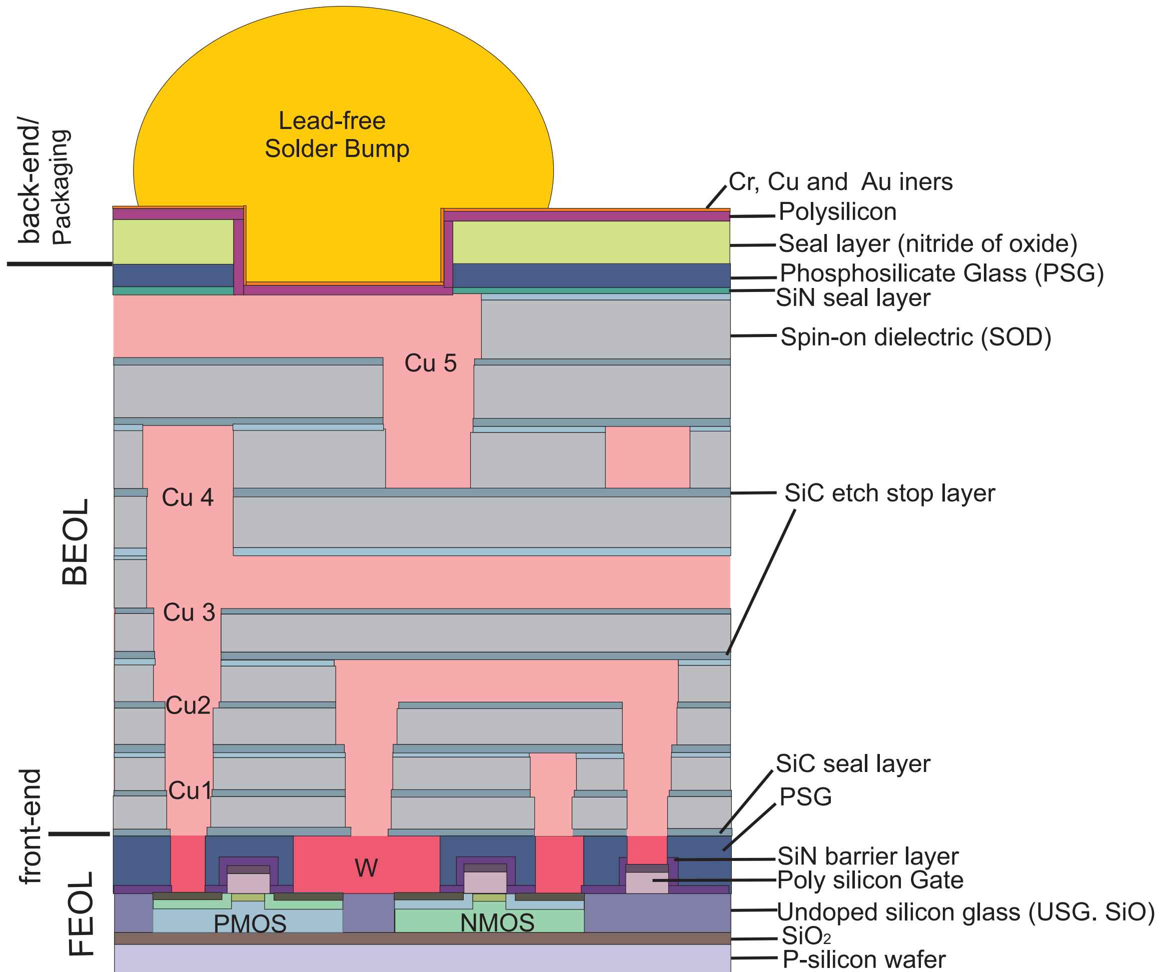

Figure 1.8 – FEOL and BEOL of a CMOS chip structure [33].

bonding, connecting the chip and substrate and also providing a heat dissipation path from the chip. Below the solder bump, a more extensive passivation layer protects the chip from the moisture and external impact. The BEOL corresponds to the region forming the interconnects layers, including dielectric insulators and metal/via layers. The FEOL corresponds to the devices in the substrate, transistors, capacitors, resistors, and inductors. The primary purpose of the BEOL is to realize the interconnection of the devices in the FEOL.

Advanced BEOL processes generally prescribe a maximum number of metalization layers, including the local, intermediate, and global lines. Each of these lines have different thicknesses based on their electrical functions. The local lines connect the circuit elements that are close to each other, and have the tightest linewidths and the roughest topography [30]. The local lines are generally subjected to the highest temperatures, since they are the nearest from the active area. In turn, the global layers distribute the supply voltage and transmit the clock and global signals of the chip. As the global lines conduct the highest currents of the circuit, these lines are fabricated with larger dimensions to avoid the EM.

While the vias connect the different metalization layers, the contact plugs connect the device in the substrate to the first metal layer. In Figure 1.8, tungsten (W) and Cu fill the contact plugs and vias, respectively. Tungsten is used to fill plugs due to the high thermal conductivity and low thermal expansion [34]. As the contact plugs are filled with a material different from the Cu interconnects, a separate step is required to fill the contact plugs. Besides via and contact layers, the BEOL contains interlayer dielectrics, barrier layers, adhesion layers, plug layers, and a passivation layer.

1.4 Electromigration Damage on the Wires

As described in the last section, the aging effects on the interconnect wires are of main concern for IC reliability. The understanding of EM is crucial for designing reliable IC's in modern technologies. Under EM, the wire is affected by hillocks and voids, where the first leads to short circuits and the last in an increased interconnect resistance or even open circuits [35].

Figure 1.9 illustrates an interconnect line under EM. The electrons through the line displace the Cu atoms to the anode end of the line creating a void on the cathode end of the line. With the continuous electron flow, the void size increases and the current path becomes more resistive. Depending on the affected line, the resistance increase affects the circuit performance seriously.

The resistance change of an interconnect due to EM can be described by two phases: a step and a linear phase [36]. In the step phase, the current initially flows through the Cu, until the void spans the line thickness and forces the current to pass through the more resistive barrier layer, generally made from Ta/TaN. In the linear phase, the current flows through a larger length in the barrier, as the void grows along the line. Since the line resistance continues to increase, a critical resistance change is used to determine the line failure.

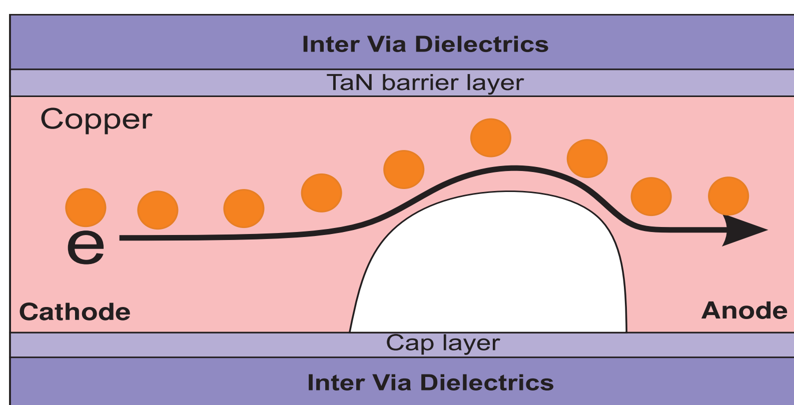

Figure 1.9 – Illustration of a void formed in an interconnect line under EM [36].

1.5 State of the Art of Interconnects and Electromigration

The continuous shrinking of IC's challenges the semiconductor industry to meet the interconnect scaling roadmap. First, the scaling of interconnect dimensions raises the conductor resistance as well as the capacitance to adjacent lines, thus affecting the chip performance [37–39]. Also, the Cu line resistivity is expected to increase significantly because of electron scattering at the interfaces and grain boundaries [40–42]. Second, in the traditional Cu dual-damascene technology [43], Cu requires a TaN/Ta diffusion barrier [44–46]. The presence of the barrier reduces the Cu fill area since it is difficult to further scale the diffusion barrier at such small dimensions [47, 48]. Third, scaled wires operate under higher current densities, accelerating the effect of EM. Therefore, alternative conductors are currently under investigation to replace Cu and further boost the performance demanded by advanced technology nodes [37, 49–51].

Figure 1.10 illustrates a typical Cu interconnect made of TaN diffusion barrier and Ta adhesion liner extensively used in modern technologies. According to the ITRS roadmap, the wire has the width, spacing, pitch and thickness dimensions fabricated 0.7 times smaller at each new technology node [53]. Since the Ta/TaN barrier and liner layers reach thicknesses below 2 nm, following the estimated ITRS scaling for technologies below 10 nm become extremely difficult, as the thinner barrier reduces its blocking capability to avoid Cu diffusion into the Si substrate. In addition, the Cu lines have larger resistances for interconnects below 10 nm technology, resulting in a high voltage drop along the interconnect [54, 55]. Also, the Cu lines are more susceptible to EM in modern technologies, as the current density increases with the technology evolution. As the wires shrinking exposes Cu and TaN/Ta limitations, the semiconductor industry has evaluated potential replacements.

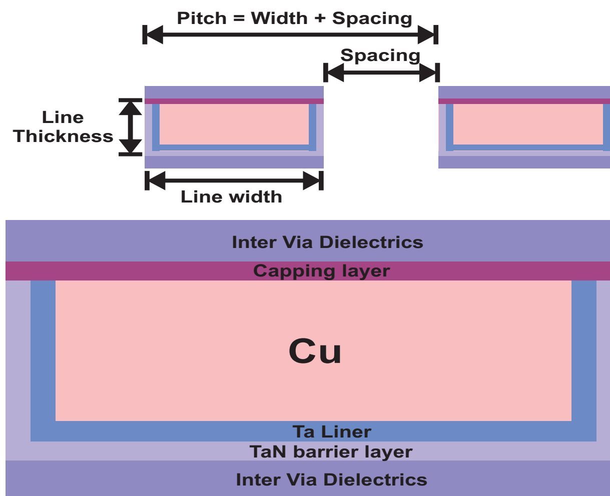

Figure 1.10 – Typical Cu interconnect made of a TaN diffusion barrier and a Ta adhesion liner [52].

Ruthenium (Ru) and cobalt (Co) are candidate materials to replace the Cu filling in interconnects and vias and also in TaN diffusion barriers and Ta liners [56–59]. In 2018, Intel adopted Co to replace Cu lines in local interconnects of a 10 nm technology. Co lines support larger current densities without reliability degradation [60–63], resulting in a significant improvement for EM. Also, Co has been used in recent studies as a replacement for tungsten (W) in the vias, which yields a less resistive path [40]. In turn, Ru interconnects have demonstrated potential for thinner barrier or barrierless integration [43, 64]. The TaN/Ta occupies a larger proportional area of the interconnect section with the technology scaling. Therefore, the substitution of Cu to Co allows using a barrier with smaller dimensions. Ru and Co have been evaluated to replace the Ta as liner materials as they have excellent adhesion to Cu and are thermodynamically stable [56, 65].

In addition to the improvements in interconnect manufacturing, some studies evaluate aspects that affect the EM at the design level. Ref. [66] shows that the lines can be structured into different layout topologies to reduce the EM . Ref. [67] shows that pin positions in a standard cell can be optimized to increase cell lifetime concerning EM. In a benchmark circuit test, the lifetime has increased more than twice [67]. Ref. [68] shows that the impedance mismatch of a driver complementary metal-oxide-semiconductor (CMOS) and driven transmission lines substantially aggravates EM and Joule heating on these lines. Ref. [69] evaluates the impact of cross noise between two adjacent lines under EM and Joule-heating on ultra large-scale integration (ULSI) chip. The cross noise becomes more critical in the today's circuits, which are more compact, with a more significant number of interconnections and a shorter distance between them. All of these analyzes allow the designer to understand how to improve integrated circuit design to mitigate the EM risks.

The methodologies to evaluate EM in the digital and analog designs are different. The digital tools automize all the design flow generating the layout automatically based on the performance expected to the circuit. In turn, the analog tools are semi-automatic and require from the designer the know-how from the physical characteristics of the circuit. The analog designer sizes manually the interconnects in the construction of the layout as also choose different metal layers.

Lines that carry AC and DC currents present differences in the intensity of the EM. The EM is more significant in the lines that supply DC voltage, which generally carry the highest current. Due to their mostly unidirectional currents, the DC lines not suffer the self-healing, a beneficial process where a current change the direction, retarding the EM effects. Signal and clock lines that transport AC signal takes advantage of the self-healing process. Nonetheless, with the current density increase, all the lines carrying

AC or DC signal are subject to the EM.

Many studies describe the need for physics-based models considering the particularities of the circuit, not just current density-based models [70–74]. The physical models which take into account variations in temperature and process in the chip, improve the reliability evaluation accuracy compared with the traditional models. [70]. Traditional EM models have two disadvantages. First, they do not accurately model the degradation of the line, and second, they do not consider the resilience in a circuit that can continue to function even after some wires fail [75, 76].

1.6 Thesis Statement and Contributions

To guarantee the interconnect reliability and, as a consequence, the IC reliability, the EDA tools use traditional methods based on the Blech Effect and on the maximum allowed current density during interconnect design [77–81]. The Blech Effect refers to the back flow of atoms due to mechanical stress gradients, which reduces or even compensates the flow due to EM. The base of these methods generally proceeds from the EM tests results with single lines under extreme conditions of temperature and current density. These results are used to define the maximum current density a line can carry for a given technology, and the threshold is considered in the process of chip design and interconnect sizing. However, these conventional methods do not take into account the impact of EM on the circuit performance.

Limitations in the traditional methods motivated the creation of different procedures to turn the EM analysis more accurate [79, 82–84].Nonetheless, these procedures are extensions of the Blech Effect and the current density thresholds and do not focus on IC performance. As a complement to the traditional methods, a method based on the circuit performance improves the EM analysis accuracy, helping the designer to identify the critical lines and resize those to guarantee adequate circuit performance and reliability.

In the scope of this work, we develop a method to identify the critical lines due to EM in an IC at design level. In this way, it is possible to evaluate the metal lines during the design and it allows the designer to resize the lines that are prone to failure. The method is based on the traditional and the resistance change criteria. The principal contributions of this thesis are:

- A method to evaluate the IC performance degradation due to void growth in the lines is provided. The method complements the traditional methods, which relies only on the current density through the lines.
- A method to identify the critical lines in an IC is proposed.

- A method to size the lines based on the traditional and the resistance change criteria is provided. Generally, the designer uses the current density threshold to design the lines.

- The time to failure of the lines based on the maximum resistance change is used to evaluate the circuit performance degradation at design level.

- A method to identify the critical blocks of a circuit considering the temperature distribution on the metal layers is developed.

1.7 Outline of the Thesis

In Chapter 2, the main concepts related to the EM is explained. Initially, the current density and the temperature influence on the EM-induced resistance change of the interconnects is described. Then, the resistance change is used to evaluate the time to an interconnect line failure. The last section briefly describes the statistical distribution related to the EM failure.

In Chapter 3, the methodology to evaluate the EM impact on an IC at the design level is explained. First, the procedures to calculate the resistance change of the lines due to EM is described. Then, the effect of the EM on the performance parameters of an IC is discussed, followed by the description of methods to identify the critical interconnect lines as well as to estimate their widths based on the EM criteria. Finally, the full methodology flow to evaluate the EM impact on an IC and size the interconnect is presented.

In Chapter 4, the temperature change of the interconnect lines due to the transistor operation is investigated. First, the estimated temperature is compared with the temperature simulated with a finite element method (FEM) 2-D model. After, it shows the relation of the estimated temperature inaccuracies in the resistance ratio of the lines. The last session shows the evaluation of the critical circuits based on the temperature.

In Chapter 5, the EM computational tool is described, explaining the procedures to identify the critical lines, to classify the lines as oversized and undersized, and to estimate the width of the lines. The tool is used to evaluate the interconnects from an operational amplifier.

In Chapter 6, the performance of an operational amplifier, a bandgap voltage reference and a ring oscillator circuits under EM is evaluated. After it shows the mean time-to-failure (MTTF) model of a metal line based on the maximum resistance change. In the end, the EM on the 45 nm and state of the art technologies is evaluated. Finally, conclusions and future work perspectives are presented in the Chapter 7.

2 Fundamentals of Electromigration

In this chapter, the main concepts related to the EM is explained. Initially, the current density and the temperature influence on the EM-induced resistance change of the interconnects is described. Then, the resistance change is used to evaluate the time to an interconnect line failure. The last section briefly describes the statistical distribution related to the EM failure.

2.1 The Electromigration Phenomenon

Electromigration (EM) is an atomic displacement caused by collisions between atoms and electrons [85]. Electrons flowing through a metal film collide with the metal atoms producing a momentum transfer. The EM becomes relevant when the electric current is sufficiently high to produce a significant momentum transfer from the electrons to the atoms causing atomic migration. Then, the displaced metal atoms flow to the anode end of the line, in the same direction from the electron flow. At the same time, the lattice defects, named vacancies, flow in the opposite direction, i.e. in the direction of the current flow.

The EM also depends on the structural properties of the interconnects after the fabrication process. A metal lattice vibrates at any temperature above 0 K [86]. The atomic vibrations change the metal atoms positions from their equilibrium and cause electron scattering. A large number of scattering events leads to a significant momentum transfer to the atoms and produces distortions in the lattice. Larger distortions occur at sites with higher density of defects, such as regions with vacancies or in a grain boundary [87]. Grain boundaries are interfaces formed between grains with different crystal orientations. They can act as sinks or sources of lattice sites and are fast diffusivity paths for atomic transport [87]. Hence, the microstructure plays an important role for the EM.

The EM-induced transport is more predominant at interfaces or surfaces than at the bulk or grain boundary (GB) for Cu lines as a consequence of the diffusion mechanism [88]. Diffusion can occur through the bulk, GB, along the interfaces and the surface, as shown in Figure 2.1. Each of these paths has a specific activation energy to initiate the diffusion event, as shown in Table 2.1. The bulk has the highest activation energy, followed by the GB, interface, and the surface, in Cu lines. While the bulk diffusion typically requires the energy of 2.1 eV [89], the surface diffusion requires 0.7 eV [89]. The activation energy for interfacial diffusion depends on the interface materials. For typical Cu interconnects with TaN/Ta barriers and capping layers, the activation energy lies in

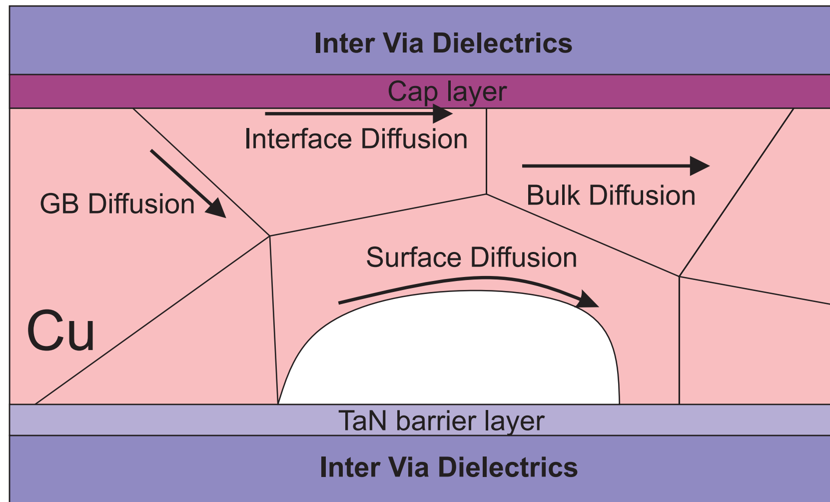

Figure 2.1 – Different diffusion paths in a line: through lattice, grain boundaries, along interfaces and surfaces.

Table 2.1 – Typical activation energies (E_A) for different EM diffusion paths in Al and Cu lines [89].

Diffusion process	E_A (eV)	
	Cu	Al
Bulk	2.1	1.4
Grain-boundary	1.2	0.6
Surface	0.7	NA
Interface	0.8-1.3	NA

the range 0.8-1.3 eV [89].

Note that Cu and Al have different activation energies for diffusion. Due to the higher melting point of Cu, its activation energy is also higher [85]. It is a common technique to introduce a small concentration of Cu in Al lines, which slows down the atomic transport due to EM [89]. The Cu doping acts as an inhibitor of Al migration, decreasing the drift velocity of the Al mass transport and increasing in the incubation time of the CuAl alloy interconnects. In turn, Al(1-2%) [85, 90], Ag (1%)[91], Mn(0.5-4%) [90, 92], Mg(2-4%) [93] and Sn(0.5-2%) [94] can also be introduced in a Cu line to retard the EM [85].

Due to EM, hillocks and/or voids can form in the wires, where the first may lead to short circuits and the last may lead to an increased resistance or even open circuits [85]. Figure 2.2(a) shows a void formed below the via. Figure 2.2(b) shows voids and hillocks formations at the cathode and the anode end of the line, respectively. Although the experimental observations generally indicate that voids and hillocks form in specific regions of the line, some studies show voids and hillocks formed all along the strip [95].

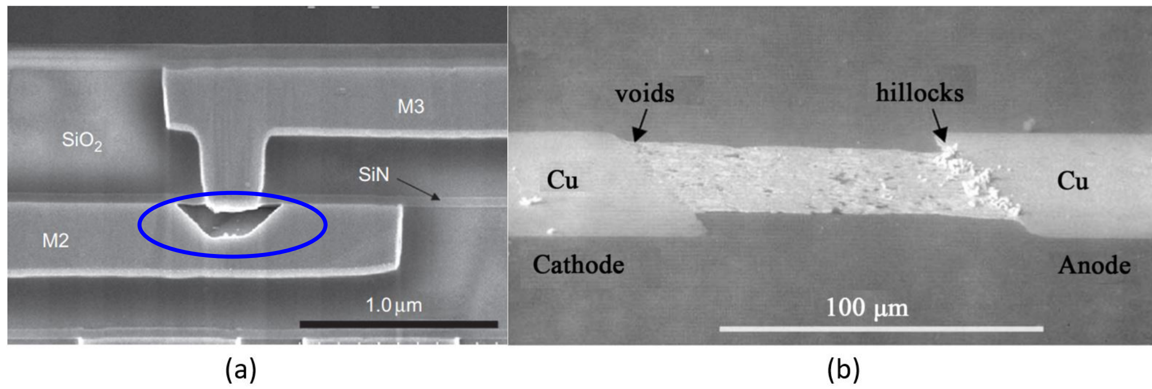

Figure 2.2 – Wire under EM. (a) Void below a via [100]. (b) Voids and hillocks formed at the cathode and anode end of the line [100].

In the technologies with metal line embedded into a rigid confinement [96–98], voids form earlier than hillocks . The earlier occurrence of voids makes void-induced degradation the main mechanism for EM failure [99].

Although there are methods of suppressing hillock formation in copper-containing conductive traces, improvements are always sought. Therefore, it would be advantageous to develop methods for fabricating copper-containing structures, such as conductive traces, which reduces or substantially eliminates hillock formation thereon.

The EM failure development is described by two distinct phases: a nucleation and a growth phase. During the nucleation phase no voids are visible and the resistance change of the line is very small [101]. A void is nucleated as soon as the mechanical stress reaches a critical magnitude [102]. After the void nucleates, the growth phase starts, where the void can evolve in several different ways until it finally grows to a critical size. In the growth phase, the line has a significant resistance increase or, a severing in a critical case, culminating in an open-circuit.

Accordingly, the EM lifetime given by the time for the void to nucleate plus the time for the void to develop can be obtained. When the nucleation is slow, and the growth is fast, the failure is nucleation dominated. If the nucleation is short, the growth has the primary influence in failure.

Figure 2.3 shows two typical failures cases in a Cu dual-damascene line [103]. In Figure 2.3(a), the nucleation phase dominates the line lifetime, where the void nucleates below the via, and failure occurs soon after nucleation. In Figure 2.3(b), the nucleated void first migrates towards the via and then grows to cause the failure. The last example is predominant in modern technologies, with the line failures dominated by the growth phase [104, 105].

Besides the EM, thermomigration (TM) and stressmigration (SM) are trans-

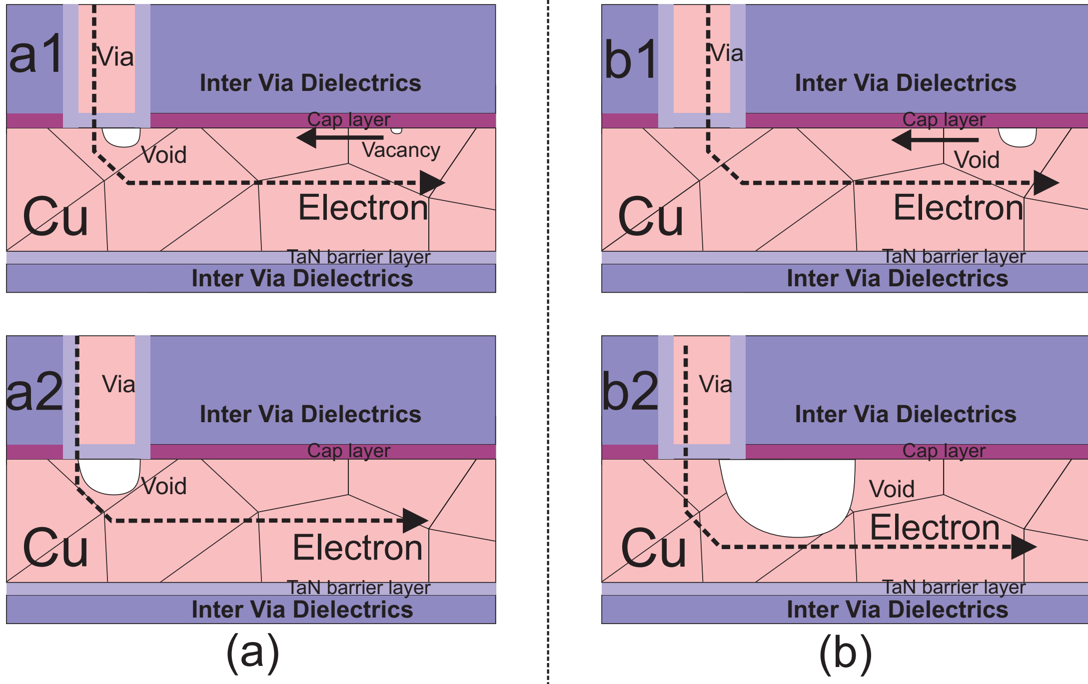

Figure 2.3 – Schematic of void formation in Cu during an EM stress for kinetics limited by (a) void nucleation and (b) void growth and migration.

port mechanisms in metal lines which can deteriorate the chip performance and reliability. The resultant atomic flux combines all the above mechanism and is defined by [106]

$$J = J_E + J_T + J_S + J_D, \tag{2.1}$$

where J_E is the EM-induce flux, J_T is the TM flux, J_S is the SM flux, and J_D is the diffusion flux due to gradients of atomic concentration.

In regions of flux divergence there is an accumulation of atoms (anode end of the line) or vacancies (cathode end of the line). The accumulation of vacancies builds up a tensile stress. If this tensile stress reaches a critical magnitude, a void is nucleated [107–111].

Under SM, atoms flow from regions of compressive stress to regions of tensile stress, thus vacancies flow in the opposite direction [112]. This atomic back-flux due to SM can eventually balance the EM flux in such a way that the net flux vanishes. Thus, there is no further accumulation of atoms and vacancies and the build-up of mechanical stress comes to a steady state. If this condition is reached before the critical stress for void nucleation is reached, there is no failure development. Besides EM, the mechanical stress generated during the interconnect fabrication process and deformation through packaging are the main reasons for the mechanical stress distribution and SM in the metal wires [113].

Under TM, the atoms flow from areas of high temperature to areas of lower temperature. Thus, the TM depends on the temperature gradient in the line, which is a function of the thermal properties of the metal and the insulation [113].

Each migration process affects the other mechanisms resulting in a positive or a negative feedback [113]. SM is a negative feedback to EM, as the atomic flow from compressive to tensile stress goes in the opposite direction to the EM flow. The resultant transport reduces and the migration of the atoms due to EM is retarded or even discontinued. The equilibrium between EM and SM was investigated by Blech, which yields a criterion to obtain the susceptible lines to EM failure [114]. In turn, the TM can acts as positive or negative feedback depending on the temperature gradient, which comes from different heat sources. In general, all these driving forces for atomic transport act together, resulting in a material transport along the interconnect line.

2.2 Impact of the Current Density

The flux of metal atoms (J_E) due to EM can be expressed by [115]

$$J_E = c \cdot v_{EM} = c \cdot D(T) \cdot \frac{Z^* e \rho(T) j}{kT}, \tag{2.2}$$

where c is the concentration of atoms, v_{EM} is the atomic drift velocity due to the EM driving force, $D(T)$ is the diffusion coefficient, Z^* is the so-called effective valence, or effective charge, which represents the sign and the magnitude of the momentum transfer between the conducting electrons and the metal atoms, $\rho(T)$ is the resistivity, e is the elementary charge, j is the current density, k is the Boltzmann's constant and T is the temperature.

The product of the effective charge and the diffusion coefficient is a function of different diffusion paths as expressed by [116]

$$Z^* D = Z^*_{GB} F_{GB} D_{GB} + Z^*_B F_B D_B + Z^*_S F_S D_S + Z^*_I F_I D_I, \tag{2.3}$$

where the subscripts GB, B, S and I refer to grain boundary, bulk, surface and interface, respectively. F corresponds to the fraction of diffusing atoms for the various diffusion paths [117, 118]. The fastest diffusion path has a lower activation energy and normally dominates the transport. As shown in Table 2.1, the dominant diffusion paths in Al and Cu lines are the grain boundary and the Cu/dielectric cap interface, respectively. In general, a higher activation energy improves the EM lifetime of the metal lines.

Given the proportionality between the EM flux and the current density, as shown by (2.2), the time-to-failure (TTF) due to EM is a function of the current density. An expression relating the mean time-to-failure (MTTF) of an interconnect due to EM is given by [119]

$$MTTF = \frac{A_m}{j^n} \exp\left(\frac{E_a}{kT}\right), \tag{2.4}$$

which is the so-called Black Equation [119]. Here, A_m is a constant which comprises the material properties and the geometry of the interconnect, E_a is the activation energy of the dominant diffusion path, and n is the current density exponent, which is determined experimentally. If the failure is dominated by the nucleation process n equals 2, while if the failure time is dominated by the void growth mechanism n equals 1 [107]. For Cu lines with a TaN diffusion barrier, the failure is normally dominated by the void growth [104, 105]. In a more general case, the failure process involves both, nucleation and growth of a void, thus the extraction of the parameter n is not straightforward.

Blech et al. [114, 120, 121] derived a criterion to indicate whether a line is fallible due to EM based on the current density and length of the line,

$$(jL)_c = \frac{\Omega\left(\sigma_{th} - \sigma_0\right)}{|Z^*|\, e\rho}, \tag{2.5}$$

where σ_{th} is the maximum mechanical stress the line can withstand, σ_0 is the initial stress, Ω is the atomic volume. Eq. (2.5) is known as Blech product.

The Blech product is a measure of the current density and the length of the metal line below which the EM damage stops. In the experiments, Blech tested a structure consisted of gold (Au) lines deposited onto a titanium nitride (TiN) film and stressed at a high current density [114]. The applied current elongated the metal line in the direction of the electron flow. While in the long lines EM were observed, in short lines the EM stopped. In the short lines, the generated mechanical stress gradient led to a back-flux which compensated the EM flux, as previously mentioned. This experiment was reproduced in lines with different materials and current density to obtain the Blech length, the length below which the EM-induced failure does not occur. The results indicated that Blech effect has a strong dependence on the fabrication process and on the geometry of the lines. Consequently, the Blech length changes for different IC technologies [122].

Besides the current density, the time-to-failure (TTF) of an interconnect due to EM depends on the temperature, as shown in (2.4). Generally, the designer considers the maximum current density to design the lines of the circuit and does not take into

account the temperature which has a significant impact on the EM. The maximum current density informed in the datasheet of the technology is not associated with temperature. However, the temperature accelerates the EM damage, thus the current density supported by the lines is lower at higher temperatures. Therefore, the temperature is an important parameter to be considered for the EM evaluation.

2.3 Impact of the Temperature

The EM is very sensitive to the temperature, as described in (2.2). Temperature changes affect the diffusion coefficient and the resistivity of lines. The diffusion coefficient follows an Arrhenius relation with an exponential variation with T given by [123]

$$D(T) = D_0 \exp\left(-\frac{E_a}{kT}\right). \tag{2.6}$$

Here, D_0 is a pre-exponential factor and E_a is the activation energy, both dependent on the diffusion mechanisms. The line's resistivity, ρ, calculated by [124]

$$\rho = \rho_0 \left[1 + \alpha \left(T - T_0\right)\right], \tag{2.7}$$

is a function of the resistivity ρ_0 in the reference temperature T_0 and the temperature coefficient α of the metal.

Figure 2.4 shows the D change in Al, Cu, Co and Ru for the temperature variation from 300 to 400 K, based on the parameters from Table 2.2. The Co and Ru has a lower D than the Cu and Al, justified by the differences in the activation energy. As Co and Ru have higher activation energies, a higher temperature is necessary for the EM to become significant. The higher activation energy is an important advantage of the Ru and Co in comparison with Al and Cu.

Table 2.2 – Parameters for Cu, Al, Co and Ru.

Material	Cu	Al	Co	Ru	Unit	Ref.
α	4.3	4.5	6.6	4.1	10^{-3}/K	[125, 126]
ρ_0	1.8	2.7	6.5	13	$\mu\Omega$–cm	[6, 88]
D_0	31x10^{-2}	66x10^{-3}	37x10^{-2}	57x10^{-2}	cm^2/s	[127–129]
E$_a$	0.7-2.1	0.6-1.4	2.4-3.1	1.9-2.9	eV	[6, 130]

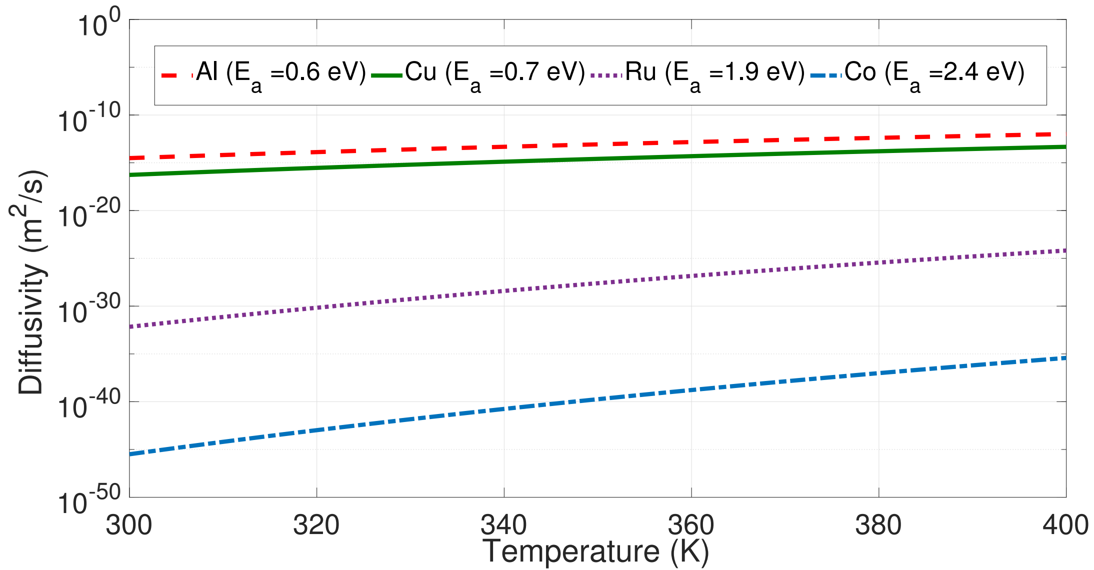

Figure 2.4 – Diffusivity variation with the temperature for 4 different metals.

2.3.1 Self-Heating from Transistors

In an IC, the temperature changes with the power dissipation of the transistors. The transistors switching produces heat, which results in heat flow through the chip. Figure 2.5 depicts the heat flow from transistors on the FEOL to the interconnects on the BEOL. As a consequence, the interconnects experience a pronounced temperature increase, mainly in the regions near the heat sources.

The transistor self-heating (SH) in the FEOL results in a non-uniform temperature distribution in the metallic layers of the BEOL [133, 134]. The temperature change

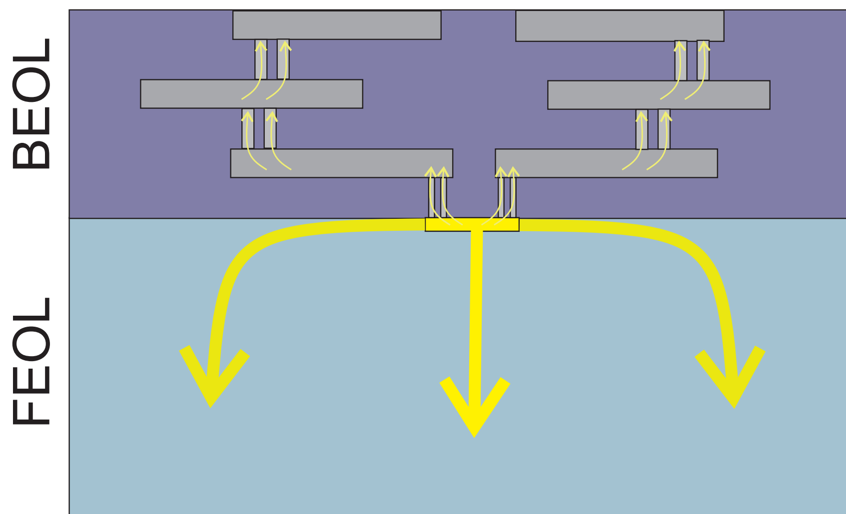

Figure 2.5 – Heat flow through the BEOL and the FEOL due to power dissipation of the transistors' operation [131, 132].

in each metallic layer is given by [133]

$$\Delta T_{PT} = \frac{P_T}{2\pi k_{eff}^{beol}} \ln\left(\frac{z}{2h_0 - z}\right), \tag{2.8}$$

where P_T is the power dissipated by transistors, z is the distance in the BEOL from heat source, h_0 is the BEOL total thickness and k_{eff}^{beol} is the effective thermal conductivity of the BEOL given by [133]

$$k_{eff}^{beol} = \left[\sum_{n=1}^{m}\left(\frac{L_n^{via}}{k_{eff_n}^{via}} + \frac{L_n^{int}}{k_{eff_n}^{int}}\right)\right]^{-1} \cdot h_0, \tag{2.9}$$

where m is the total number of interconnect layers, L_n^{via} and L_n^{int} are the height of the vias and interconnects, respectively, for a particular layer n, k_{eff}^{via} and k_{eff}^{int} are the thermal conductivities of the via and the metallic layers, respectively.

The thermal conductivities of the via and interconnects layers depend on the volume fraction of vias (V_{via}) and lines (V_{int}), respectively, relative to the complete volume of a specific layer. The k_{eff}^{via} varies with the thermal conductivity of the metal (k_m) and insulating (k_i) materials according to [133]

$$k_{eff}^{via} = k_m V_{via} + k_i(1 - V_{via}). \tag{2.10}$$

Considering a typical copper dual-damascene technology, $k_m = 401$ W/(m.K) [135] and $k_i = 1.4$ W/(m.K) [136]. The thermal conductivity of the interconnects is given by [133]

$$k_{eff}^{int} = \beta k_i \frac{1 + \eta V_{int}}{1 - V_{int}} \tag{2.11}$$

where η and β are related to k_m, k_i, the length and the thickness of the lines [133]. The dimensionless parameters η and β can be approximated to 1, however, for interconnect lines with dimensions above 10 μm [137]. The model above allows estimating the temperature increase in interconnects as a function of the power dissipated by the circuit.

2.3.2 Joule Heating in the Interconnects

Joule heating (JH) refers to the temperature change of the interconnect line when a current passes through the conductor. For an elevated current density, JH produces enough energy to make the lines heat up significantly. Accordingly, JH is evidenced for

modern technologies because the lines are more resistive and operate with higher current densities [138].

The temperature increase due to the JH for 90 nm technologies is below 3K, modest in comparison with the temperature change due to the SH from the transistors. For 22 nm and 45 nm technologies, the temperature increase due to JH in the local interconnects is 5 K and 20 K, respectively [139]. The reduced contribution of the JH to the temperature change is more noticeable in the metal lines of the layers near the transistors [140, 141]. Nevertheless, the interconnect heating results in a temperature gradient and a corresponding TM flux.

Figure 2.6 illustrates the heat flow in the IC. The primary heat flows through metal and substrate and the secondary heat flows through the inter-metal dielectric. Heat generation occurs mainly by transistors, but also the effect of JH on interconnects. The effects act simultaneously, and as a result, there is heat flow and temperature distribution that depends on both.

2.4 Impact of Electromigration on Wire Resistance

In addition to the current density and the temperature, the structure also affects the line reliability. In old technologies, Al lines had high values of resistivity and large dimensions, and the EM was not a bottleneck. The high resistivity of the Al lines resulted

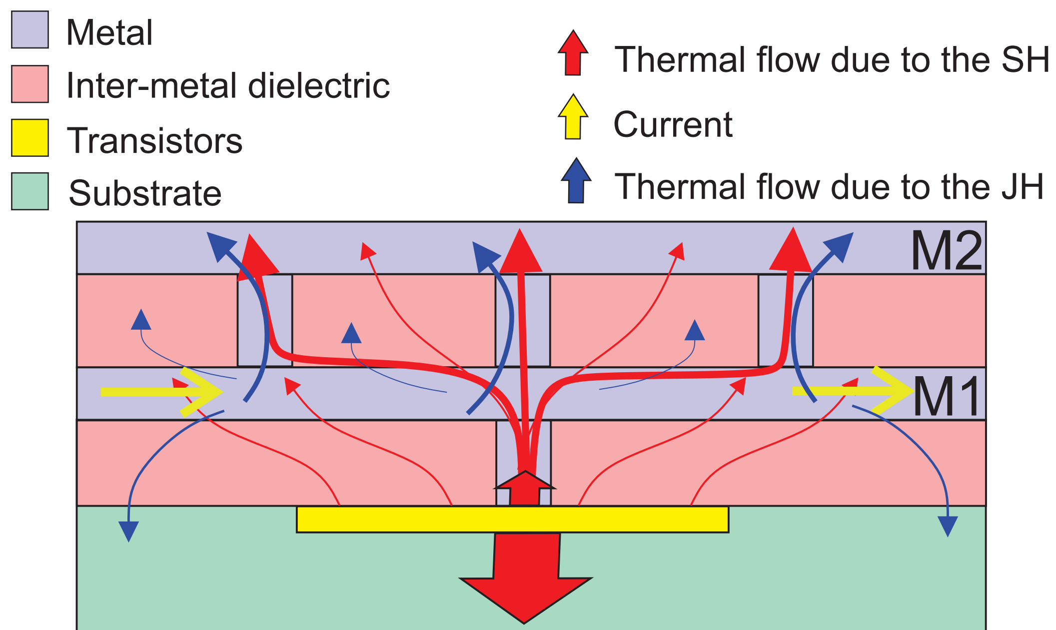

Figure 2.6 – A schematic diagram of the combined effect of transistor self-heating (SH) and Joule heating (JH) heats up metal line, with the heat flowing mainly through the metal and the substrate.

in a high resistance and the Joule heating became more relevant with line shrinking at each new technology node. With a continuous increase in the number of transistors and interconnects in advanced ICs, interconnects made of Al became prohibitive [22, 142].

In 1993, Cu replaced Al in the interconnect lines. The higher conductivity of Cu lowered the RC delay and the Joule heating resulting in a faster chip with reduced power dissipation. Also, due to the lower resistivity of Cu, there was margin to maintain the continuous reduction of the interconnects' dimensions. Based on these advantages, the semiconductor industry adopted Cu conductors in modern technologies.

On the other hand, the continuous shrinking resulted in an elevated current density, increasing the impact of the EM in ICs. With the lines reaching dimensions of hundred of nanometers, the Cu material is considered a bottleneck, mainly in the interconnects with elevated current density. The elevated current density is a reason to replace the Cu, to increase line reliability. Intel has tested Co in lines of the metal 1 and metal 2 for a 10 nm technology. Even though Co is 3.5 times more resistive than Cu [6, 88], Co lines are more resistant to EM. The adoption of Co lines allows to meet the ITRS estimations for the next IC generations [12, 25, 40, 60, 143].

2.4.1 Interconnect Structure

Figure 2.7 shows a typical Cu interconnect line used in new technology nodes. The Cu line has a width, thickness, and length represented by w, h, L, respectively. The terms w_b and t_b indicate the diffusion barrier thicknesses. The Cu area is the product $w \cdot h$. The barrier area is given by

$$A_b = 2w_b \cdot h + t_b \cdot w + 2w_b \cdot t_b. \tag{2.12}$$

The barrier of TaN has a larger resistivity than Cu. Its typical thickness varies between 8–15 nm for the 180 nm technology [144], which results in a maximum cross-sectional area of 7980 nm^2 considering metal 1 dimensions of minimum width and height as specified in XFAB 180 nm technology [145, 146]. Table 2.3 shows the evolution of the parameters of the line from different technologies, based on the ITRS estimation. The minimum metal area estimated for metal 1 interconnects is 288 nm^2 for technologies developed in 2020, 9 times lower than the metal area in 2011's technologies.

The barrier layer protects the diffusion of Cu into the surrounding dielectric. The diffusion barrier is placed on the sides and at the bottom of the Cu line, while a dielectric capping film is on the top. Typically, TaN, Ta or a TaN/Ta bilayer are excellent diffusion barriers, where TaN provides a good adhesion to the surrounding dielectric, and

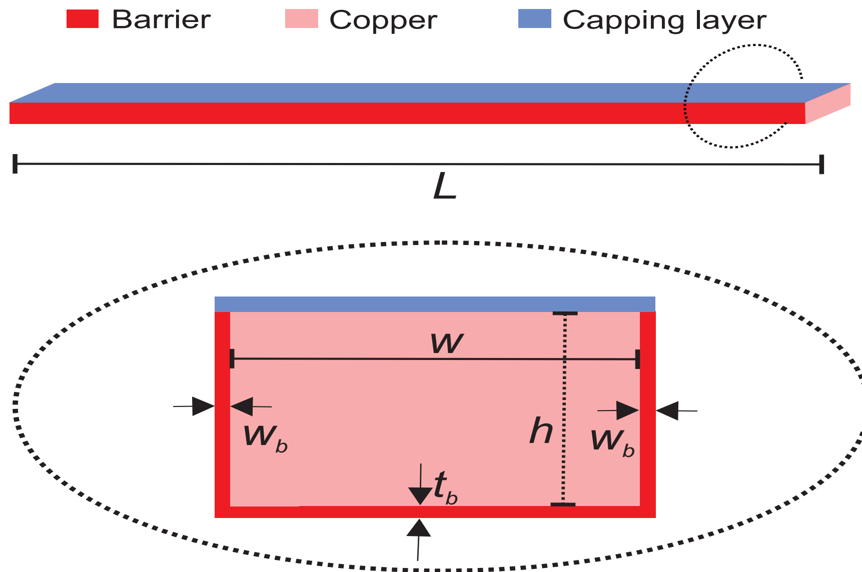

Figure 2.7 – Typical Cu interconnect structure.

Table 2.3 – Parameters of the interconnects based on the ITRS reports. [25, 144]

Year of Production	2011	2013	2015	2017	2019	2020
Barrier thickness (nm)	2.9	2.4	1.9	1.5	1.2	1.1
Metal 1 width (nm)	38	27	21	17	13	12
Metal 1 thickness (nm)	68	51	40	34	26	24
Metal 1 area (nm^2)	2584	1377	840	578	388	288

Ta provides a surface with good wettability of the Cu seed layer [147, 148]. Silicon nitride (SiN), silicon carbide (SiC), silicon carbonitride (SiCN), silicon oxynitride (SiON), and silicon dioxide (SiO2) considered along the thesis, are typical dielectric materials used as capping layers [149–154].

The barriers have an essential function, besides to avoid the Cu material diffusion into the Si active region. The barrier functions as a redundant shunt layer and prevents an open circuit due to a void growth [155]. This shunt layer can conduct electrons even if a void exists in the metal conductor. It can withstand high current densities for long times. The industry has investigated alternatives to manage the *RC* delay, and one alternative is to reduce the thickness of the diffusion barrier. However, a minimum thickness above 1 nm is needed to achieve the line reliability of the modern technologies [156].

2.4.2 Interconnect Resistance Variation

Under EM, the interconnect resistance increase degrades the performance of circuits. This resistance variation is initially minimal, as the growing void has not reached the wire barrier, as shown in Figure 2.8 (a). When the void reaches the barrier, the current begins to flow through part of the barrier, which is a much more resistive material, shown in Figure 2.8 (b). In this case, the resistance variation (ΔR) is linear and calculated by [146]

$$\Delta R = \frac{\rho_b D \left| Z^* \right| e \rho j \Delta t}{A_b k T}, \tag{2.13}$$

where ρ_b is the resistivity of the barrier, A_b is the barrier area and Δt is the time variation. As explained in Section 2.3, ρ, ρ_b and D are temperature dependent.

The ratio between the resistance variation (ΔR) and the initial resistance (R_0) for the line under EM is commonly used to determine the interconnect failure and is given by [146]

$$\frac{\Delta R}{R_0} = \frac{\rho_b D \left| Z^* \right| e I \Delta t}{A_b k T L}, \tag{2.14}$$

where I is the electrical current and L is the length of the line.

Figure 2.9 shows a typical $\Delta R/R_0$ variation in a Cu line. The phase 1, initiated by the nucleation and an initial growth, has a small resistance increase. Some studies report a resistance increase of 1% to 5% [146, 157]. When the void reaches the barrier, the resistance exhibits a significant increase. As mentioned, at this moment, the line becomes more resistive as the current passes through the TaN. Then, phase 2 initiates and the resistance varies linearly with the time, given by (2.13).

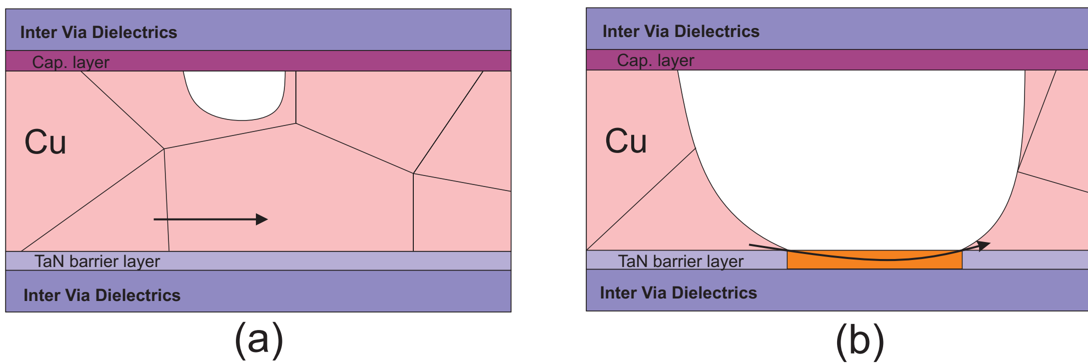

Figure 2.8 – Cross section of an interconnect. In (a), the growing void has not reached the wire barrier and the current passes throught the Cu. In (b), the void reaches the barrier and the current begins to flow through part of the barrier.

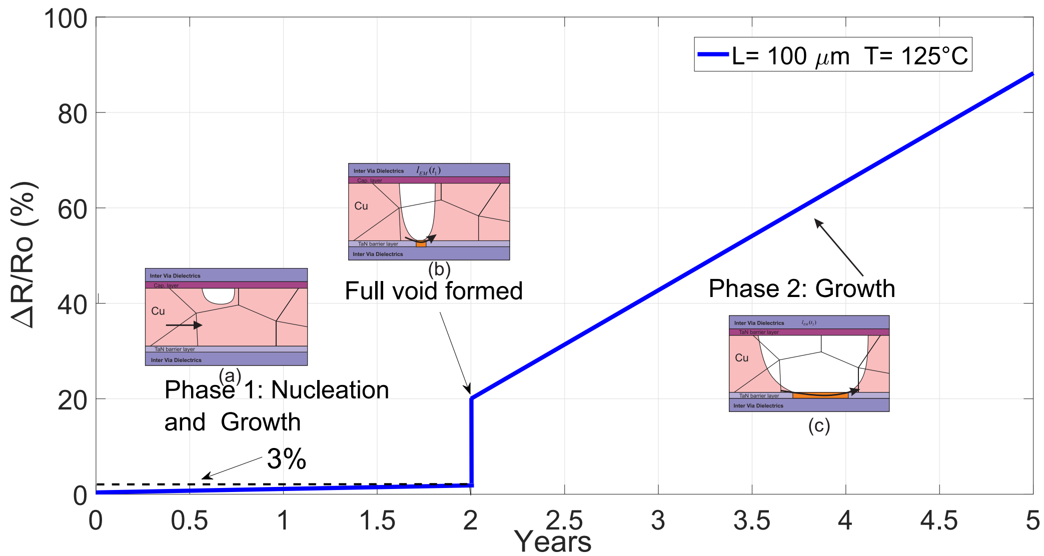

Figure 2.9 – Resistance change of an interconnect during the phases of nucleation and growth [146, 158].

The $\Delta R/R_0$ and the period of phase 1 shown in Figure 2.9 is an estimation based on recent EM studies with isolated interconnects [36, 146]. Experiments indicate that the failure occurs mainly in phase 2 for damascene Cu interconnects with a diffusion barrier [104, 105, 159, 160]. A detailed derivation of (2.13) and (2.14) is provided in Appendix A.

Figure 2.10 shows the evolution of the $\Delta R/R_0$ ratio given by (2.14) as a function of time considering the values from Table 6.1 for two interconnects with different lengths (L = 125 μm and L = 100 μm) and two temperatures (T = 353 K (80 °C) and

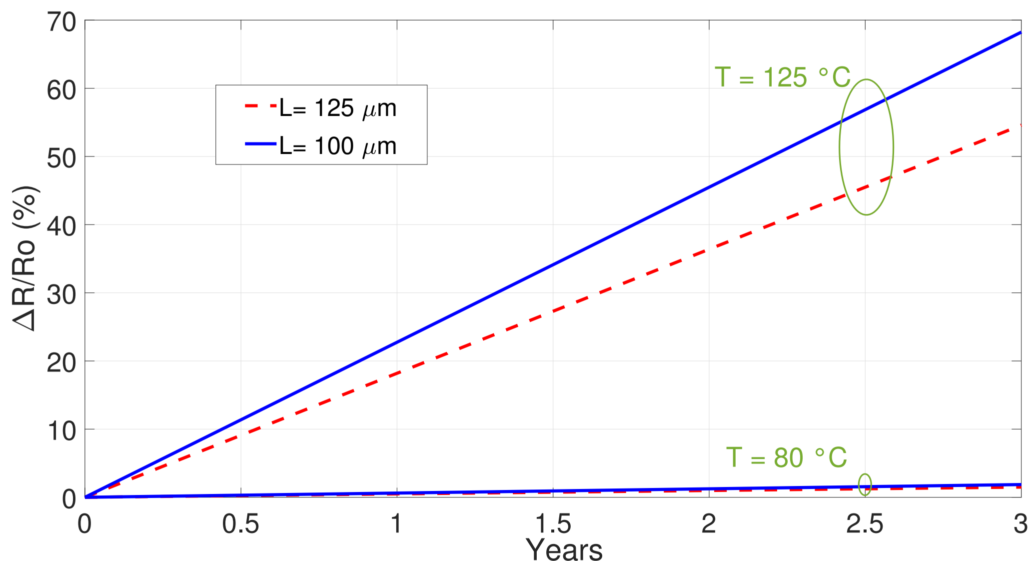

Figure 2.10 – Resistance ratio variation as a function of time according to (2.14) for XFAB 180 nm technology [1].

Table 2.4 – Parameters based on the XFAB 180 nm technology used to calculate the $\Delta R/R_0$ ratio from (2.14) [1].

Symbol	Name	Value	Unit	Ref
ρ_b	Ta resistivity	3x10^{-6}	Ω.m	[146]
α_b	Ta thermal coeffcient	6.5x10^{-6}	1/K	[161]
D	Cu effective diffusivity	^{1}1.6x10^{-19}, ^{2}6.7 x10^{-18}	m^2/s	[128]
Z^*	Effective valence	1	-	[162]
e	Electron charge	1.6x10^{-19}	C	[163]
ρ	Cu resistivity	24x10^{-9}	Ω.m	[162]
α	Cu thermal coeffcient	17x10^{-6}	1/K	[164]
I	Current	2.3x10^{-4}	A	-
A_b	Ta barrier area	7.98x10^{-15}	m^2	[145]
k	Boltzmann constant	1.38x10^{-23}	J/K	[163]
T	Temperature	318, 353	K	-
w	Line width	0.6	μm	[145]
h	Line heigth	0.17	μm	[145]
E_a	Cu line activation energy	1.0	eV	[165]

^{1}318 K, ^{2}353 K.

398 K (125 °C)). The values are based on XFAB 180 nm technology [145]. As expected, the higher is the temperature, the larger is the resistance variation, which leads to shorter failure times. It is interesting to note that, although longer lines are supposed to be more critical considering the Blech Effect [114, 120, 121], the smaller ones may be the bottleneck, being more sensitive to small resistance variations.

2.5 Interconnect Lifetime

The lifetime of a line depends on its geometry and crystal structure. Figure 2.11 shows different crystal structures in metallic interconnects. The polycrystalline lines in (a) present a reduced lifetime due to the grain boundaries, which results in more

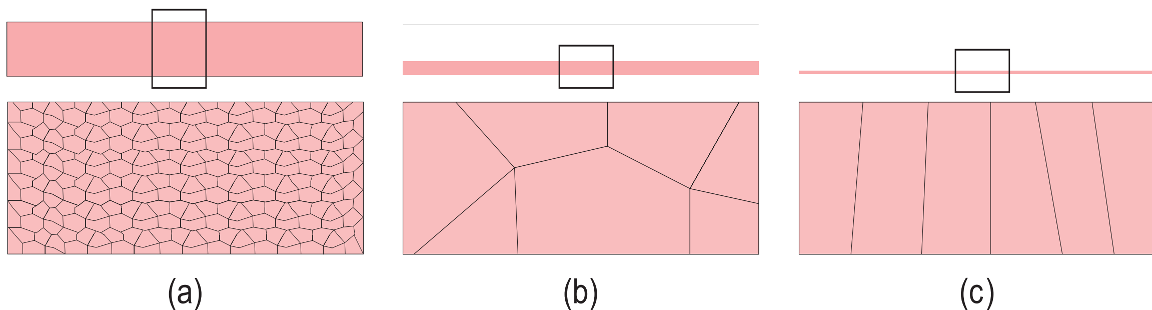

Figure 2.11 – Different crystal lattice structures in metallic interconnects (a) polycrystalline, (b) near-bamboo and (c) bamboo.

diffusion paths favorable to EM evolution. The near-bamboo lines in (b) have a smaller dimension, with a reduced number of grain boundaries, an important feature to increase the line reliability. In the bamboo line in (c), the grain occupies the width of the lines, resulting in no continuous grain boundary path in the direction of the current flow. In bamboo and near-bamboo lines, interfacial diffusion is the main mechanism for EM [166–168]. In this context, under the same current density, the bamboo and near-bamboo are significantly more reliable than polycrystalline lines. In recent technologies, the metal lines are becoming more polycrystalline, as the bamboo microstructure has been challenging to achieve in interconnect structures having widths less than 100 nm [169].

A resistance increase of 10% is generally used as a failure criterion, since this variation in global wiring can produce timing errors [170]. Using this percentage increase as a failure criterion has some limitations. First, the actual damage that causes the failure is a function of the initial resistance of the line, which is affected by the temperature and the stress during the fabrication. Second, the resistance ratio can assume values higher than 10%, and the circuit continues operating correctly or, on the other hand, it can be lower than 10% and the circuit loses the minimum performance. Therefore, a better failure criterion considers the resistance change for each line, that is, the maximum resistance change that a particular line can withstand before problems in the circuit performance occurs. A disadvantage is that there is no global criterism valid for all the lines.

2.5.1 Time-to-Failure of Interconnects

The line resistance increases faster when it operates with elevated current density and temperature. These two parameters are extrapolated to accelerate the line degradation process during the interconnect lifetime evaluation tests. Traditionally, a $\Delta R/R_0$ of 10% indicates the interconnect failure. However, this resistance variation does not necessarily degrade the performance of the circuit in a catastrophic way. Figure 2.12 shows the time for a wire resistance to increase 10% as a function of temperature for three typical values of activation energies, namely, 0.8 eV, 0.9 eV and 1.0 eV operating with a current of 110 μA calculated by 2.14. The line has a width of 60 nm, a length of 125 μm and a thickness of 170 nm [171]. Note that a higher activation energy of 1.0 eV requires a higher temperature of 473 K to a resistance change of 10% in 1 year.

The time to an interconnect failure according to the Black Equation is expressed by (2.4). Traditionally, (2.15) evaluates the line lifetime, considering the results obtained from accelerated tests ($MTTF_{acel}$) with elevated current density (j_{acel}) and temperature (T_{acel}) values. Then, assuming n=1 and that the parameters E_a and A do not change, the time-to-failure at use conditions ($MTTF_{use}$) is given by [172]

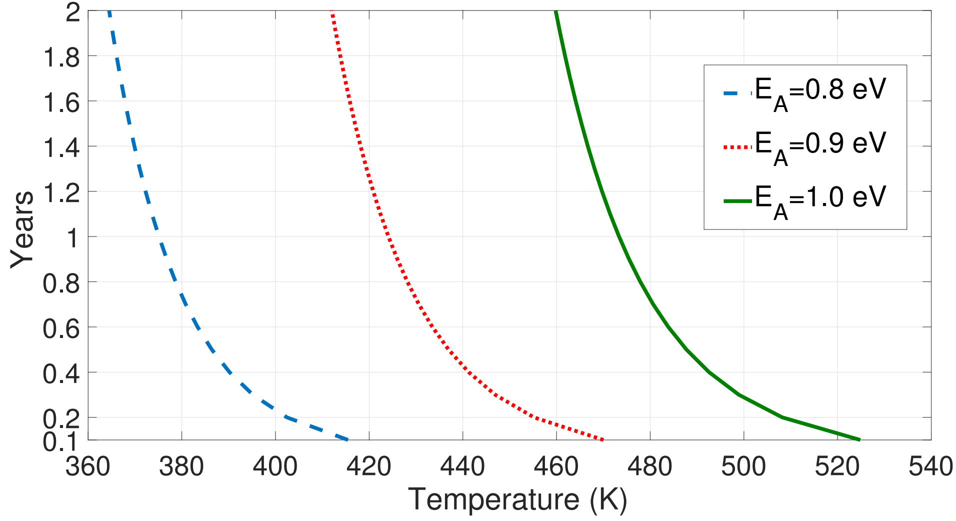

Figure 2.12 – Time for a wire resistance variation of 10% as a function of the temperature for three activation energies operating with a current of 110 μA, and a width of 60 nm, thickness of 170 nm and length of 125 μm.

$$\left[\frac{MTTF_{use}}{MTTF_{acel}}\right]_1 = \left(\frac{j_{acel}}{j_{use}}\right) \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{acel}}\right)\right]. \tag{2.15}$$

The time for the line to reach a critical resistance variation, $(\Delta R/R_0)_{crit}$, can be obtained using (2.14). The $(\Delta R/R_0)_{crit}$ is the resistance ratio value that results in a circuit performance change out of an acceptable range. Then, the time to reach this critical value can be considered the time to circuit failure and expressed by [173]

$$MTTF = \frac{kLA_bT}{De\,|Z^*|\,\rho_b(T)I}\left(\frac{\Delta R}{R_0}\right)_{crit}. \tag{2.16}$$

Similar to (2.15), another relation between the time-to-failure (TTF) in use and accelerated conditions are obtained by [173]

$$\left[\frac{MTTF_{use}}{MTTF_{acel}}\right]_2 = \frac{T_{use}D_{acel}\rho_{b acel}j_{acel}}{T_{acel}D_{use}\rho_{b use}j_{use}}, \tag{2.17}$$

where T, D, j and, ρ_b are the temperature, the diffusivity, the current density and the resistivity in use and accelerated conditions.

Equations (2.15) and (2.17) are two expressions to calculate the TTF, the first is a direct application of Black's equation and the second has been derived based on the resistance growth model. These equations are related through

$$\left[\frac{MTTF_{use}}{MTTF_{acel}}\right]_2 = \beta\left[\frac{MTTF_{use}}{MTTF_{acel}}\right]_1 \tag{2.18}$$

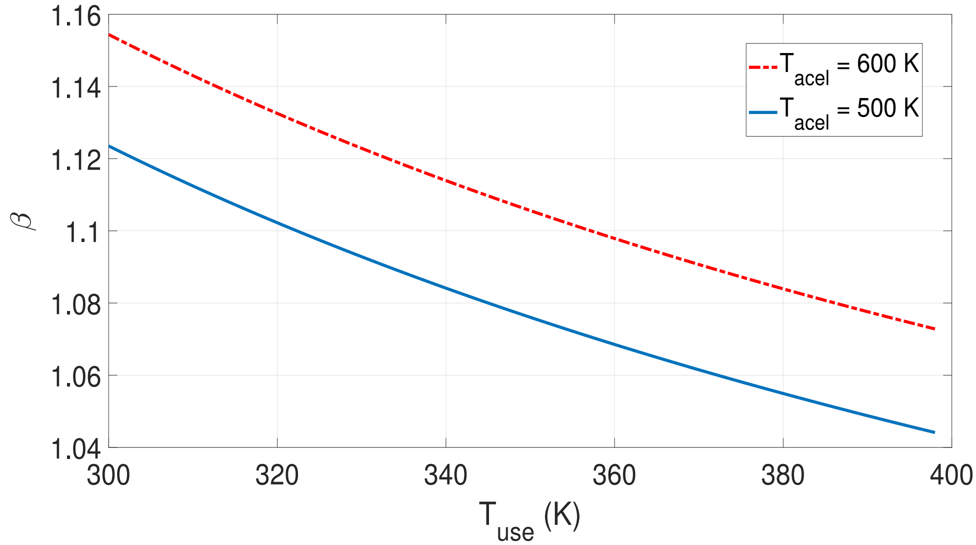

Figure 2.13 – β change with T_{use} variation from 300 K to 398 K, for T_{acel} of 500 K and 600 K, and $T_0 = 293$ K.

where β is a coefficient given by

$$\beta = \frac{T_{use}}{T_{acel}} \left[\frac{1 + \alpha_b \Delta T_{acel}}{1 + \alpha_b \Delta T_{use}} \right] \tag{2.19}$$

where α_b is the linear temperature coefficient for the barrier resistivity, ΔT_{acel} and ΔT_{use} are given by

$$\Delta T_{use} = T_{use} - T_0, \tag{2.20}$$

$$\Delta T_{acel} = T_{acel} - T_0, \tag{2.21}$$

where T_0 is a reference temperature.

Equations (2.18) and (2.19) imply that the use of Black's equation can lead to an inaccurate extrapolation. Figure 2.13 shows the β change with T_{use} variation from 300 K to 398 K, for T_{acel} of 500 K and 600 K, α_b of 0.0045/K and $T_0 = 293$ K. A larger difference between T_{use} and T_{acel} results in a higher β coefficient, which means a larger deviation between (2.15) and (2.17). Also, the β coefficient increases with the T_{acel}. Therefore, the higher is the temperature used in the accelerated tests, less accurate is the MTTF of the lines with the Black's Equation and may result in an unrealistic analysis.

2.5.2 Electromigration Statistical Distribution

The lognormal and Weibull distributions are used to fit the data from accelerated EM tests [174]. Generally, the TTF of the interconnect is extrapolated from the accelerated to the use conditions, and then the circuit lifetime is estimated by a modified form of the Black Equation [175–177]. Even though Weibull may appear to fit the lifetime data with a good accurracy, the lognormal distribution is more appropriate to obtain predictive extrapolated lifetimes [178]. Ref. [179] shows that the lognormal distribution of the grain sizes is a primary cause for the lognormal distribution of EM lifetimes.

The ideal EM analysis should evaluate all the current densities and temperatures in each interconnect path of an IC. As the complex interconnects have multibranch paths, each path can have a different current density and temperature. Besides the estimation of the EM in all the lines, a better MTTF prediction should consider different scenarios, including worst-case conditions due to variations in manufacturing process, operating temperature and supply voltage [180].

The reliability analysis in an IC is more complicated than in a typical EM test structure, composed of samples of similar interconnects. The IC reliability analysis involves, besides the interconnect, the aging effects in the transistors. Also, the stress formed in the fabrication process reduces the lifetime of the IC.

2.6 Parasitic Extraction of the Interconnects

In early integrated circuits, the wiring had a negligible impact on the IC performance. However, below the 0.5 μm technology node, the resistance and the capacitance of the interconnects started making a significant impact on the IC performance [181]. With the improvement in performance, density, and complex designs, the parasitic effects have become more challenging in modern IC design, especially for 65 nm and below [182]. Also, for high-speed chip designs, longer wire lengths plus the use of low-k dielectrics require inductive effects to be also considered [183].

Parasitic extractors are integrated into EDA tools to extract the parasitic resistances, capacitances, and inductances of devices and wires of an integrated circuit. Parasitic extraction results help designers to analyze the impact of the physical implementation on the performance of the circuit by evaluating the layout of the design.

The correlation between the measured chip performance and post-layout simulation is a function of the accuracy of the parasitic resistances, capacitances and inductances calculated for devices and wires. As the parasitic extraction gives a more realistic model of the circuit together with the effects of the parasitics added to the simulation, it

is possible to verify if the additional parasitics still allow the designed circuit to properly function. The interconnect parasitics affect the timing of the signal propagation, the coupled noise from adjacent elements, IR drop on longer lines and the change in biasing and performance of transistors on the finished chip [184].

To calculate the parasitic resistance and capacitance of the interconnects, extraction tools use: the layout of the design in the form of polygons on a set of layers; a mapping to a set of devices and pins obtained from a Layout Versus Schematic (LVS) simulation; and parameters of the layers including metal resistivity [185, 186]. The extraction tool uses this information to create a layout which has added resistances between various sub-parts of the wires, vias, contacts, pins and all other resistances obtained from the extracted result. In turn, the parasitic capacitance of an interconnect is divided and shared among the sub-nodes proportionally. As the number of parasitic elements increase with the number of devices and interconnects, the extraction tool consumes more memory and time which increases the complexity of the post-layout design simulation.

Figure 2.14 illustrates the parasitic resistances of the interconnects for three layout structures. Figure 2.14(a) shows the wire with two terminals and one parasitic resistance. For longer lines, generally, a row of resistances in series represents the wire. Figure 2.14(b) shows a wire with three terminals named C, D and E and three parasitic resistances for metal paths. A more complex wire in the Figure 2.14(c) illustrates that the resistance extraction becomes more challenging as the number of terminals increase. Here, the wire has five terminals and seven parasitic resistances. As the interconnects

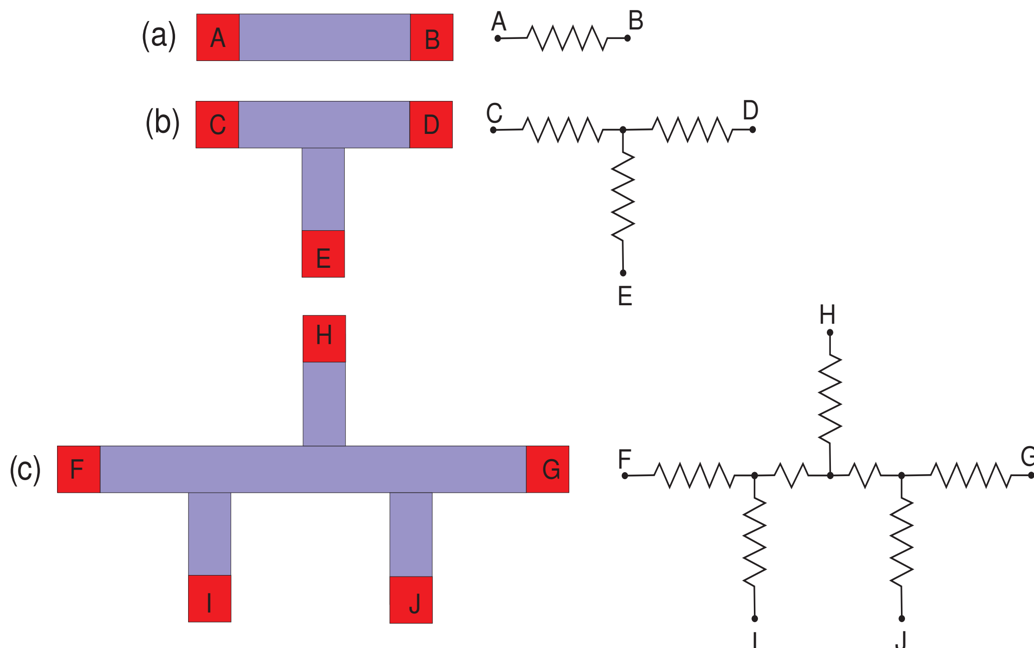

Figure 2.14 – Different interconnect structures and possible equivalent representation with resistances.

in integrated circuits have multiple terminals, the EM parameters generally obtained in accelerated tests with hundreds of structures similar to Figure 2.14(a), are extrapolated to the more complex wires, like the wires in Figure 2.14(b) and Figure 2.14(c). This extrapolation decreases the complexity, but also the accuracy of the EM analysis.

The netlist from a layout is a description of the electronic elements and connected nodes within that circuit layout, including all the extracted parasitic resistances and capacitances across every interconnect. While the netlist of a circuit schematic has only the electronic devices models connected with ideal wires, the netlist from the layout contains the parasitics that affect the circuit performance. SPICE, H-SPICE, and other compact modeling platforms use the netlist from layout for circuit-level simulation, giving to the IC designer a realistic understanding of the circuit environment, along with the performance implications of parasitics. As the identification of the specific layers that define the transistors and the metal wiring is critical for accurately calculating the parasitic values, the development of new methods to more accurately obtain the parasitics becomes more relevant for ultra-high-speed circuits [187–189].

3 Methodology to Evaluate the Impact of Electromigration on Chips during Design

In this chapter the methodology to evaluate the EM impact on an IC at the design level is explained. First, we describe the procedures to calculate the resistance change of the lines due to EM. Then, the effect of the EM on the performance parameters of an IC is discussed, followed by the description of methods to identify the critical interconnect lines as well as to estimate their widths based on the EM criteria. Finally, the full methodology flow to evaluate the EM impact on an IC and size the interconnect is presented.

3.1 Traditional EM Methodology

In commercial tools, the EM analysis consists in comparing the current density on each wire to the foundry EM rules and then link to an IC implementation toolset for automated or manually assisted fixing. The foundries define the EM rules based on a maximum current density limit and on the Blech product to control EM for each wire. The maximum current density calculation includes the wire width, layer, activity, frequency, and temperature [190, 191]. In turn, the Blech product calculation includes the length of the lines. Thus, the width and the length of the wires become part of the design rule set.

Figure 3.1 shows an interconnect to exemplify the EM evaluation in the commercial tools. The interconnect has Metal 1, Metal 2, and Metal 3 paths with a current flowing through them. Metal 1 and Metal 2 have the width $w1$ of 200 nm and $w2$ of 260 nm, and a current of 0.5 mA. Metal 3 have currents of 0.3 mA and 0.2 mA and the width

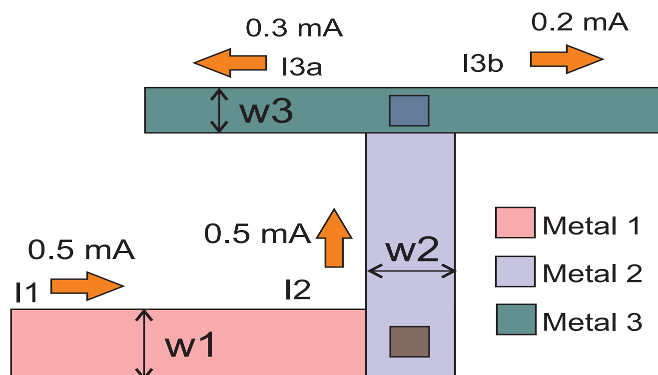

Figure 3.1 – Layout top view of an interconnect line with paths made of Metal 1, Metal 2, and Metal 3 and the corresponding currents flowing through them.

Table 3.1 – Parameters from the interconnect of Figure 3.1.

Path	w (nm)	I (mA)	J (mA/μm)	Condition
Metal1	200	0.5	2.5	Critical
Metal2	260	0.5	1.92	Non-critical
Metal3a	140	0.3	2.14	Critical
Metal3b	140	0.2	1.42	Non-critical

$w3$ of 140 nm. First, the EM tool calculates the current density and then evaluates if the paths is critical based on the EM rules. Here, the line is classified as critical if the paths have current density above 2 mA/μm, a typical value for 45nm technologies [171]. Table 3.1 shows that Metal 1 and Metal 3a are critical, while Metal 2 and Metal 3b are non-critical.

IC designers use some strategies to minimize the EM problem [192, 193]. The most used strategy is to enlarge the wire to reduce the current density. As the foundry fixes the thicknesses of the lines, the designer can only change the width and the length. Thus, the current density is represented in mA/μm instead of the formal definition of MA/cm^2. Other strategies to improve the EM reliability is to reduce the supply voltage, the frequency and the wire length.

Unfortunately, these strategies have area and performance trade-offs. Fixing a critical line due to EM is not a simple task of just following the rules. As an increase in the width changes the spacing, the rules related to the minimum distance to neighboring wires have to be guaranteed. Enlarging the wires not only increases the area, but also can cause timing violations and affects the circuit performance. In this context, the designer needs an effective EM analysis which helps to minimize the EM risk without sacrificing too much area and performance.

The evaluation of the circuit performance degradation due to the EM allows the designer to identify with more accuracy if the performance is satisfactory, even if the lines operate with an elevated current density or to verify if a single line is critical even when operating with a current density below the maximum threshold. To evaluate the EM, the resistance change of the lines has to be calculated considering mainly the temperature and the current density. With the EM evolution, the circuit performance changes. Nevertheless, as the EM evolution is an extended time process, the circuit can operate under an elevated current density and still maintain an adequate performance.

As the analog IC design works semi-automatically, an analog designer draws the lines manually using a router, a design ruler checker (DRC) and a Layout-Versus-Schematic (LVS) tools. With the DRC tool, the designer evaluates if the lines are according

to the rules informed by the foundry. The LVS tool compares the layout and schematic, informing to the designer the wrong and the incomplete connections needed to finish the layout. Using a router, the designer chooses the metal layer to realize the connections lines' width, and the number of vias and contacts.

In turn, the digital designer uses fully automated tools in the chip design. However, the designer needs to understand the problem, use larger wires, run an EM analysis, and fix the violations. Along with power, timing, and leakage, EM is a relevant factor to be considered, mainly in modern technologies. Thus, the digital designer also need to understand how EM affects chip performance.

3.2 Estimation of an Interconnect Resistance Change due to EM

Figure 3.2(a) shows the methodology flow to calculate the resistance change of interconnects due to the EM. The methodology requires the schematic and layout files of the integrated circuit under design. Here, we use the SPICE simulator, the parasitics extractor, and other EDA tools. Figure 3.2(b) shows the main procedures to calculate the EM resistance change.

The schematic represents the circuit with the models of electrical components, such as transistors, capacitors, and inductors. The designer chooses the models for commercial, industrial, or military applications, which have different process costs, as well as contain particularities, such as the threshold voltage of the transistors. The standard

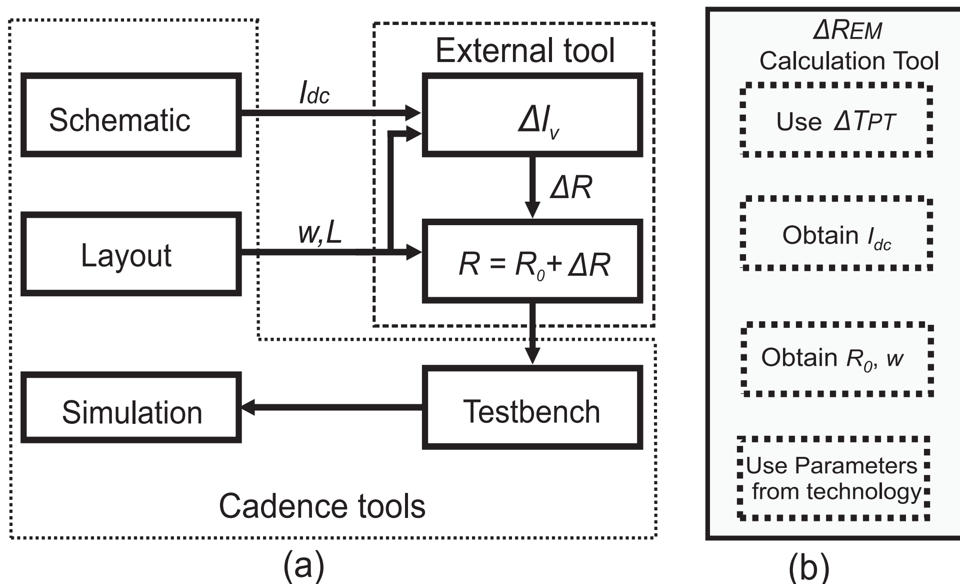

Figure 3.2 – (a) Proposed methodology flow to calculate the resistance change of interconnects due to EM. (b) Main procedures to calculate the EM resistance change.

temperature ranges from 0° to 85°, -40° to 100°, and -55° to 125° for commercial, military, and industrial applications [194, 195]. In addition to the temperature range, the designer has to observe the power consumption of the transistors. Generally, the power transistors demand higher currents, which make the corresponding lines potentially more susceptible to EM failures.

The designer uses a SPICE simulator to obtain the average or DC, root-mean-square (RMS), and peak currents for each wire segment by a DC or transient analysis. The peak current is the maximum current at any instant in time during the signal transition, which is always greater than the RMS current, or the average current. Thus, the use of the peak current generally overestimates the EM degradation as the lines do not operate full time.

Unidirectional and bidirectional currents have different influence on EM. As the unidirectional current flows in the same direction through a metal segment during both the rising and falling transition of the signal, the DC value is nonzero. On the other hand, as the bidirectional current flows in one direction during the rising transition and the other direction during the falling transition, DC is close to zero, and the lifetime becomes larger than the lines under unidirectional current. However, under a sufficient current density, the Joule heating potencialize the EM, degrading the benefical self-healing from bidirectional lines. Generally, the EM analysis requires the use of the three currents when the circuit contains unidirectional and bidirectional currents. The proposed methodology consider the DC value to calculate the resistance change, as shown in Figure 3.2, the RMS and peak current also can be included in this methodology.

The layout represents the circuit at the physical level, which the interconnects and electrical components have geometric layers with different materials and dimensions. While the transistors have polysilicon, diffusion and metal layers which are isolated from each another by thin insulating layers, the metal layers represent the interconnects and resistors. In this mode, the Electrically Aware Design (EAD) tool from Cadence identifies the metal lines used to represent the interconnects and indicates the current density, width, and length of the lines, which are used to calculate the EM resistance change. Besides the current density and the dimensions extracted from the layout, the resistance change depends on the resistivities of the metal and barrier materials, as well as on the width and thickness of the barrier.

The calculated EM resistance is inserted in the circuit to evaluate the IC performance degradation compared with a circuit model, free of the EM in a verification environment named testbench. The designer can add the EM resistance manually, including resistors in the interconnect lines of the schematic, or an extra layer in the layout to represent the increased resistance. In an automatic mode, the change of the original

resistance value of the lines is directly included in the netlist which is generated from the parasitic extractor. The automatic mode is more accurate as the extra resistance manually included in the circuit can result in larger capacitance and resistance parasitics.

In the testbench, the designer defines the stimulus used as the inputs signals, chooses the analysis to simulate the performance of the circuit, and collects the output signals. Typically, industry-standard VHDL, Verilog, or other hardware description languages (HDL) is used to create a digital circuit testbench. For analog circuits, transistors or an HDL adequate for analog simulation is applied. In this way, the designer can evaluate the performance change of the circuit with the lines affected by the EM, and understand the lines which degrade the different performance parameters. Besides the circuit performance, the simulation of the EM impact on the threshold voltage, transconductance, and other parameters of the transistor is useful to find the more sensible parts in the circuit.

The resistance change of the metal lines depends on the temperature dissipated by the transistors (ΔT_{PT}) as shown the methodology flow in Figure 3.3(a). In turn, the ΔT_{PT} depends on the power dissipated by the transistors (P_T), the metal layers position and parameters of the vias and metal layers used to calculate the effective conductivity of the BEOL. The number of vias (N_{via}), width of the vias (W_{via}), length of the lines (L), and width of the lines (W) are extracted from the layout to calculate the fraction volume of metal and vias. The parameters obtained from technology are the thickness of the via layer (L_n^{via}), the thickness of the metal layer (L_n^{int}) and the conductivities of the metal (k_m) and insulator (k_i). Figure 3.3(b) shows the main procedures to calculate the ΔT_{PT}.

The power dissipated by the transistors is obtained in the testbench. The power dissipation in CMOS ICs has a static and a dynamic contribution. The dynamic power is due to switching currents required to charge/discharge output loads and short circuit currents that flow between the transistors as the input signal changes [196]. The static power is due to leakage sources in the transistors, including reverse bias pn-junction leakage between the source/drain and substrate and the subthreshold conduction between source and drain [196]. The power dissipation typically with a predominant dynamic parcel, became more static, as the static power increases with every new technology node. Below 65 nm technology node, the static power exceeds the dynamic power dissipation in some advanced circuits [197].

The effective conductivity of the BEOL (k_{eff}^{beol}) given by (2.9) depends on the used materials. As mentioned before, we consider only the volume fraction of the metals and insulators in k_{eff}^{beol}. A typical advanced IC has a volume fraction of 2% to 6% for vias and 28% to 42% for the metal layers, in relation to the layer volume [133]. The volume fraction of metals is the metal volume occupied in a layer, obtained with the length and width from all the lines. While the short lines can affect the k_{eff}^{beol}, the longer lines cause

an insignificant change in the effective conductivity, as explained in Appendix F.

3.3 Description of an IC Performance Change under EM

ICs have different metrics of performance depending on the application. For digital circuits, the designer has to optimize the area, the delay and the power, which leads to trade-offs, since a faster circuit requires a higher current driving, which increases the power consumption, or an smaller area to reduce the RC delay in the lines. Despite fewer transistors in an analog circuit, the analog designer evaluates gain, slew-rate, frequency, power consumption, settling time, offset, noise, etc, resulting in a complex analysis. Similarly to aging effects on the transistors, an interconnect line affected by EM can degrade more than one performance metric. Therefore, the designer has to identify the critical lines, i.e. the lines that degrade the circuit performance more significantly.

Figure 3.4 illustrates the variation of three performance parameters, named P1, P2 and P3, due to EM on one wire. In Figure 3.4(a) the performance parameter P1 decreases by 20% *before* the time t_1, while the performance parameter P2 decay 20% *after* t_1, as shown in Figure 3.4(b). In turn, the parameter P3 in Figure 3.4(c), experiences a non-linear reduction after the time t_2. Considering that a performance variation (ΔP) larger than 20% results in a significant degradation of the circuit operation, the parameter P1 is the most affected by the EM as it reaches the critical ΔP earlier.

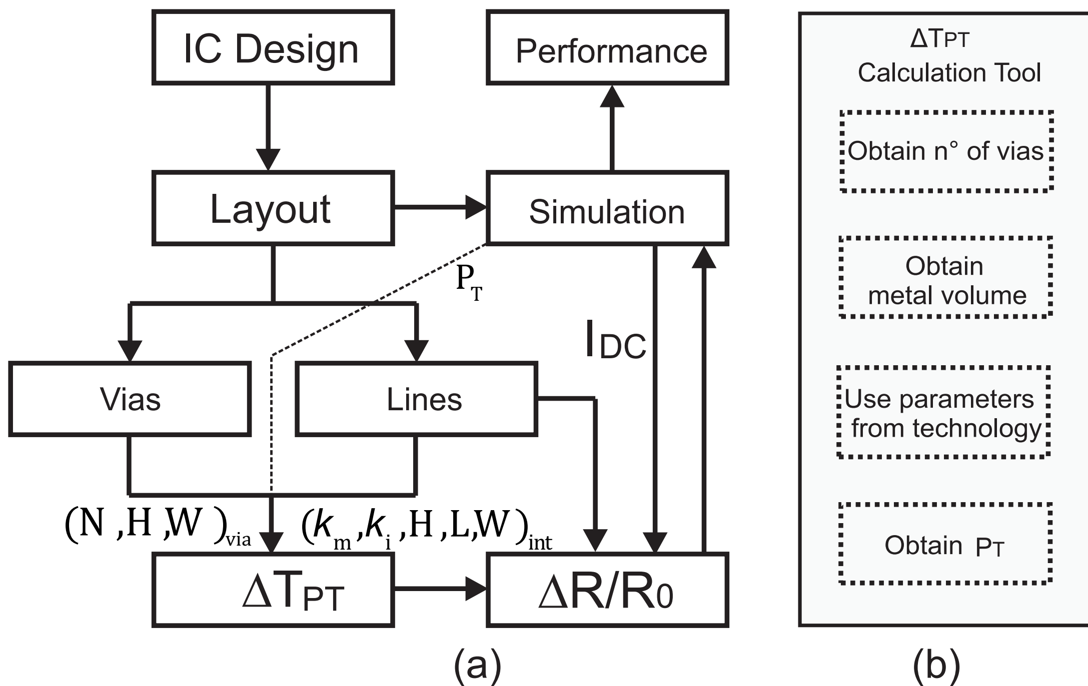

Figure 3.3 – (a) Methodology flow to calculate the ΔT_{PT} of the interconnects. (b) Main procedures to calculate the ΔT_{PT}.

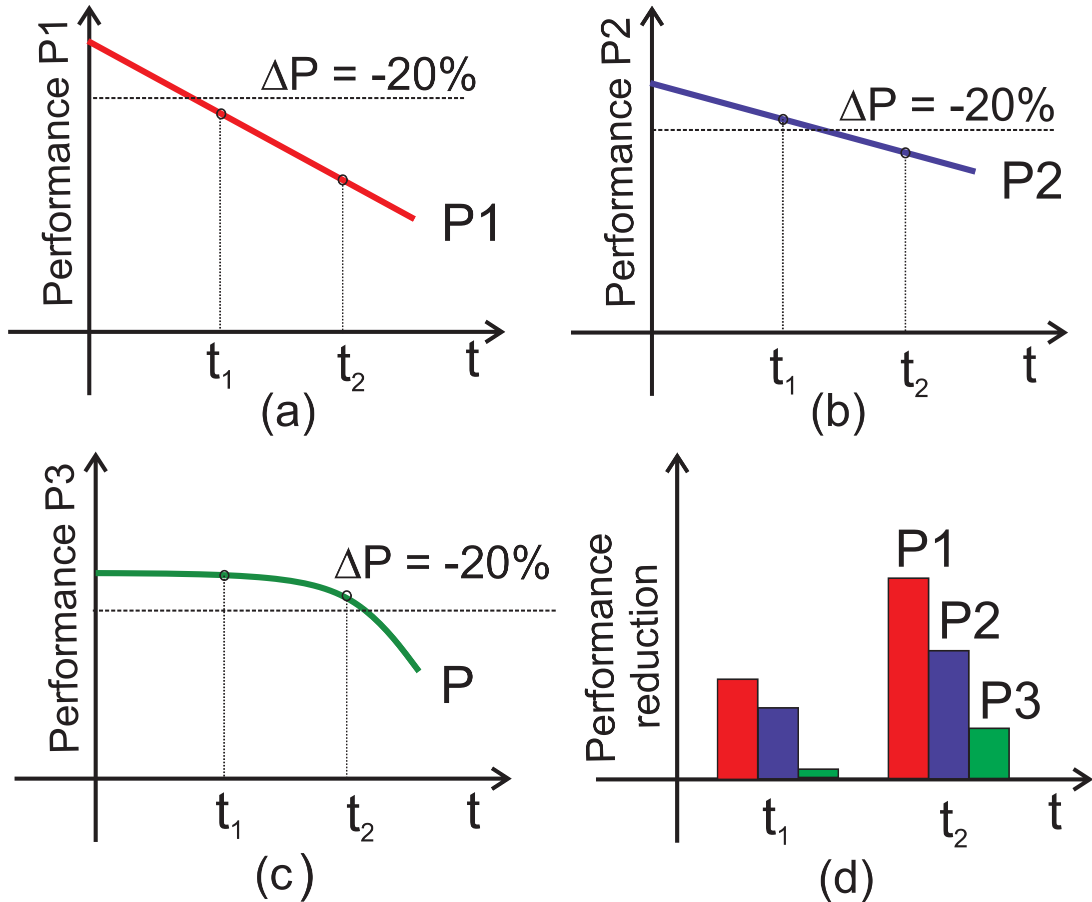

Figure 3.4 – Performance parameters P1 (a), P2 (b) and P3 (c) variation due to EM on one wire. In (d) P1, P2 and P3 reduction after t_1 and t_2.

Figure 3.4 indicates evaluations that the designer has to consider in the EM analysis. First, the designer has to associate the EM to the chip performance and the application. If t_1 is the time expected to a commercial application, the wire under EM effects needs some fix to increase the IC performance P1. In turn, if t_2 is the time expected for military or space application, the performance P2 also needs improvement.

Second, the designer has to choose the most relevant IC performance parameters for the EM evaluation. While the gain of an amplifier can be more critical for audio applications, the offset can be more important for application in high frequency. Although the performance P1 has a larger percentual variation than P2 in Figure 3.4(d), the parameter P2 can have a smaller margin to change and, as a consequence, be more critical. In this example, the same safe margin of 20% has been used for all the performance parameters, although the safe margin is generally different for each performance parameter. Thus, the designer has to evaluate the safe margin for the chosen parameters using the corner simulation, which includes extreme cases of temperature, voltage, and process.

Third, the designer has to identify the lines which affect each performance parameter of the chip. Besides the line evaluated, other lines under EM effects can degrade

the IC performance. As some lines are more sensitive to a resistance variation, mainly the RF lines, a Monte Carlo analysis is crucial to understand the critical lines of the circuit. The analysis of the most critical lines for each IC performance parameter allows the designer to identify all the lines that can cause a performance degradation and a premature chip failure.

3.4 Identification of the Critical Lines based on EM Criteria

Figure 3.5 illustrates metal lines classified as critical due to EM based on the $\Delta R/R_0$ criterion. Depending on the accuracy of the parameters used to calculate the resistance change, lines in intermediary condition, represented in black, can be classified as critical or non-critical. The critical lines represented in red have a critical $\Delta R/R_0$ change in a shorter time than the EM safe lines in blue. While some lines are critical with a lower resistance change, other lines with a higher resistance change are non-critical.

A good reliability analysis adopts strategy to improve the accuracy and the time to identify the EM critical lines. The Blech product and the maximum current density are two criteria commonly used to filter the lines susceptible to failure. Along with these traditional criteria, the inclusion of a performance degradation criterion allows the designer to understand the EM effect on the circuit and to fix in the layout the lines which lead to performance degradation and failure of the circuit.

Figure 3.6 presents an example of the EM criteria applied to evaluate four interconnects L1, L2, L3, and L4. Blech product criterion, shown in Figure 3.6(a), has a critical margin below the threshold, below which the lines are considered EM safe. The critical margin guarantees that a line near the threshold does not result in a wrong analysis. Note that the lines L2 and L3 are not critical. The line L1 is critical, as the Blech product is larger than the threshold. In turn, the line L4 is below the threshold; nevertheless, it is critical as it lies in the critical margin.

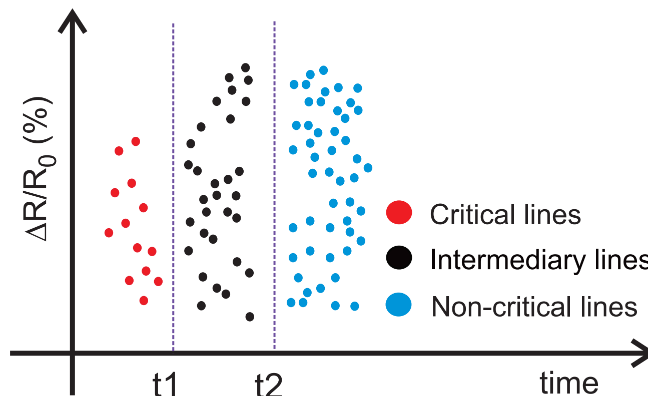

Figure 3.5 – Classification of the critical lines due to EM based on $\Delta R/R_0$.

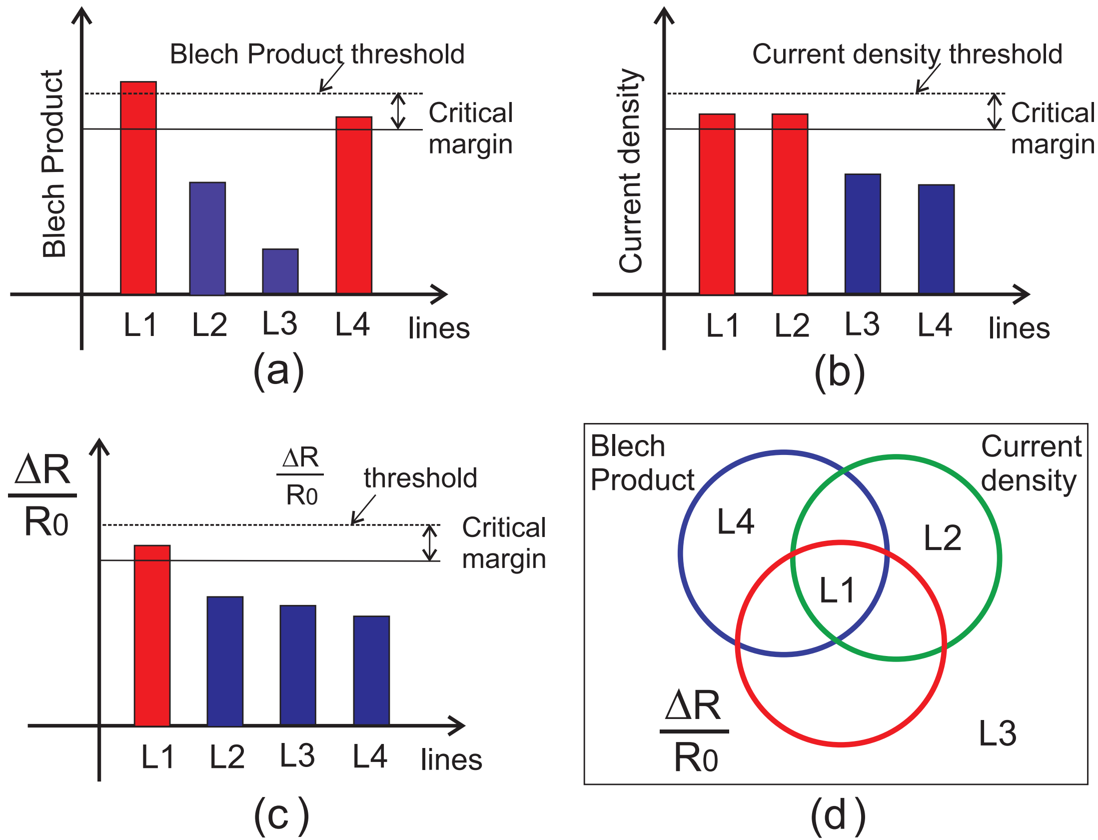

Figure 3.6 – Example of the EM criteria applied to evaluate four interconnects L1, L2, L3, and L4. (a) Blech product. (b) Maximum current density. (c) Resistance degradation. (d) Venn Diagram.

Figure 3.6(b) illustrates the interconnect evaluation based on the maximum current density criterion. Here, the EM safe lines L3 and L4 are below the critical margin. L1 and L2 are critical, as these lines have a current density in the critical margin.

Similarly, Figure 3.6(c) shows the resistance degradation criterion, which indicates that L1 is critical. A critical line is typically defined for a resistance increase of 10% [170]. Note that the threshold here is a fixed percentual. In our methodology, a critical line is defined for a resistance increase which results in a significant degradation of the circuit performance. Thus, each interconnect line can have a different threshold and a line can be critical with variation as small as 5% and not be critical with variation as large as 20% [198].

Figure 3.6(d) shows a report of the four lines in a Venn Diagram. As the L1 is critical for the three criteria, this line has a higher probability of suffering EM and affecting the circuit performance. L2 and L4 are also prone to suffer EM degradation; nevertheless, its resistance change due to EM probably does not affect the chip performance. In turn, L3 does not present a significant EM degradation and its resistance increase does not affect the chip performance.

3.5 Evaluation of Interconnects' Dimensions

Based on the current though the line (I), the analog designer chooses the width (w) of the line to guarantee a current density below the maximum current density (j_{max}) according to [199]

$$w > \frac{I}{h \cdot j_{max}}. \tag{3.1}$$

The thickness of the lines (h) is fixed. The analog designer adjusts the width of the lines manually, respecting the minimum distance to the other metal lines. Figure 3.7(a) shows a case with two interconnects, L1 and L2, where the line L1 has a higher current and, thus, a larger width than the line L2.

According to the Blech product, the lines with jL product above the Blech product threshold jL_c are susceptible to failure. In this way, the designer can choose the width as a function of the length of the line (L), according to [114]

$$w > \frac{IL}{h \cdot jL_c}. \tag{3.2}$$

Figure 3.7(b) illustrates the interconnect sizing according to the Blech product criterion.

A third method to design the lines uses the EM resistance change criterion. A larger width retards the EM, as the void needs more time to grow larger. Figure 3.7(c) shows a case where L2 is wider than L1, which means that L2 has a bigger impact on the performance of the circuit.

From (2.14), the barrier area of the line is given by

$$A_b = \frac{\rho_b D \left|Z\right| eI\Delta t}{kTL} \left(\frac{\Delta R}{R_0}\right)^{-1}, \tag{3.3}$$

where the parameters from these equations is explained in session 2.4.2. With the barrier area from (2.12), the width of the line based on EM resistance change is given by

$$w = \frac{\rho_b D \left|Z\right| eI\Delta t}{kTLt_b} \left(\frac{\Delta R}{R_0}\right)^{-1} - 2w_b\left(1 + \frac{h}{t_b}\right). \tag{3.4}$$

As the width of the line must have ($\Delta R/R_0$) below the maximum resistance ratio change

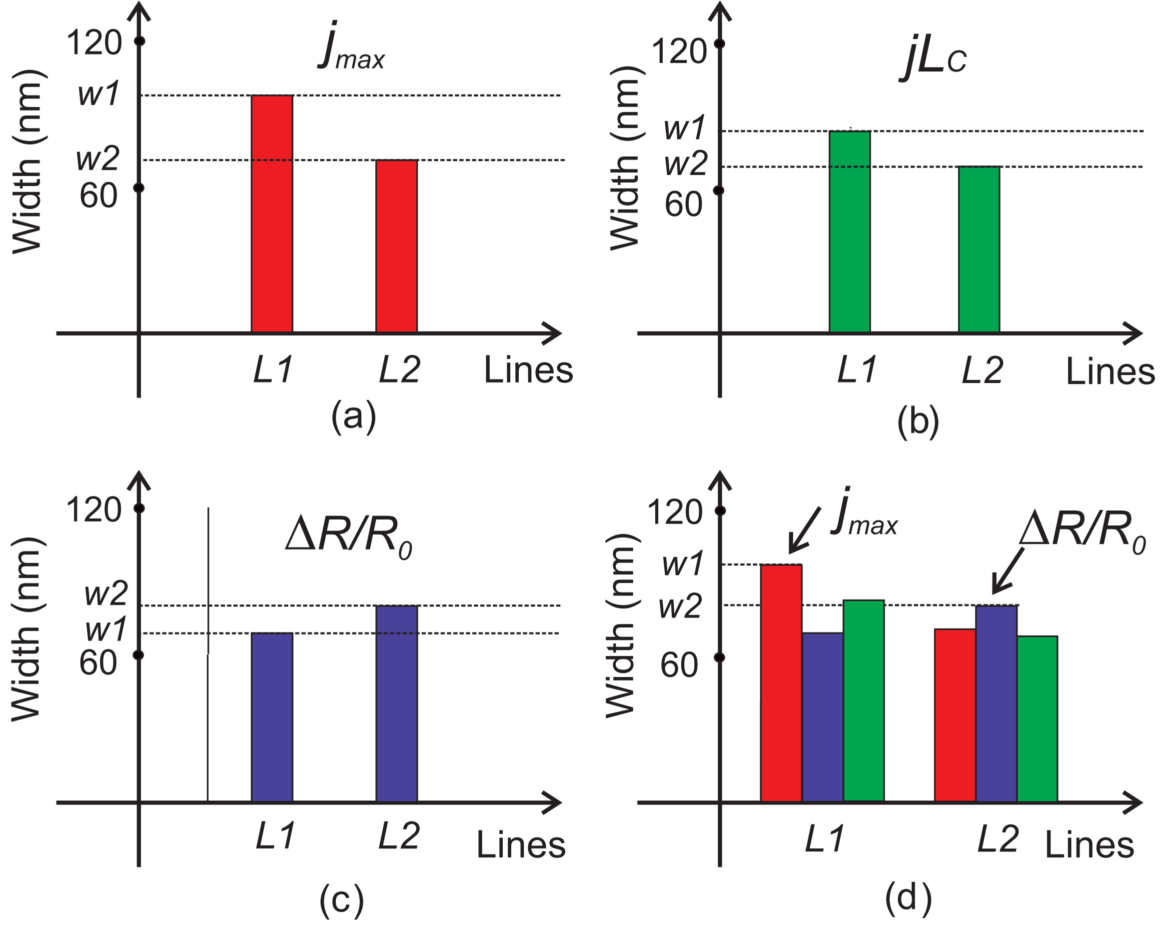

Figure 3.7 – Sizing the width of the lines L1 and L2 following EM criteria. (a) Based on the maximum current density. (b) Based on the Blech product. (c) Based on the resistance degradation. (d) Comparison between the three criteria.

$(\Delta R/R_0)_{max}$, expressed by

$$\left(\frac{\Delta R}{R_0}\right) < \left(\frac{\Delta R}{R_0}\right)_{max}, \tag{3.5}$$

the width of the line is related by

$$w > \frac{\rho_b D\,|Z|\,eI\Delta t}{kTLt_b}\left(\frac{\Delta R}{R_0}\right)_{max}^{-1} - 2w_b\left(1+\frac{h}{t_b}\right). \tag{3.6}$$

Figure 3.7(d) shows a comparison of the width of the lines based on the three criteria. Each criterion indicates the minimum width recommended for an interconnect. While the maximum current density limits the width of the line L1, the line L2 has the width determined by the resistance change criterion. Thus, the adequate width of each line can be more accurately determined.

3.6 Evaluation of the EM Critical Blocks

Floorplanning is an essential design step to strategically evaluate the placement of the blocks in an integrated circuit, providing an estimation of the area and position of each blocks. With the temperature increase intensifying the EM issues in the chips, the designer requires new methods for floorplanning the blocks, identifying the more critical lines due to EM and protecting the thermal sensitive regions.

Figure 3.8 shows the methodology flow to evaluate the potential EM critical blocks comparing the estimated temperature (T), that is the sum of the temperature of reference (T_0) and the estimated temperature change (ΔT_{PT}), with the maximum allowed temperature (T_{max}). If T is higher than the T_{max}, it increases the probability of a block to have EM critical lines and, thus to be a critical block. From the schematic, the power dissipated by the transistors (P_T) is simulated, and from the layout the metal and via volume fractions are obtained. These data are used to estimate the temperature of the blocks. The $(\Delta R/R_0)_{max}$ of the interconnects is determined from an evaluation of the performance metrics.

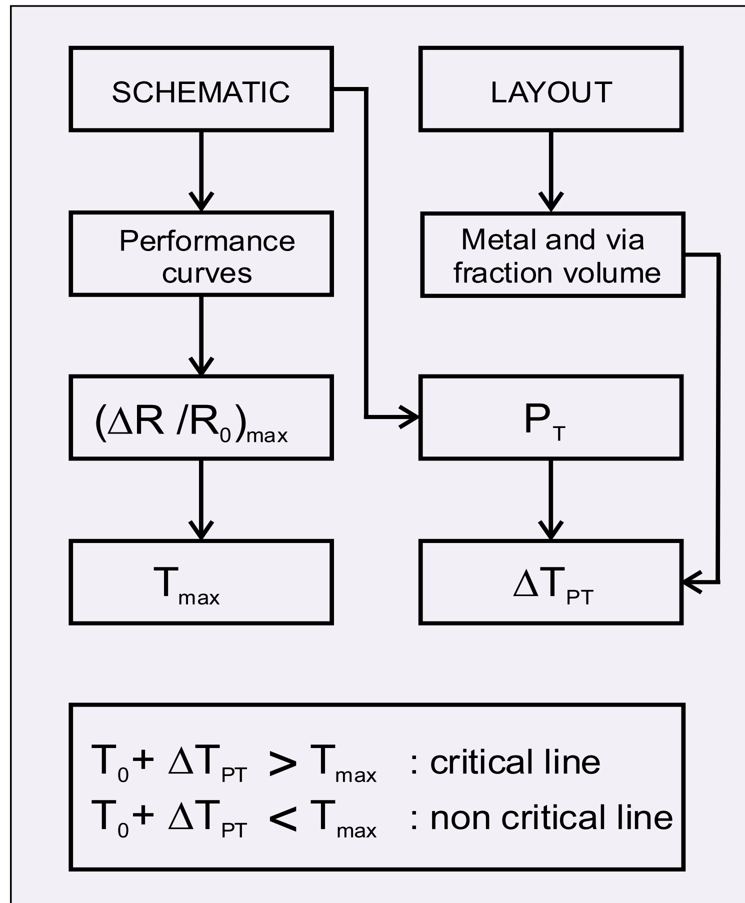

Figure 3.8 – Methodology flow to evaluate the EM critical blocks in a chip.

From (2.14), the maximum temperature of an interconnect T_{max} is given by

$$T_{max} \exp\left(\frac{E_a}{kT_{max}}\right) = \frac{D_0 \rho_b e I \Delta t \,|Z^*|}{A_b k L}\left[\left(\frac{\Delta R}{R_0}\right)_{max}\right]^{-1}, \tag{3.7}$$

which is based on the $(\Delta R/R_0)_{max}$ and the current through the line.

The probability of a block to be critical is based on the probability of the lines to operate above the T_{max}. An EM critical line has the temperature ratio given by

$$\frac{T_0 + \Delta T_{PT}}{T_{max}} > 1. \tag{3.8}$$

The maximum temperature have different restrictions, depending if the use is for commercial, military or space. This methodology can be used to reposition the blocks in a layout, protecting those circuits that have more critical lines due to EM and increasing the IC reliability.

3.7 EM Methodology Flow

Figure 3.9 shows the full methodology flow to evaluate and size the interconnects based on the EM criteria. In addition to the traditional IC design flow from Cadence, we include tools to calculate ΔR_{EM}, ΔT_{PT} and the width of the lines, as well as a tool to filter the EM critical lines. In a traditional analog design flow, the DRC and the LVS tools verify the layout, while the Quantus QRC Extraction Solution tool extracts the parasitics. With the parasitics, the designer simulates the current and the power dissipated by the transistors. Along with the simulated power, the number of vias and the metal volume fraction extracted from the layout is used to calculate the temperature in each metallic layer. Next, the EAD tool provides the resistance and the width of the lines, which, along with the simulated current and the estimated temperature, is used to calculate the resistance change of the lines. The $\Delta R/R_0$ change of the lines is determined according to the expected circuit lifetime.

The maximum current density, the Blech product and the $\Delta R/R_0$ criteria filter the EM critical lines. After adding the EM resistance change to the initial resistance of the critical lines, the EM on the chip performance is evaluated. For this purpose, the ADE Spectre tool is applied to simulate, at a given Δt, the netlist with the resistance change of the lines included in a testbench in the Virtuoso (VLS). Then the circuit performance is compared against an EM-free circuit using the Cadence calculator. If the performance change is above the expected, the interconnect line has to be modified to retard the EM

for the expected circuit lifetime. To evaluate the width of the interconnects and provide a more reliable and accurate design, the designer considers the recommended width of the lines based on the three EM criteria. Finally, a report with the critical lines based on the three EM criteria and the recommended lines' widths for the design is issued.

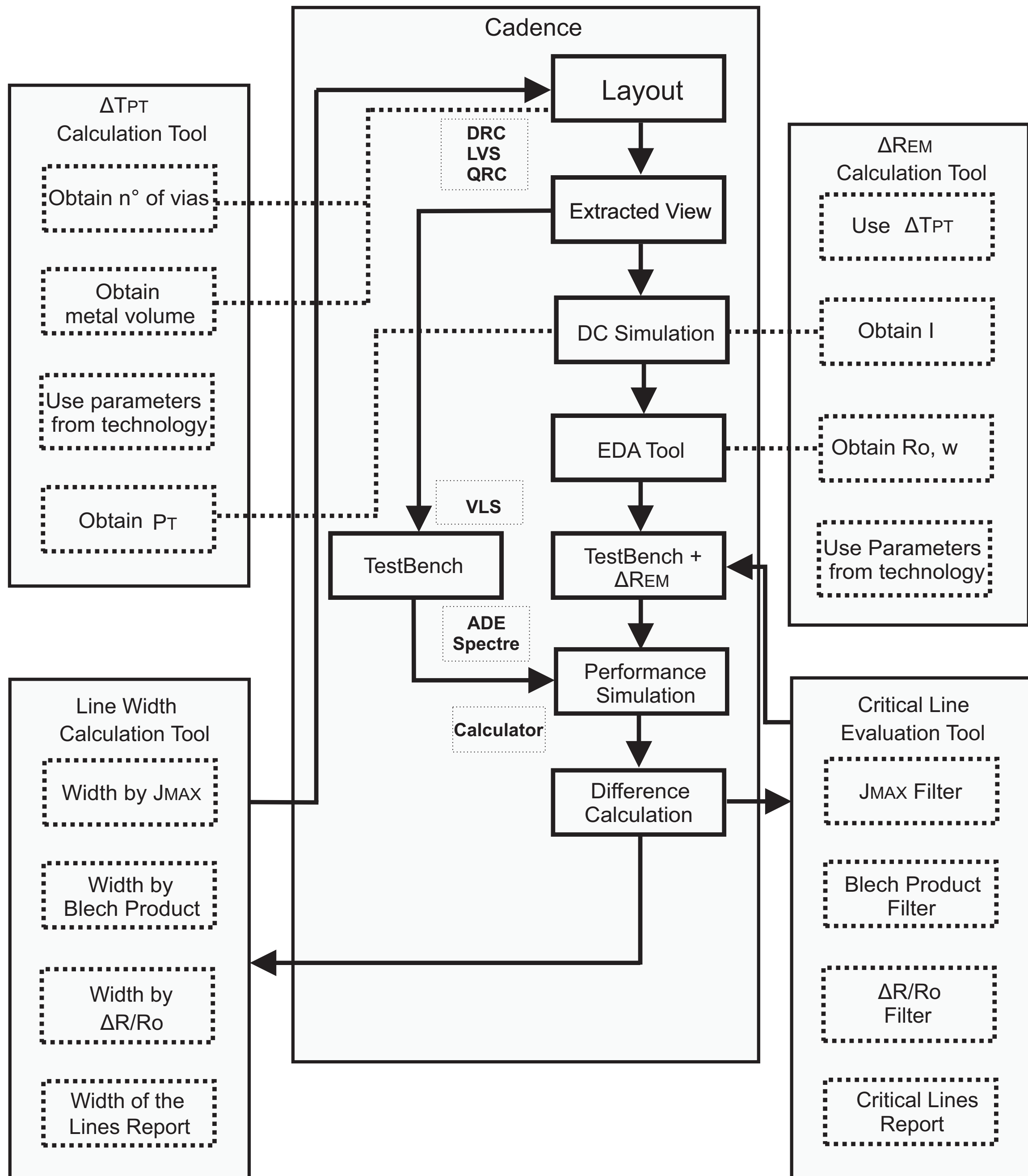

Figure 3.9 – Full methodology to evaluate the EM on chips. Cadence tools are used complemented by tools to calculate the ΔR_{EM}, ΔT_{PT}, the width of the lines, and to determine the critical lines, which were developed during this work.

4 Analysis of the Temperature Estimation

In this chapter the estimated temperature change (ΔT_{PT}) of the interconnect lines is investigated. First, the ΔT_{PT} is compared with the temperature simulated with a FEM 2-D model. After, the importance of the ΔT_{PT} in the resistance ratio $\Delta R/R_0$ of the lines is shown. The last session shows the evaluation of the critical circuits based on the temperature.

4.1 Temperature Distribution on BEOL Interconnects

The temperature and the current density are the two parameters that mostly affect the EM resistance change of the lines. Inaccuracies in these parameters result in a overestimated or underestimated resistance change and, as a consequence, in a misleading EM evaluation. Thus the EM analysis has to consider the temperature increase in the metal layers due to the power dissipated by the transistors.

Figure 4.1 illustrates a temperature distribution on a chip with a length from x_1 to x_2 and a width from y_1 to y_2. Here, the primary heat source in the center of the chip produces heat that flows into the BEOL and changes the temperature of the lines. The temperature in regions further away from the heat source, in particular at the corners A, B, C, and D, undergoes a lower change.

The finite element method (FEM) is a useful tool to understand the effect of heat transfer from transistors in the silicon substrate. With FEM, we simulate the temperature change in the interconnects with the 2D physical model for the BEOL shown

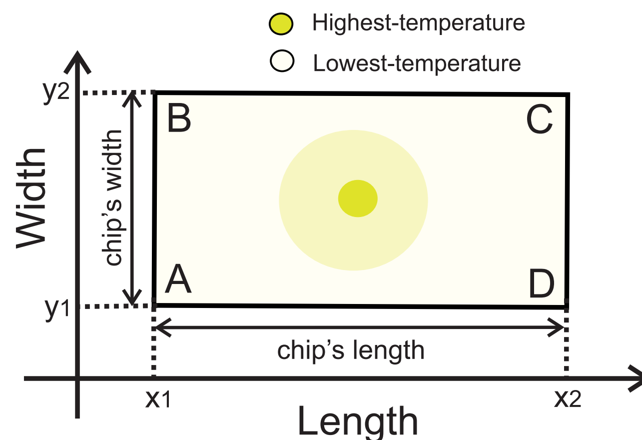

Figure 4.1 – Top view of the temperature distribution on a chip with a primary heat source in the center.

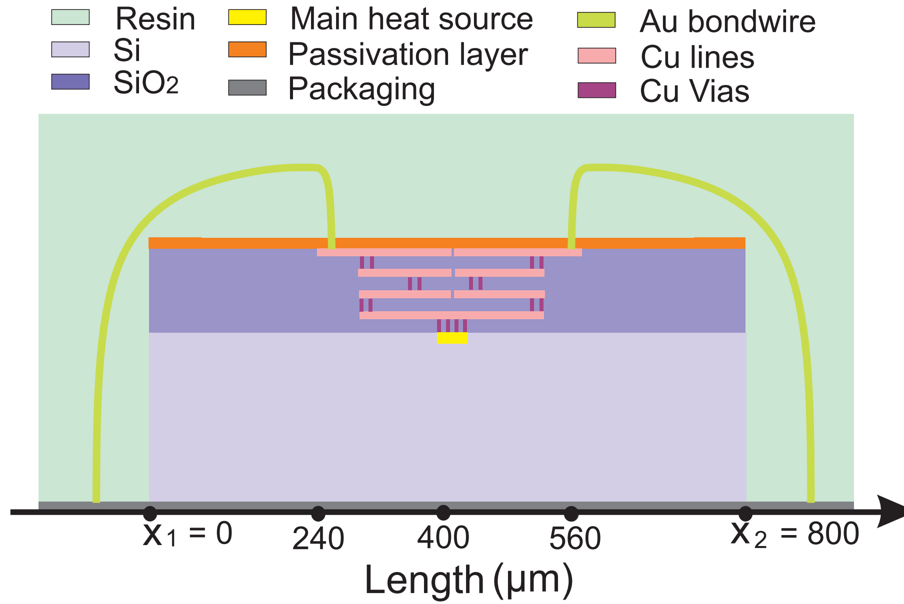

Figure 4.2 – Cross section of the BEOL and FEOL structure model used to simulate the temperature in metal layers.

in Figure 4.2, developed based on 45 nm technology [171]. The BEOL has 11 layers of interconnects and 10 of vias, with 6% of volume fraction of the vias and 40% of volume fraction of the metal in each layer. A very low thermal conductivity epoxy resin isolates gold bond wires which are connected to the packaging. The thermal conductivity of the materials, dimensions of the vias and the metal layers, etc are described in Table 4.1.

In the first case, we simulate the thermal distribution on the BEOL from $x_1 = 240$ μm to $x_2 = 560$ μm with the primary heat source in the center of the chip at $x = 400$ μm, and the power dissipation of 400 W/m. The transistors occupy a small region of 2 μm, equivalent to 0.25% of the width of the chip, resulting in a higher temperature in a narrow central region of the metal lines. In a typical integrated circuit, the transistors occupy a larger area, and as a consequence, the temperature distribution is more homogeneous along the lines. Besides the power dissipated by the transistors, the temperature change in each metallic layer (ΔT_{PT}) is a function of thermal conductivity of the several materials, the geometry of the layers, and the number of vias.

Figure 4.3 shows the temperature of lines from Metal 1 to Metal 11 from x=240 to 560 μm. The interconnects of the local layers near the primary heat source operate under the highest temperatures. As expected, the temperature near the corners A, B at $x = 240$ μm and C, D at $x = 560$ μm are significantly lower than in the center of the chip. The result considers the vias distributed at the end of the metallic layers, in a formation named quasi-manhattan structure [200]. The concentration of the vias near the heat source between the layers M2-M3, M4-M5, M6-M7, M8-M9 and M10-M11 results in the same ΔT_{PT} for the lines of these layers.

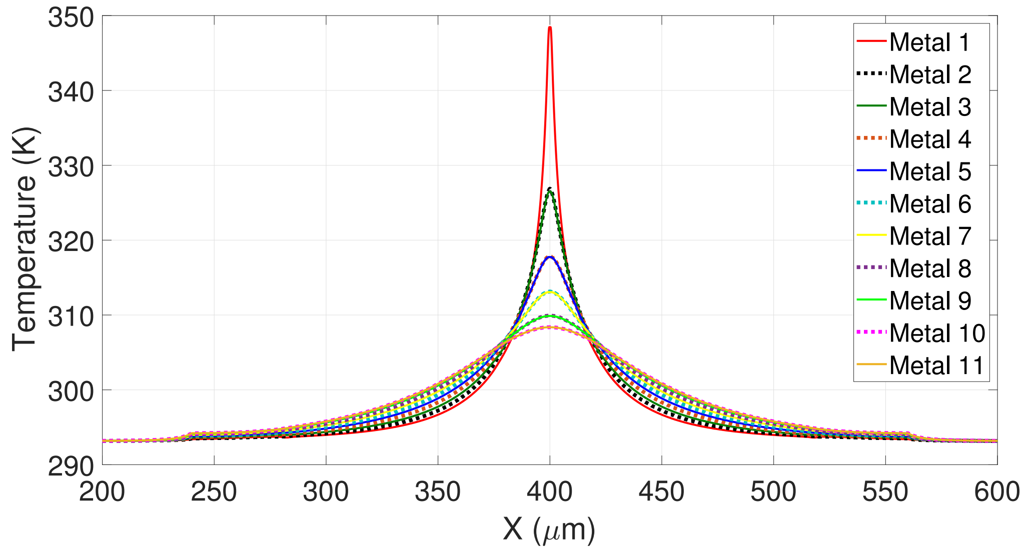

Figure 4.3 – Temperature on the BEOL with the heat source in the center of the chip at x = 400 μm and the power dissipation of 400 W/m.

Table 4.1 – Parameters used in the BEOL model simulated in the COMSOL [2].

Name	Value	Unit	Description
Si_thick	20000	nm	Si thickness
Chip_w	800000	nm	Chip's width
Contact_h	150	nm	Contact's heigth
via1_h and via2_h	150	nm	Vias1 and vias 2 heigth
via3_h to via9_h	180	nm	Vias3 and vias 9 heigth
via10_h to via11_h	1000	nm	Vias10 and vias 11 heigth
m1_t and m2_t	150	nm	Metal 1 and metal 2 thickness
m3_t to m8_t	180	nm	Metal 3 and metal 8 thickness
m9_t to m11_t	1000	nm	Metal 9 and metal 11 thickness
m1_per to m11_per	0.4	n.a.	Volume fraction of metal
contact_w	65	nm	Contact width
w_via12	65	nm	Via12 width
w_via23 and w_via34	70	nm	Via23 and Via34 width
w_via45 to w_via67	140	nm	Via45 and Via67 width
w_via78 and w_via89	400	nm	Via78 and Via89 width
w_via910 and w_via1011	800	nm	Via910 and Via1011 width
via1_per to via 10_per	0.06	n.a.	Volume fraction of via
via_distance	500	nm	Distance between vias
h_pack	100	nm	Packaging thickness
h_heat	60	nm	Heat source thickness
Circuit_W	2000	nm	Main Heat Source Width
w_bond_wire	2000	nm	Bond wire width
k_iso_SiO2	1.4	W/(Km)	SiO2 - Thermal conductivity
k_iso_Si	130	W/(Km)	Si - Thermal conductivity
k_iso_Cu	400	W/(Km)	Cu - Thermal conductivity
k_iso_A	0.18	W/(Km)	Acrylic - Thermal conductivity
Passivation_thick	5000	nm	Passivation thickness

In a second case, the primary heat source is near one of the chip's corners, shown in Figure 4.4. With the primary heat source near the corner A, the highest ΔT_{PT} of 57 K is at $x = 280$ μm and a lower ΔT_{PT} at the other corners, as shown in Figure 4.5. Observe that the primary heat source sized near the extremity results in a temperature of 333 K and 324 K in M2 and M3, equivalent to a ΔT_{PT} of 33 K and 24 K, respectivelly. Difererently from the first case, the others pairs M4-M5, M6-M7, M8-M9 and M10-M11

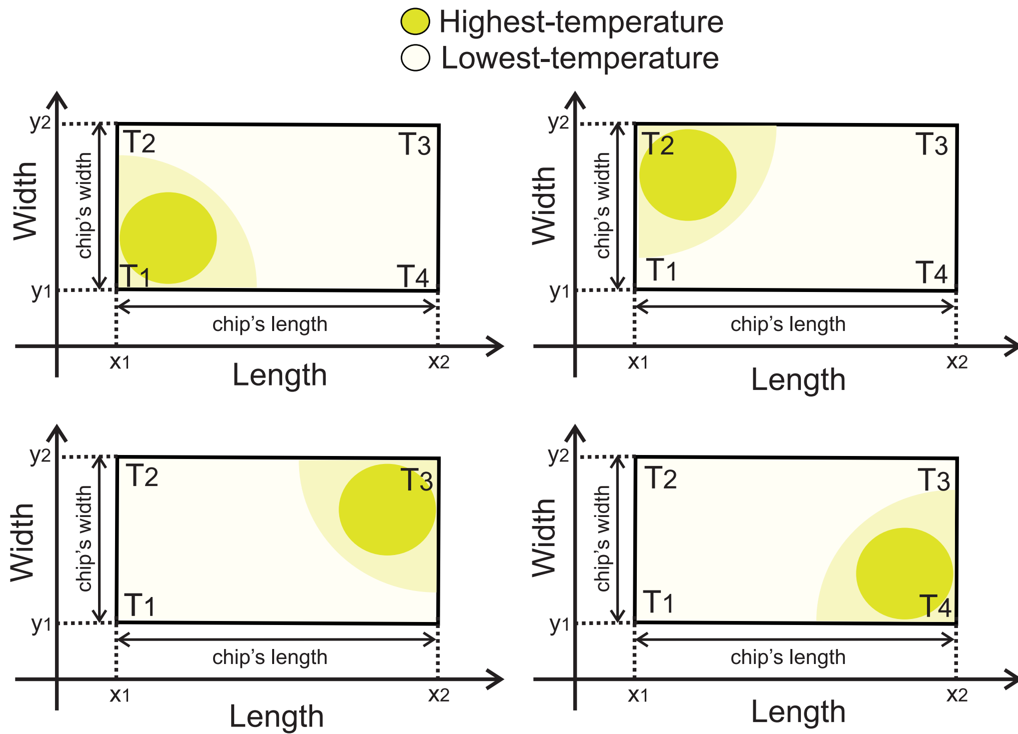

Figure 4.4 – Temperature distribution with the primary heat source near the corners of the chip.

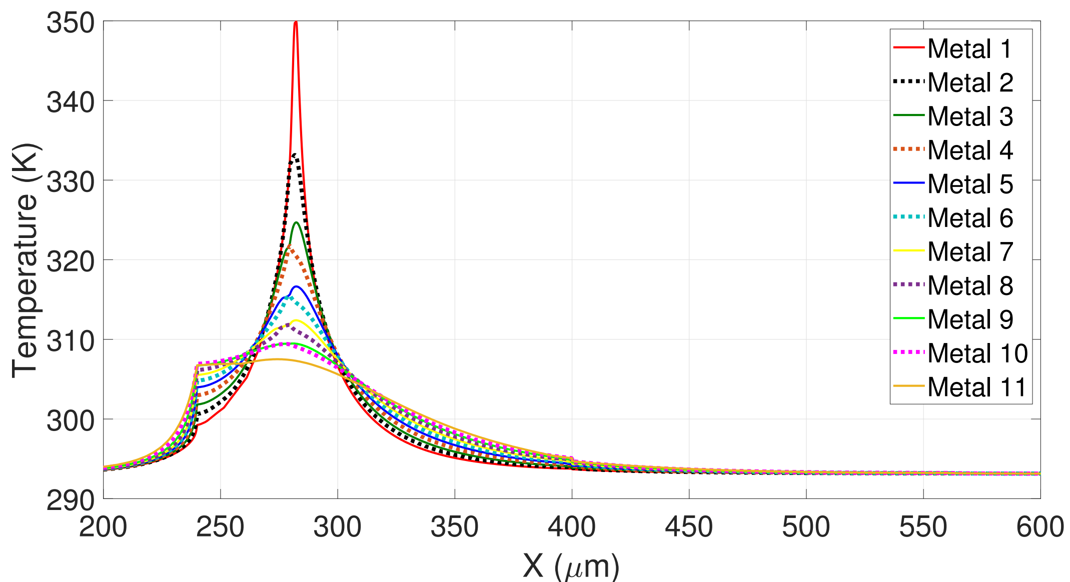

Figure 4.5 – Temperature on the BEOL with the primary heat source near the corner A of the chip at x = 280 μm and the power dissipation of 400 W/m.

also have a different ΔT_{PT} due to the position of the vias in the extremity of the metal layers, and the primary heat source placed in an intermediary position near the corner A.

In the third case, the center and regions near the corners have heat sources with the same power dissipation of 400 W/m, as illustrated in Figure 4.6. Figure 4.7 shows the temperature along the BEOL with the heat sources at the center at $x = 400$ μm and near the corners A and D, at $x = 280$ μm and at $x = 520$ μm. The inclusion of more heat sources increasing the power dissipated in the FEOL, increases the temperature on the BEOL as observed in the Metal 10 layer, which has the maximum temperature of 311 K,

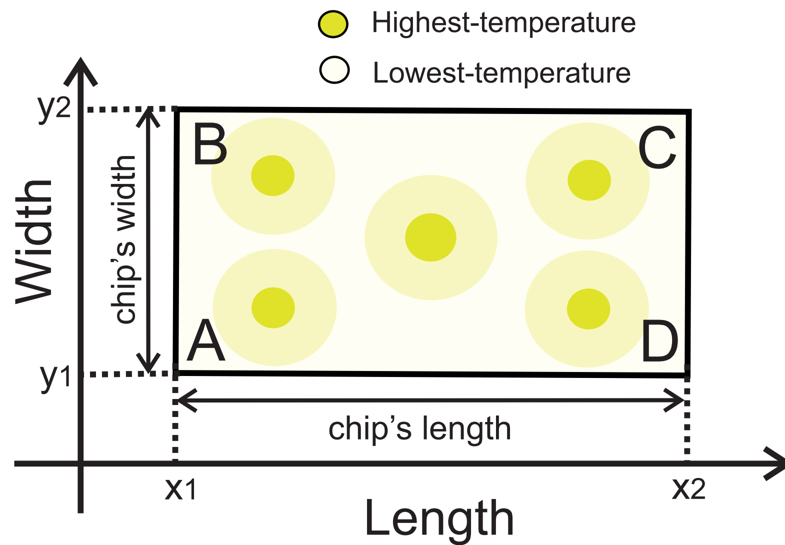

Figure 4.6 – Temperature distribution with heat sources at the center and near the corners of the chip.

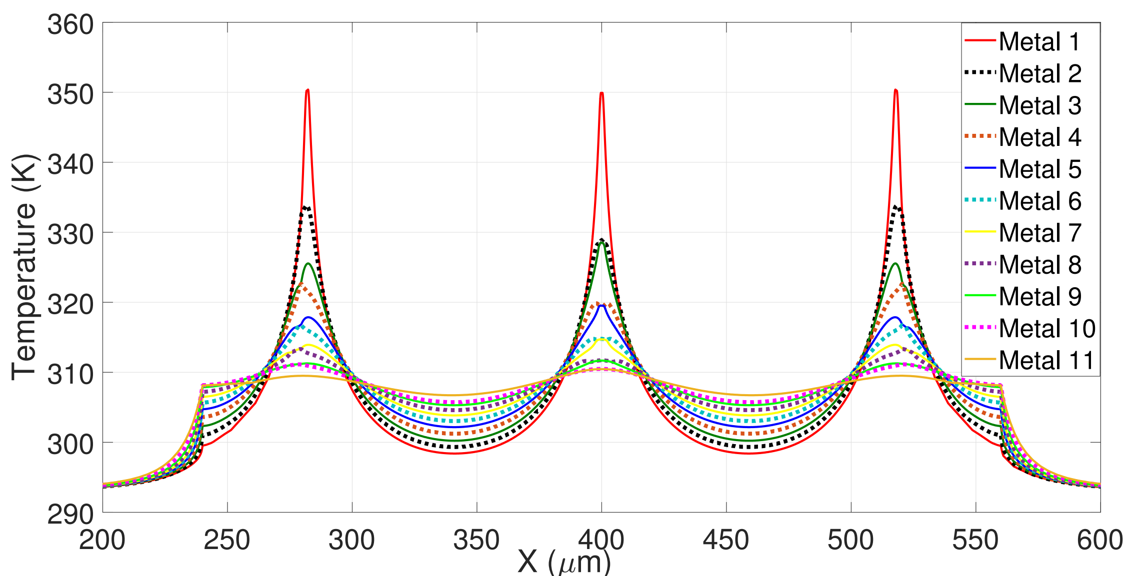

Figure 4.7 – Temperature on the BEOL with the primary heat source near the corners A and D at x = 280 μm and x = 520 μm, respectively and in the center of the chip at x = 520 μm, with P_T = 400 W/m.

equivalent to ΔT_{PT} of 11 K, 4 K higher than the case 2, and 3 K higher than the case 1. Note that the Metal 2 in the position 280 μm has a temperature of 334 K, 5 K higher than the Metal 2 positioned in 400 μm, in the center of the chip, indicating the influence of the position of the vias in the thermal distribution of the chip.

Figure 4.8 shows a comparison between the maximum temperature change on each metal layer estimated with (2.8) and simulated with the primary heat source at the center and at the corner (Figures 4.3 and 4.5). A large temperature difference between two consecutive layers is observed in the three curves. For example, the ΔT_{PT} in the Metal 1 layer is 56 K, 12 K higher than the ΔT_{PT} in the Metal 2. The results indicate that in Metal 1 the ΔT_{PT} of 56 K is near to the simulated temperature change of 55 K in Figures 4.3 and 4.5. The small difference of 1 K in the ΔT_{PT} has a relation with the different materials used in the simulation, such as the the material of the resin, substrate and bondwire, while the temperature estimated considers the effective conductivity from the Si and Cu. The distribution of the vias and the heat source position affect the temperature, as the heat flows in the BEOL more efficiently when the vias are positioned near the heat source, evidenced by the differences between the temperatures simulated in Figures 4.3 and 4.5. The calibration of the boundary conditions in the analytical model can contribute to a better estimation of the temperature, mainly in the top layers positioned above 3 μm in the BEOL height.

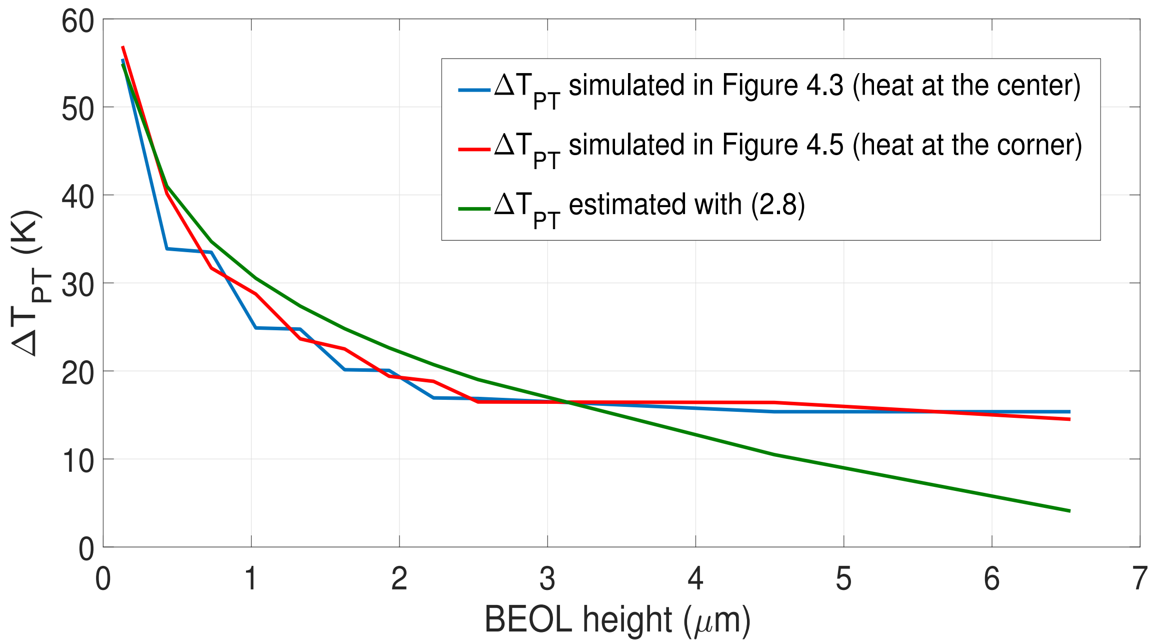

Figure 4.8 – Comparision between the maximum ΔT_{PT} estimated with (2.8) and simulated in Figure 4.3 and 4.5.

4.2 Impact of the Temperature Estimation on $\Delta R/R_0$

The temperature change increases the diffusivity exponentially, affecting $\Delta R/R_0$ and disturbing the EM evaluation. Besides the temperature, the current density, geometry, and materials of the lines can affect the EM evaluation.

To evaluate the impact of the ΔT_{PT} in $\Delta R/R_0$ and in the circuit lifetime, we simulate 176 paths from interconnects of an operational amplifier. The length and the width of the paths vary from 2 μm to 123 μm and from 0.06 μm to 1.7 μm, respectively, as illustrated in the histograms from Figure 4.9(a) and Figure 4.9(b). Here, the length is the longest metal line of an interconnect containing the path. The lines are designed with 3 metal layers, where 6 paths are Metal 3, 33 paths are Metal 1 and 137 paths are Metal 2, as shown in Figure 4.9(c). The resistance of each path is given in Figure 4.9(d). The histograms in Figure 4.9(e) and Figure 4.9(f) indicate the current density though the lines in relation to the maximum current density of 2 mA/μm for static and DC simulations. Note that some paths have the current density ratio (J/J_{max}) higher than 1 and operate under a current density above the maximum indicated by the technology, which accelerates the EM.

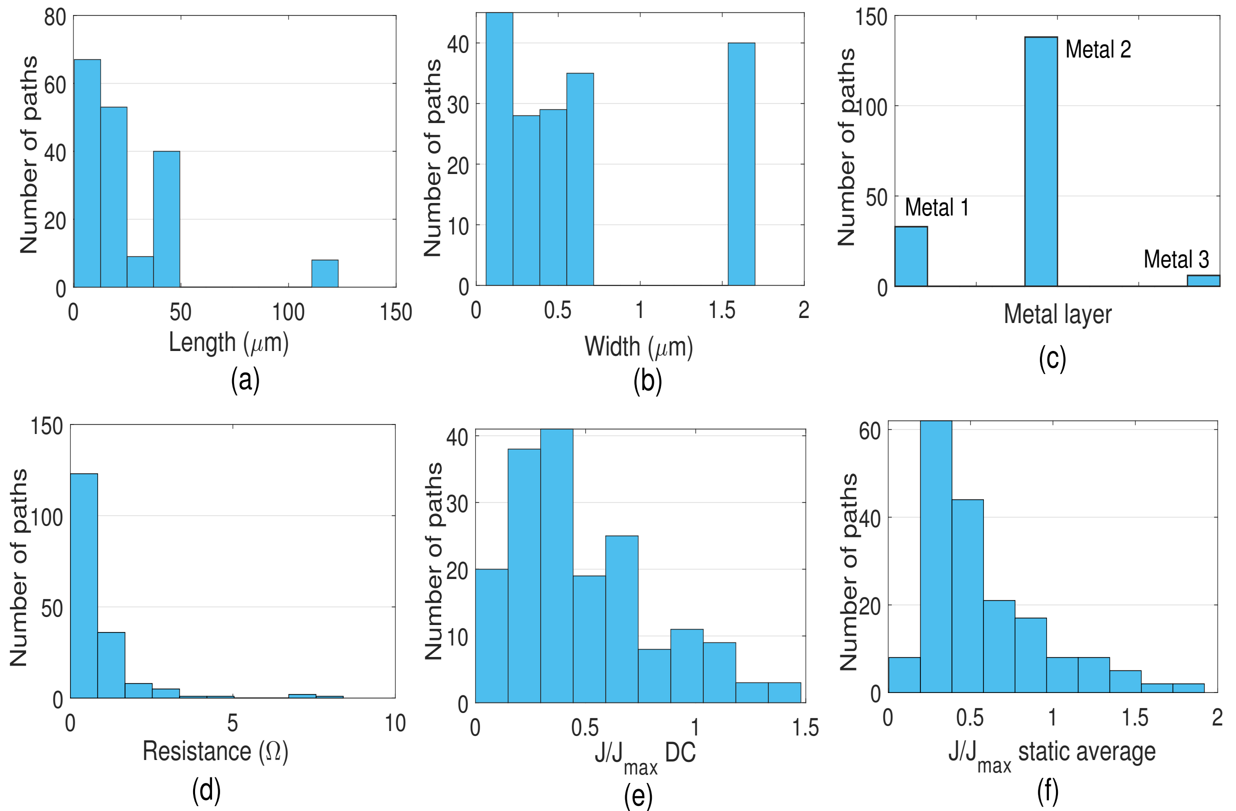

Figure 4.9 – Parameters to evaluate the lines of an operational amplifier: (a) Length. (b) Width. (c) Metal layer. (d) Resistance. (e) Current density ratio in DC operation. (f) Current density ratio in static operation.

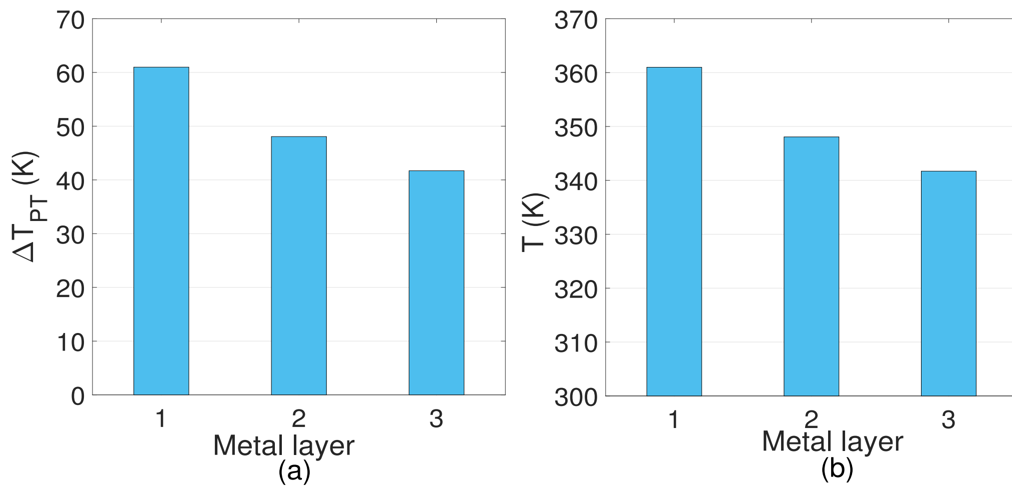

Figure 4.10 – (a) ΔT_{PT} in metal layers. (b) Temperature estimated in metal layers.

The average power dissipated per transistor is 75 μW, equivalent to a normalized power of 416 W/m, for the transistor's pitch of 180 nm. Figure 4.10(a) shows the ΔT_{PT} of 61 K, 48 K and 42 K for the Metal 1, Metal 2 and Metal 3 respectively. This results in a temperature of 361 K, 348 K, and 342 K, for a reference temperature of 300 K, as shown in Figure 4.10(b). The importance to estimate the temperature by layer is evident when observing the temperature in Metal 1, which is 19 K higher than the estimated temperature in the Metal 3 layer. Although the local layers have elevated temperature, ICs can support higher temperatures. A chip designed for a commercial application, for example, supports maximum temperatures of 398 K.

Figure 4.11 shows the time to the first ten interconnect paths failure, i.e., the time to ten paths suffer a critical resistance change due to EM. The MTTF_{10} in Figure

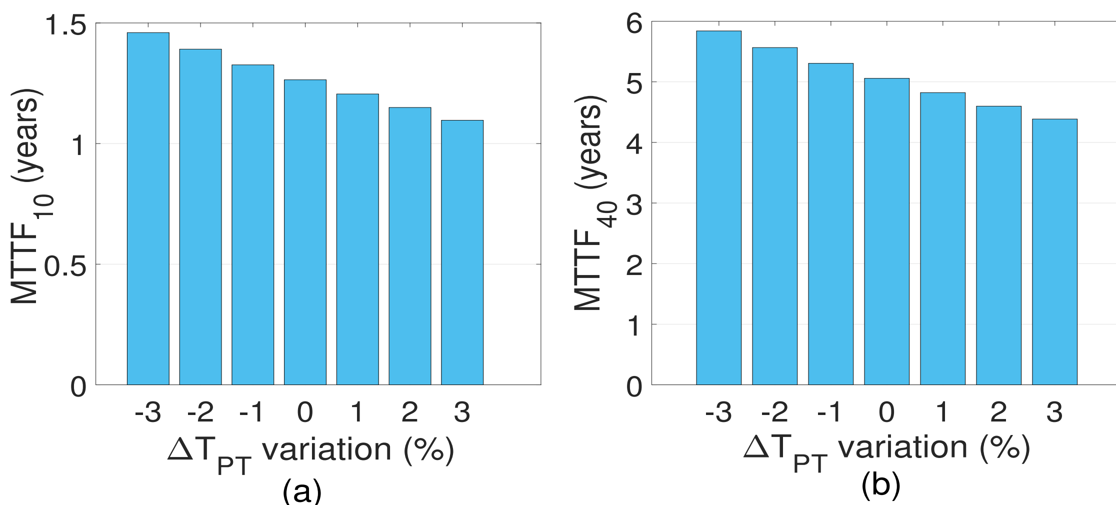

Figure 4.11 – (a) Time to the resistance of the lines increase 10% with a ΔT_{PT} variation from -3% to 3%. (b) Similar analysis with the critical resistance of the lines of 40%.

4.11(a) means that the critical resistance is 10%, while in Figure 4.11(b) the $MTTF_{40}$ represents the critical resistance of 40%. Observe in Figure 4.11(a) that a variation from -3% to 3% in ΔT_{PT} changes the $MTTF_{10}$ from 1.45 to 1.2 years. In Figure 4.11(b), the expected lifetime varies from 5.8 to 4.3 years for the same ΔT_{PT} variation. A reduction of some degrees in the temperature improves the MTTF of the circuit considerably. This analysis considers that the electronic circuit works full time. For a workload of 50%, the lifetime of the lines doubles.

The variation in the resistance change ratio $(\Delta R/R_0)_V$ is given by

$$\left(\frac{\Delta R}{R_0}\right)_V = \left|\left[\left(\frac{\Delta R}{R_0}\right)_1 - \left(\frac{\Delta R}{R_0}\right)_2\right]\right| \cdot \left[\left(\frac{\Delta R}{R_0}\right)_1\right]^{-1}, \tag{4.1}$$

where the resistance change ratio $(\Delta R/R_0)_1$ is a function of the estimated temperature (T) and the resistance change ratio $(\Delta R/R_0)_2$ is a function of the T plus the temperature difference ΔT_V.

From (2.14), $(\Delta R/R_0)_V$ is given by

$$\left(\frac{\Delta R}{R_0}\right)_V = \left|1 - \frac{T}{T + \Delta T_V} \exp\left[\frac{E_a}{k}\left(\frac{\Delta T_V}{T(T + \Delta T_V)}\right)\right]\right|. \tag{4.2}$$

Figure 4.12 shows the impacts of the ΔT_V variation of 3 K in the $(\Delta R/R_0)_V$ of the Metal 1, Metal 2 and Metal 3 lines from Figure 4.10. With a ΔT_V of 3 K the $(\Delta R/R_0)_V$ increases above 20%, indicating again the importance of consider the different temperatures on the BEOL in the estimation of the resistance change of the lines.

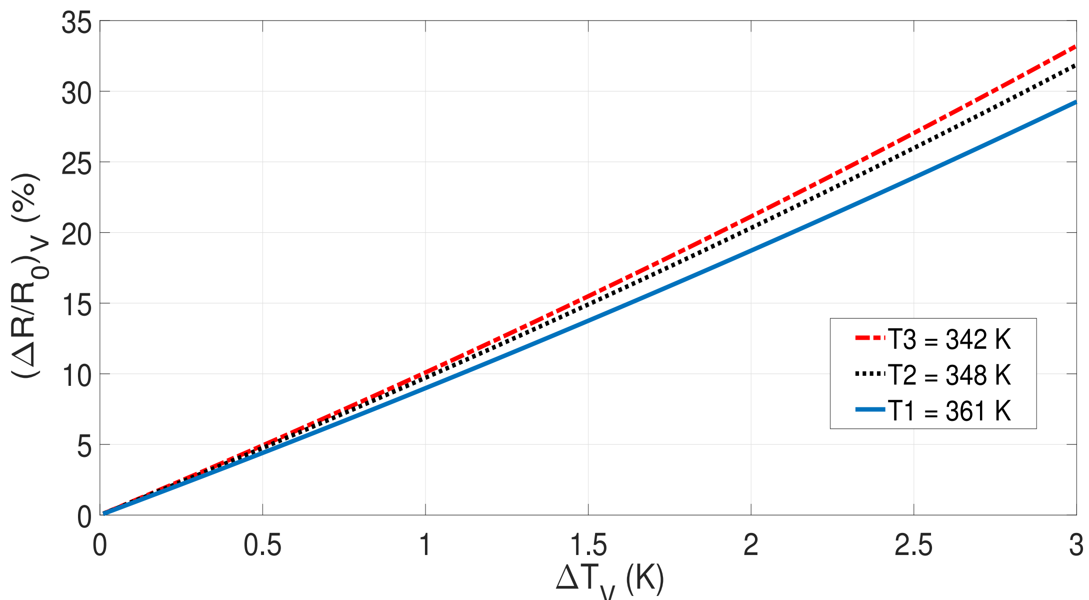

Figure 4.12 – $(\Delta R/R_0)_V$ of the lines with the ΔT_V from 0 to 3 K.

4.3 Evaluation of Critical Blocks based on the Temperature

To use the methodology proposed in section 3.6, we evaluate six sub-circuit blocks named B1 to B6 with the normalized power dissipation from transistors given in Figure 4.13(a). The block B4 has the highest power dissipation, and possibly the highest temperature in the interconnects. The blocks B1 and B2 are more sensitive to the temperature, therefore they are positioned far from B4, as in Figure 4.13(b). Each block contains 1000 interconnects operating under the maximum current density, with the $(\Delta R/R_0)_{max}$ variating from 5% to 50%, and the length of the lines variating from 10 μm to 125 μm, as shown in Figure 4.14.

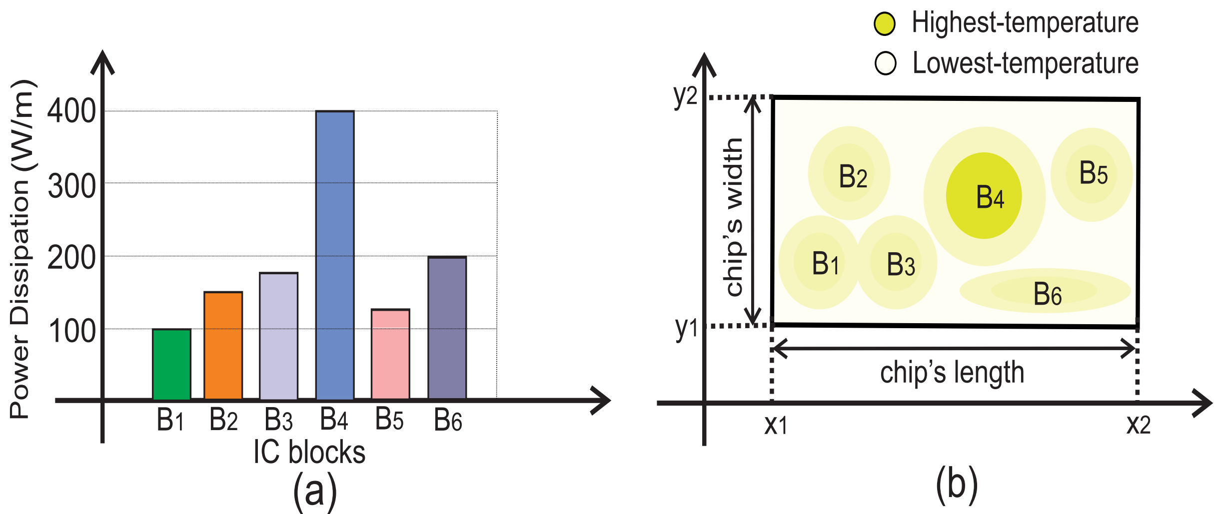

Figure 4.13 – (a) Power dissipation of the six blocks. (b) Temperature map of the chip.

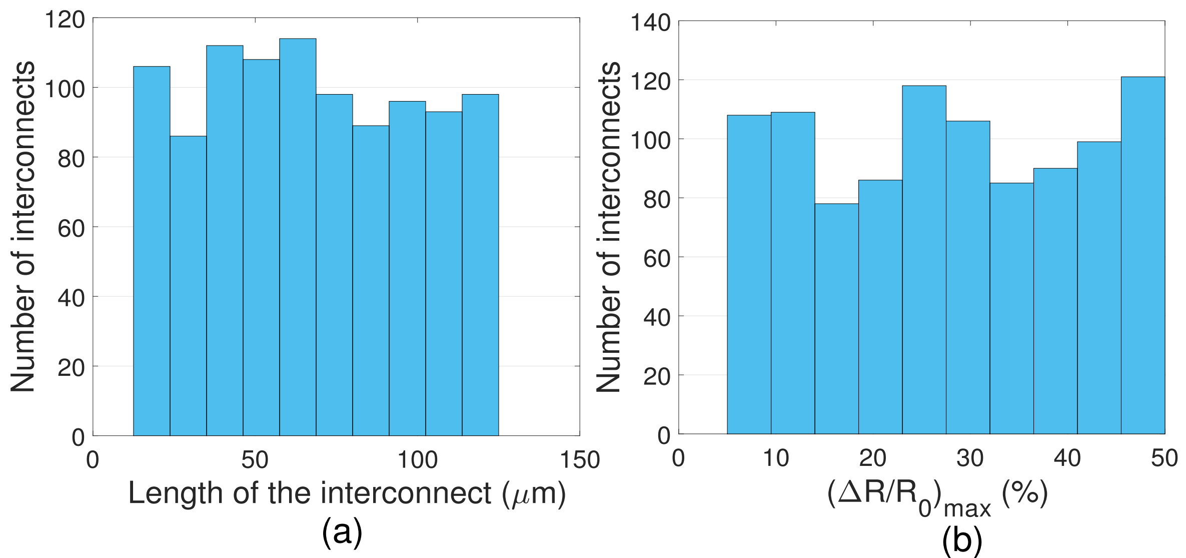

Figure 4.14 – Histograms from parameters of the 1000 lines. (a) Length. (b) $(\Delta R/R_0)_{max}$.

Table 4.2 – Normalized values for current and width of the six blocks.

Parameters	B1	B2	B3	B4	B5	B6
Current	I	$1.5I$	$1.75I$	$4I$	$1.25I$	$2I$
Width	w_{min}	$1.5w_{\text{min}}$	$1.75w_{\text{min}}$	$4w_{\text{min}}$	$1.25w_{\text{min}}$	$2w_{\text{min}}$

All the blocks have the lines operating under the maximum current density informed by the foundry [171]. The lines of B4 have a width 4 times larger than the minimum width (w_{min}) of the technology, resulting in a current of $4I$. In turn, B1, with the lowest power dissipation, have the lines with w_{min} and under a current of I. For Metal 1 lines from GPDK 45 nm technology, with the maximum current density of 2 mA/μm and the w_{min} of 65 nm, I = 130 μA. The normalization of the width and the current is considered for the other blocks, as shown in Table 4.2.

Figure 4.15 shows the ΔT_{PT} of the blocks B1 to B6 based on (2.8), considering the power dissipated in each block, the metal and via volume fraction of 40% and 6%, respectively, k_i of 1.4 W/m·K and k_m of 401 W/m·K, and the via and metal layers from 45 nm technology, described in Table 4.3 [171]. The ΔT_{PT} of the Block B4 in the Metal 1 is 57 K, as the block operates under the highest power dissipation, while the other blocks have a lower ΔT_{PT}. Here, we use the Metal 1 lines to evaluate the critical blocks, and we consider that in a block the Metal 1 lines operates with the same ΔT_{PT}.

Table 4.3 – Thickness of the lines and via layers from GPDK 45 nm.

Layer	Metal thickness (nm)	Via thickness (nm)
1-8	150	150
9-10	1000	1000
11	1400	-

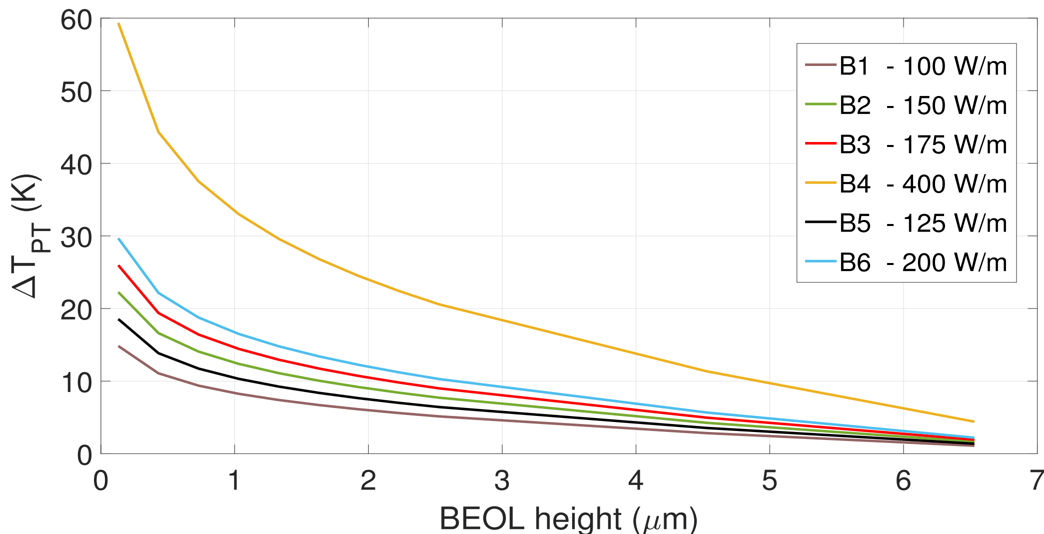

Figure 4.15 – ΔT_{PT} in the layers from the blocks B1 to B6.

The comparison of the estimated temperature (T), obtained from the sum of the reference temperature and the ΔT_{PT}, with the maximum temperature (T_{max}) in the lines, gives the probability of a block being critical. T_{max} is given by (3.7), which ρ_b is 0.6 $\mu\Omega$m, I and w are from the Table (4.2), Δt is 2 years, A_b is given by (2.12), the reference temperature is 300 K, the length and the $(\Delta R/R_0)_{max}$ are from Figure 4.14.

Figure 4.16 shows the T and the T_{max} of the Metal 1 lines from B1 to B6. Note that all the lines from B4 have the T above the T_{max}, indicating that B4 is probably the most critical block. Table 4.4 presents the number of critical lines susceptible to EM failure and the probability of the blocks to failure, obtained from comparison of the temperatures. B1 is the block less susceptible to failure with 16 critical lines, equivalent to a 1.6% of the lines from the block, and 0.87% of the critical lines from the chip. In

Table 4.4 – EM evaluation of the blocks B1 to B6.

Block	T (K)	T_{max} (K)	Critical lines	Critical lines (%)	Critical block (%)
B1	309	304 - 344	16	1.6	0.87
B2	316	303 - 341	67	6.7	3.64
B3	321	302 - 339	254	25.4	13.9
B4	350	298 - 334	1000	100	54.7
B5	312	302 - 342	37	3.7	2.14
B6	324	301 - 338	453	45.3	24.79

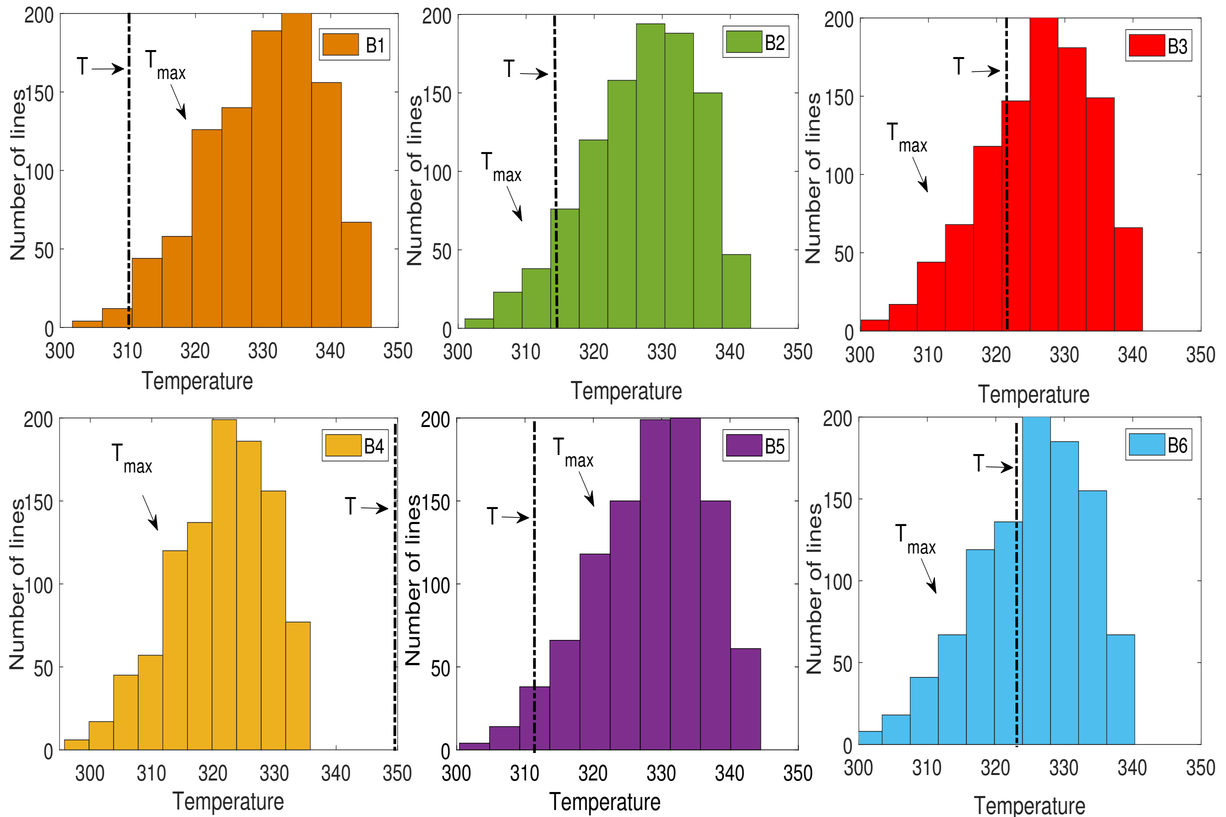

Figure 4.16 – T and T_{max} of the Metal 1 lines from B1 to B6.

turn, B4 is the most critical block in terms of temperature, with 54.7% of the critical lines of the chip.

This methodology allows identifying the blocks potentially critical due to EM based on the temperature. This allows to the designer strategically position the blocks in the chip avoiding the parts more sensible to those that dissipate more power. For example, positioning B1 near B2 can increase the temperature in B1 to 316 K and increase the critical lines in B1 to 77. In turn, positioning B1 near B6 increases the number of critical lines in B1 to 314. Notice that the elevated temperature in B4 indicates the need to maintain a distance to the other blocks. In this way, the concept of electromigration is expanded to evaluate critical blocks as a function of the temperature.

5 Electromigration Evaluation Tool

In this chapter the EM computational tool is described, explaining the procedures to identify the critical lines and to estimate the width of the lines. The tool is applied to evaluate the interconnects of an operational amplifier (Opamp).

5.1 Tool Description

The proposed tool has four main routines named: input parameters, EM evaluation, critical lines report and the dimension of the lines. The input parameters routine includes the resistivity of the interconnects and barrier, the minimum width of the lines, the thickness of the via and metal layers, the activation energy, the diffusivity of the metal and all the parameters related to EM. The width, the length, the resistance, the metal layer, and the current density through the lines are obtained from the EDA tool.

The EM evaluation routine uses the traditional and the resistance change criterion to evaluate the lines. According to the traditional criterion, the critical lines present a current density or the Blech Product above the threshold. All the lines can be evaluated based on the resistance change, where the performance of the circuit is evaluated with the degradation of the lines. Nevertheless, to reduce the time of the analysis, the traditional criteria can filter the lines prone to failure. For a margin of 20%, i.e., the lines with a current density of 80% of the maximum allowed one or with the Blech product of 80% of the critical threshold, the lines are classified as susceptible to failure and evaluated with the resistance change criterion.

The maximum resistance of each interconnect is simulated with Cadence, where the equivalent resistance of the interconnect is incremented until it reaches the value that degrades the circuit performance, violating the specifications. This critical resistance can be used in two ways to evaluate the critical lines. The first approach evaluates the maximum resistance that a line can degrade without affecting significantly the circuit performance and then compare it with the critical resistance determined above. The second approach calculates the line resistance increase due to EM, according to the expected circuit lifetime, and then simulates if the inclusion of the EM seriously degrades the circuit performance.

The time of the first line to reach a critical resistance determines the lifetime of the circuit from the EM point of view. For a circuit with more than two performance metrics, the lifetime is based on the parameter that degrades first. As the circuit lifetime

is affected by the temperature of the lines, the temperature is estimated as described in chapter 4.

The volume fraction of the metal is the percentual of interconnects occupying a metal layer of the chip. As the layers have a different number of interconnects, the volume fraction of the layers is generally different. In turn, the via fraction volume is the percentual occupied by the vias in a via layer. The increase in the number of vias and the width of the metal lines allows the heat to flow more easily to the global layers of metal and reduces the temperature in the local layers. As the vias occupy a smaller area than the metal lines, and the enlargement of the lines can affect the minimum distance to the adjacent lines, it is easier to insert more vias to change the thermal conductivity of the BEOL.

The critical lines from a circuit are shown in the EM report, where the critical lines are classified as 1 and the non-critical lines classified as 0, for the three EM criteria. The report shows the number of lines propense to EM failure, filtered with the maximum current density and the Blech product. The critical and non-critical lines are also reported in a Venn Diagram [201], which shows the number of critical and non-critical lines according to the EM criteria.

The oversized and undersized lines are informed, where the oversized lines are indicated by 1 and have a width larger than the minimum of the technology without giving an advantage in terms of EM. The undersized lines are indicated with the number 2 and have a dimension smaller than the informed by the three criteria, increasing the risk to the circuit failure due to EM. The suggested width for the lines based on the EM criteria is also reported.

As the width of the lines is typically designed based only on the maximum current density criterion, generally the lines are classified as oversized. Even through the correction of the lines changes the metal volume fraction, the change is not expressive to affect the temperature on the BEOL.

5.2 Tool Application for a Line of an Operational Amplifier

Figure 5.1 shows the supply voltage interconnect named Vdd of an operational amplifier evaluated with the proposed tool. The circuit designed in GPDK 45 nm technology has the Vdd line composed of 70 paths made in Metal 1, Metal 2 and Metal 3 layers, where the metal thickness is 150 nm and the maximum current density (j_{max}) is 2 mA/μm. The minimum width for Metal 1 is 60 nm, while for Metal 2 and Metal 3 it is 80 nm [171].

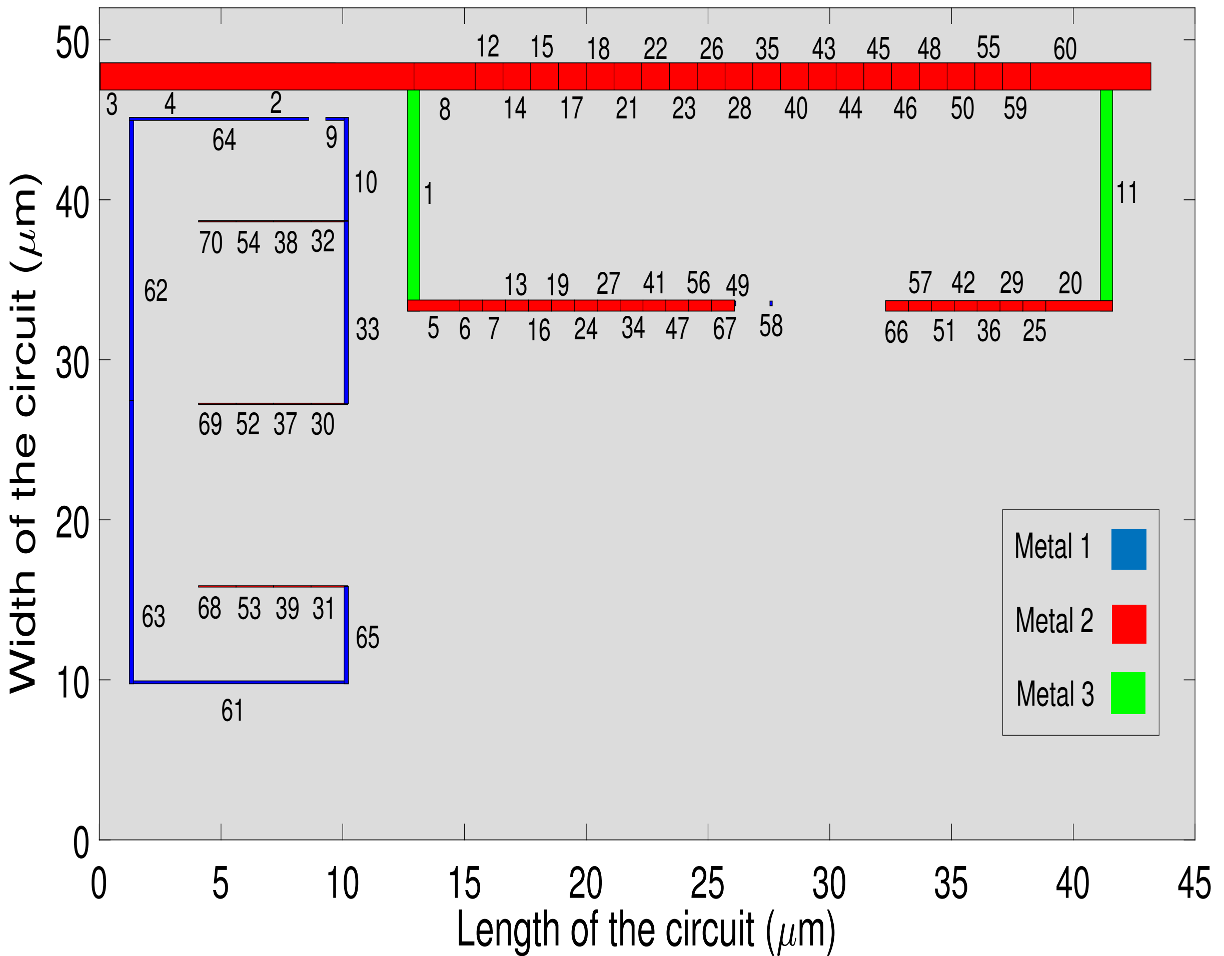

Figure 5.1 – Vdd line of an operational amplifier designed with three metal layers. The interconnect paths are enumerated from 1 to 70.

Tables 5.1 and 5.2 show the EDA data from the Vdd paths enumerated from 1 to 70. The paths 1 to 5 operate under a current density (j) above the maximum (j_{max}). Note that some paths designed with a width of 1.7 μm operate with a current density below 60% of j_{max}, as an example the paths 59 and 60, indicating possibly two oversized lines. To evaluate the Vdd line with the Blech product and $\Delta R/R_0$ criteria, we use the more resistive metal segment including each path (L_{EM}), which varies from 2.15 μm to 123.1 μm. The resistance (R) of the paths varies between 0.04 Ω to 6.93 Ω.

Table 5.3 shows the typical values of the parameters to estimate the temperature change on the BEOL and the resistance change in a metal line of the 45 nm technology. Table 5.4 and Table 5.5 show the volume fractions of the Metal 1 to Metal 3 (ϕ_{int}) and the vias 1-2 and 2-3 (ϕ_{via}) layers, obtained with the areas of the vias (A_{via}), metals (A_{int}) and circuit, which measures 2250 μm^2. The aspect ratio a_r is the average ratio of the length and the thickness of the lines in each layer of the circuit. The parameter

a_r (explained in Appendix F) is used to obtain the effective thermal conductivity of the metal (k_{eff}^{int}) and via (k_{eff}^{via}) layers, which in turn is used to calculate the effective thermal conductivity of the BEOL (k_{eff}^{beol}).

Table 5.1 – EDA data of the Vdd paths enumerated from 1 to 40.

Path	Layer	j/j_{max}	W (μm)	L (μm)	L_{EM} (μm)	R (Ω)	I (mA)
1	Metal 3	1.44	0.50	14.0	15.5	1.69	1.44
2	Metal 2	1.23	1.70	4.82	43.1	0.34	4.18
3	Metal 2	1.23	1.70	4.07	43.1	0.14	4.18
4	Metal 2	1.12	1.70	3.98	43.1	0.13	3.80
5	Metal 2	1.04	0.69	1.91	13.7	0.16	1.44
6	Metal 2	0.97	0.69	0.94	13.7	0.08	1.34
7	Metal 2	0.90	0.69	0.94	13.7	0.08	1.25
8	Metal 2	0.69	1.70	2.51	43.1	0.08	2.36
9	Metal 1	0.92	0.18	0.84	123.1	0.32	0.33
10	Metal 1	0.92	0.18	6.39	123.1	2.52	0.33
11	Metal 3	0.91	0.50	14.1	15.4	1.70	0.91
12	Metal 2	0.69	1.70	1.14	43.1	0.04	2.34
13	Metal 2	0.84	0.69	0.94	13.7	0.08	1.16
14	Metal 2	0.68	1.70	1.14	43.1	0.04	2.31
15	Metal 2	0.66	1.70	1.14	43.1	0.04	2.27
16	Metal 2	0.77	0.69	0.94	13.7	0.08	1.06
17	Metal 2	0.65	1.70	1.14	43.1	0.04	2.23
18	Metal 2	0.64	1.70	1.14	43.1	0.04	2.20
19	Metal 2	0.70	0.69	0.94	13.7	0.08	0.97
20	Metal 2	0.70	0.65	2.50	14.3	0.23	0.91
21	Metal 2	0.63	1.70	1.14	43.1	0.04	2.16
22	Metal 2	0.62	1.70	1.14	43.1	0.04	2.12
23	Metal 2	0.61	1.70	1.14	43.1	0.05	2.08
24	Metal 2	0.63	0.69	0.94	13.7	0.08	0.87
25	Metal 2	0.62	0.65	0.94	14.3	0.08	0.81
26	Metal 2	0.57	1.70	1.14	43.1	0.04	1.95
27	Metal 2	0.56	0.69	0.94	13.7	0.08	0.78
28	Metal 2	0.51	1.70	1.14	43.1	0.04	1.73
29	Metal 2	0.55	0.65	0.94	14.3	0.08	0.72
30	Metal 2	0.55	0.08	1.45	8.31	0.88	0.08
31	Metal 2	0.55	0.08	1.45	8.31	0.88	0.08
32	Metal 2	0.55	0.08	1.45	8.31	0.92	0.08
33	Metal 1	0.53	0.18	11.4	123.1	4.49	0.19
34	Metal 2	0.50	0.69	0.94	13.7	0.08	0.69
35	Metal 2	0.44	1.70	1.14	43.1	0.04	1.51
36	Metal 2	0.48	0.65	0.94	14.3	0.08	0.62
37	Metal 2	0.44	0.08	1.54	8.31	0.95	0.07
38	Metal 2	0.44	0.08	1.54	8.31	0.95	0.07
39	Metal 2	0.44	0.08	1.54	8.31	0.95	0.07
40	Metal 2	0.38	1.70	1.14	43.1	0.04	1.30

Table 5.2 – EDA data of the Vdd paths enumerated from 41 to 70.

Path	Layer	j/j_{max}	W (μm)	L (μm)	L$_{EM}$ (μm)	R (Ω)	I (mA)
41	Metal 2	0.43	0.69	0.94	13.7	0.08	0.59
42	Metal 2	0.41	0.65	0.94	14.3	0.08	0.53
43	Metal 2	0.34	1.70	1.14	43.1	0.04	1.17
44	Metal 2	0.33	1.70	1.14	43.1	0.04	1.12
45	Metal 2	0.32	1.70	1.14	43.1	0.04	1.10
46	Metal 2	0.31	1.70	1.14	43.1	0.04	1.07
47	Metal 2	0.36	0.69	0.94	13.7	0.08	0.50
48	Metal 2	0.30	1.70	1.14	43.1	0.04	1.03
49	Metal 1	0.35	0.10	0.29	2.15	0.18	0.07
50	Metal 2	0.29	1.70	1.14	43.1	0.04	0.99
51	Metal 2	0.33	0.65	0.94	14.3	0.08	0.44
52	Metal 2	0.33	0.08	1.54	8.31	0.95	0.05
53	Metal 2	0.33	0.08	1.54	8.31	0.95	0.05
54	Metal 2	0.33	0.08	1.54	8.31	0.95	0.05
55	Metal 2	0.28	1.70	1.14	43.1	0.04	0.96
56	Metal 2	0.29	0.69	0.94	13.7	0.08	0.40
57	Metal 2	0.26	0.65	0.94	14.3	0.08	0.34
58	Metal 1	0.28	0.10	0.29	2.15	0.18	0.05
59	Metal 2	0.27	1.70	1.14	43.1	0.04	0.92
60	Metal 2	0.26	1.70	3.13	43.1	0.11	0.90
61	Metal 1	0.25	0.18	8.82	123.1	3.45	0.09
62	Metal 1	0.25	0.18	17.6	123.1	6.93	0.09
63	Metal 1	0.25	0.18	17.6	123.1	6.93	0.09
64	Metal 1	0.25	0.18	7.27	123.1	2.85	0.09
65	Metal 1	0.25	0.18	5.99	123.1	2.35	0.09
66	Metal 2	0.19	0.65	0.94	14.3	0.08	0.25
67	Metal 2	0.22	0.69	0.94	13.7	0.08	0.31
68	Metal 2	0.22	0.08	1.54	8.31	0.95	0.03
69	Metal 2	0.22	0.08	1.54	8.31	0.95	0.03
70	Metal 2	0.22	0.08	1.54	8.31	0.95	0.03

Table 5.3 – Parameters to estimate the resistance and the temperature change.

Parameter	Symbol	Value	Unit	Ref
Width of the barrier	w_b	3.0	nm	[162]
TaN barrier resistivity	ρ_b	6x10^{-7}	Ω·m	[202]
Cu diffusion pre-factor	D_0	3x10^{-5}	m^2/s	[128]
Thermal conductivity of the metal	k_m	401	W/m·K	[135]
Thermal conductivity of the insulator	k_i	1.4	W/m·K	[136]
Activation energy	E_a	1.0	eV	[165]

Note that the Metal 2 has the highest volume fraction of 19.7% and the k_{eff}^{int} of 2.08 W/m·K. Metal 3 has a lower fraction volume of 4.4% and the k_{eff}^{int} of 1.52 W/m·K. In turn, the via 1-2 placed between the Metal 1 and Metal 2 layers have the k_{eff}^{via} of 2.9 W/m·K, higher than the k_{eff}^{via} of 2.5 W/m·K from via 2-3 layer.

Table 5.4 – Parameters of the metal layers to calculate k_{eff}^{int}.

Metal layer	ϕ_{int} (%)	k_{eff}^{int} (W/m·K)	a_r (μm)
Metal 1	8.3	1.65	22.3
Metal 2	19.7	2.08	12.3
Metal 3	4.4	1.52	24.5

Table 5.5 – Parameters of the via layers to calculate k_{eff}^{via}.

Via layer	A_{via} (μm^2)	ϕ_{via} (%)	k_{eff}^{via} (W/m·K)
Via12	8.64	0.38	2.9
Via23	6.48	0.28	2.5

Table 5.6 – Temperature of the metal layers.

Metal layer	ΔT_{PT} (K)	T (K)
Metal 1	38.4	338.4
Metal 2	24.2	324.2
Metal 3	14.8	314.8

From (2.9) the k_{eff}^{beol} is estimated in 2 W/m·K, where the BEOL thickness of 750 nm is obtained from the sum of the thicknesses of the 3 metal layers and 2 via layers. From (2.8), the power dissipated in the FEOL increases the temperature to that shown in Table 5.6. As expected, the Metal 1 layer temperature is larger than that from Metal 2 and Metal 3, since it is closer to the FEOL.

Tables 5.7 and 5.8 show the evaluation of the paths as a critical and non-critical for the three criteria: maximum current density (C.j), maximum resistance change (C.$\Delta R/R_0$), and the Blech product (C.jL). The paths classified as 1 are critical and the paths classified as 0 are non-critical. The path 1 is critical for C.j, with a current density of 2.98 mA/μm, above the maximum of 2 mA/μm. Nonetheless, path 1 is non-critical for C.jL, since the line presents the Blech product of 0.29 A/μm, below the threshold for Cu lines of 0.37 A/μm [203].

The lines prone to failure (LPF) have current density or Blech product above the threshold [204]. Path 1 is classified as LPF since it has a current density above the maximum. The LPF lines are evaluated with the $\Delta R/R_0$ criterion that compares the resistance change of the line with the the maximum resistance change of 10%. For example, Table 5.7 shows that after 2 years operating in a workload of 50%, the resistance of the path 1 increases 8.18%, below the threshold of 10%.

The 5 paths critical to the C.j and the 17 paths critical to the C.jL result in 19 LPF paths. From the LPF paths, only the path 5 is critical to the C.$\Delta R/R_0$ criterion, indicating that the other 18 paths can suffer EM degradation and not damage seriously the performance of the Opamp. In turn, the 13 lines classified as a critical due to C.$\Delta R/R_0$

and not LPF can damage significantly the IC performance, even operating under a current density below the threshold. This analysis shows the importance of considering the impacts of the resistance change in the IC performance to evaluate the critical lines due to EM, being an important complement to the traditional criteria based on the current density.

Table 5.7 – Evaluation of the critical paths 1 to 40 with the EM criteria.

Path	j (mA/μm)	jL (A/μm)	$\Delta R/R_0$ (%)	C.j	C.jL	LPF	C.$\Delta R/R_0$
1	2.89	0.29	8.18	1	0	1	0
2	2.46	0.70	9.69	1	1	1	0
3	2.46	0.70	9.69	1	1	1	0
4	2.24	0.64	8.81	1	1	1	0
5	2.09	0.19	21.20	1	0	1	1
6	1.95	0.17	19.82	0	0	0	1
7	1.81	0.16	18.44	0	0	0	1
8	1.39	0.40	5.48	0	1	1	0
9	1.85	1.51	4.80	0	1	1	0
10	1.85	1.51	4.80	0	1	1	0
11	1.82	0.18	5.16	0	0	0	0
12	1.38	0.39	5.44	0	1	1	0
13	1.68	0.15	17.05	0	0	0	1
14	1.36	0.39	5.35	0	1	1	0
15	1.33	0.38	5.27	0	1	1	0
16	1.54	0.14	15.67	0	0	0	1
17	1.31	0.37	5.18	0	1	1	0
18	1.29	0.37	5.10	0	1	1	0
19	1.41	0.12	14.28	0	0	0	1
20	1.40	0.13	13.36	0	0	0	1
21	1.27	0.36	5.01	0	0	0	0
22	1.25	0.36	4.92	0	0	0	0
23	1.22	0.35	4.83	0	0	0	0
24	1.27	0.11	12.90	0	0	0	1
25	1.25	0.12	11.97	0	0	0	1
26	1.15	0.33	4.53	0	0	0	0
27	1.13	0.10	11.52	0	0	0	1
28	1.02	0.29	4.02	0	0	0	0
29	1.11	0.10	10.59	0	0	0	1
30	1.11	0.06	5.55	0	0	0	0
31	1.11	0.06	5.55	0	0	0	0
32	1.11	0.06	5.55	0	0	0	0
33	1.06	0.87	2.76	0	1	1	0
34	1.00	0.09	10.14	0	0	0	1
35	0.89	0.25	3.51	0	0	0	0
36	0.96	0.09	9.21	0	0	0	0
37	0.88	0.04	4.40	0	0	0	0
38	0.88	0.04	4.40	0	0	0	0
39	0.88	0.04	4.40	0	0	0	0
40	0.76	0.22	3.01	0	0	0	0

Table 5.8 – Evaluation of the critical paths 41 to 70 with the EM criteria.

Path	j (mA/μm)	jL (A/μm)	$\Delta R/R_0$ (%)	C.j	C.jL	LPF	C.$\Delta R/R_0$
41	0.86	0.07	8.75	0	0	0	0
42	0.82	0.07	7.83	0	0	0	0
43	0.68	0.19	2.71	0	0	0	0
44	0.66	0.19	2.61	0	0	0	0
45	0.65	0.18	2.56	0	0	0	0
46	0.63	0.18	2.48	0	0	0	0
47	0.72	0.06	7.37	0	0	0	0
48	0.60	0.17	2.39	0	0	0	0
49	0.70	0.01	69.39	0	0	0	1
50	0.58	0.16	2.31	0	0	0	0
51	0.67	0.06	6.45	0	0	0	0
52	0.66	0.03	3.32	0	0	0	0
53	0.66	0.03	3.32	0	0	0	0
54	0.66	0.03	3.32	0	0	0	0
55	0.56	0.16	2.22	0	0	0	0
56	0.59	0.05	5.98	0	0	0	0
57	0.53	0.05	5.07	0	0	0	0
58	0.56	0.01	56.26	0	0	0	1
59	0.54	0.15	2.14	0	0	0	0
60	0.53	0.15	2.10	0	0	0	0
61	0.50	0.41	1.30	0	1	1	0
62	0.50	0.41	1.30	0	1	1	0
63	0.50	0.41	1.30	0	1	1	0
64	0.50	0.41	1.30	0	1	1	0
65	0.50	0.41	1.30	0	1	1	0
66	0.38	0.03	3.68	0	0	0	0
67	0.45	0.04	4.60	0	0	0	0
68	0.44	0.02	2.23	0	0	0	0
69	0.44	0.02	2.23	0	0	0	0
70	0.44	0.02	2.23	0	0	0	0

Tables 5.9 and 5.10 show the calculated width of the paths for the maximum current density (W_j) given by (3.1), the Blech product (W_{jL}) given by (3.2) and the maximum resistance change (W_r) given by (3.6). The suggested width (W_s) depends on the LPF index. If the line is classified as LPF, this width is chosen as the maximum value calculated by the three criteria. If the line is not LPF, the width is the maximum between the two traditional criteria. The minimum width of Metal 1 is 0.06 μm and of Metal 2 and Metal 3 is 0.08 μm, according to the technology rules [171].

The lines which are wider than W_s are classified as oversized and indicated by the number "1" in the last column (size evaluation). The undersized lines are narrower than W_s and are indicated by the number "2". The lines indicated with "0" have adequate sizes, i.e. their widths are larger than W_s by 5% at most. Although the Vdd line have 47

oversized paths, some of the 15 undersized paths operate under a higher current density, which reduces the expected lifetime of the circuit.

Table 5.9 – Dimensions of the paths 1 to 40 of the Vdd interconnect.

Path	W_j (μm)	W_{jL} (μm)	W_r (μm)	W_s (μm)	W (μm)	Size evaluation
1	0.72	0.40	0.31	0.72	0.5	2
2	2.09	3.25	0.34	3.25	1.7	2
3	2.09	3.25	0.34	3.25	1.7	2
4	1.90	2.96	0.34	2.96	1.7	2
5	0.72	0.35	0.34	0.72	0.69	0
6	0.67	0.33	0.34	0.67	0.69	0
7	0.62	0.31	0.34	0.62	0.69	1
8	1.18	1.84	0.32	1.84	1.7	2
9	0.16	0.73	0.31	0.73	0.18	2
10	0.16	0.73	0.31	0.73	0.18	2
11	0.45	0.25	0.31	0.45	0.5	1
12	1.17	1.82	0.32	1.82	1.7	2
13	0.58	0.28	0.34	0.58	0.69	1
14	1.15	1.80	0.32	1.80	1.7	2
15	1.13	1.77	0.32	1.77	1.7	0
16	0.53	0.26	0.33	0.53	0.69	1
17	1.12	1.74	0.32	1.74	1.7	0
18	1.10	1.71	0.32	1.71	1.7	0
19	0.48	0.24	0.33	0.48	0.69	1
20	0.45	0.23	0.33	0.45	0.65	1
21	1.08	1.68	0.32	1.68	1.7	0
22	1.06	1.65	0.32	1.65	1.7	0
23	1.04	1.62	0.32	1.62	1.7	0
24	0.43	0.21	0.33	0.43	0.69	1
25	0.40	0.21	0.32	0.40	0.65	1
26	0.97	1.52	0.32	1.52	1.7	1
27	0.39	0.19	0.32	0.39	0.69	1
28	0.86	1.35	0.32	1.35	1.7	1
29	0.36	0.18	0.32	0.36	0.65	1
30	0.04	0.01	0.31	0.06	0.08	1
31	0.04	0.01	0.31	0.06	0.08	1
32	0.04	0.01	0.31	0.06	0.08	1
33	0.09	0.42	0.30	0.42	0.18	2
34	0.34	0.17	0.32	0.34	0.69	1
35	0.75	1.18	0.32	1.18	1.7	1
36	0.31	0.16	0.32	0.31	0.65	1
37	0.03	0.01	0.30	0.06	0.08	1
38	0.03	0.01	0.30	0.06	0.08	1
39	0.03	0.01	0.30	0.06	0.08	1
40	0.65	1.01	0.31	1.01	1.7	1

Table 5.10 – Dimensions of the paths 41 to 70 of the Vdd interconnect.

Path	W_j (μm)	W_{jL} (μm)	W_r (μm)	W_s (μm)	W (μm)	Size evaluation
41	0.29	0.14	0.32	0.29	0.69	1
42	0.26	0.13	0.32	0.26	0.65	1
43	0.58	0.91	0.31	0.91	1.7	1
44	0.56	0.87	0.31	0.87	1.7	1
45	0.55	0.86	0.31	0.86	1.7	1
46	0.53	0.83	0.31	0.83	1.7	1
47	0.25	0.12	0.32	0.25	0.69	1
48	0.51	0.80	0.31	0.80	1.7	1
49	0.03	0.01	0.36	0.06	0.1	1
50	0.49	0.77	0.31	0.77	1.7	1
51	0.22	0.11	0.31	0.22	0.65	1
52	0.02	0.01	0.30	0.06	0.08	1
53	0.02	0.01	0.30	0.06	0.08	1
54	0.02	0.01	0.30	0.06	0.08	1
55	0.48	0.74	0.31	0.74	1.7	1
56	0.20	0.10	0.31	0.20	0.69	1
57	0.17	0.08	0.31	0.17	0.65	1
58	0.02	0.01	0.35	0.06	0.1	1
59	0.46	0.72	0.31	0.72	1.7	1
60	0.45	0.70	0.31	0.70	1.7	1
61	0.04	0.20	0.30	0.20	0.18	2
62	0.04	0.20	0.30	0.20	0.18	2
63	0.04	0.20	0.30	0.20	0.18	2
64	0.04	0.20	0.30	0.20	0.18	2
65	0.04	0.20	0.30	0.20	0.18	2
66	0.12	0.06	0.31	0.12	0.65	1
67	0.15	0.07	0.31	0.15	0.69	1
68	0.01	0.01	0.30	0.06	0.08	1
69	0.01	0.01	0.30	0.06	0.08	1
70	0.01	0.01	0.30	0.06	0.08	1

Some paths have the dimensions significantly different from W_s. The paths 2 and 3, for example, are sized with widths of 1.7 μm. Nevertheless, these lines are undersized as the W_s is 3.25 μm, 91% larger than the designed width. In turn, the path 46 designed with 1.7 μm is 2 times wider than the suggested width.

The suggested dimensions for the paths of the Vdd line have a large variation. To maintain a pattern in the design, the paths from a ramification can be designed with the dimension of the widest path. For example, the paths 2,3 and 4, placed in a ramification, could be designed with the dimmension of 3.25 μm, even W_s of the path 4 being smaller. The same procedure to obtain the adequate width of the paths in a ramification can be extended to the other interconnects.

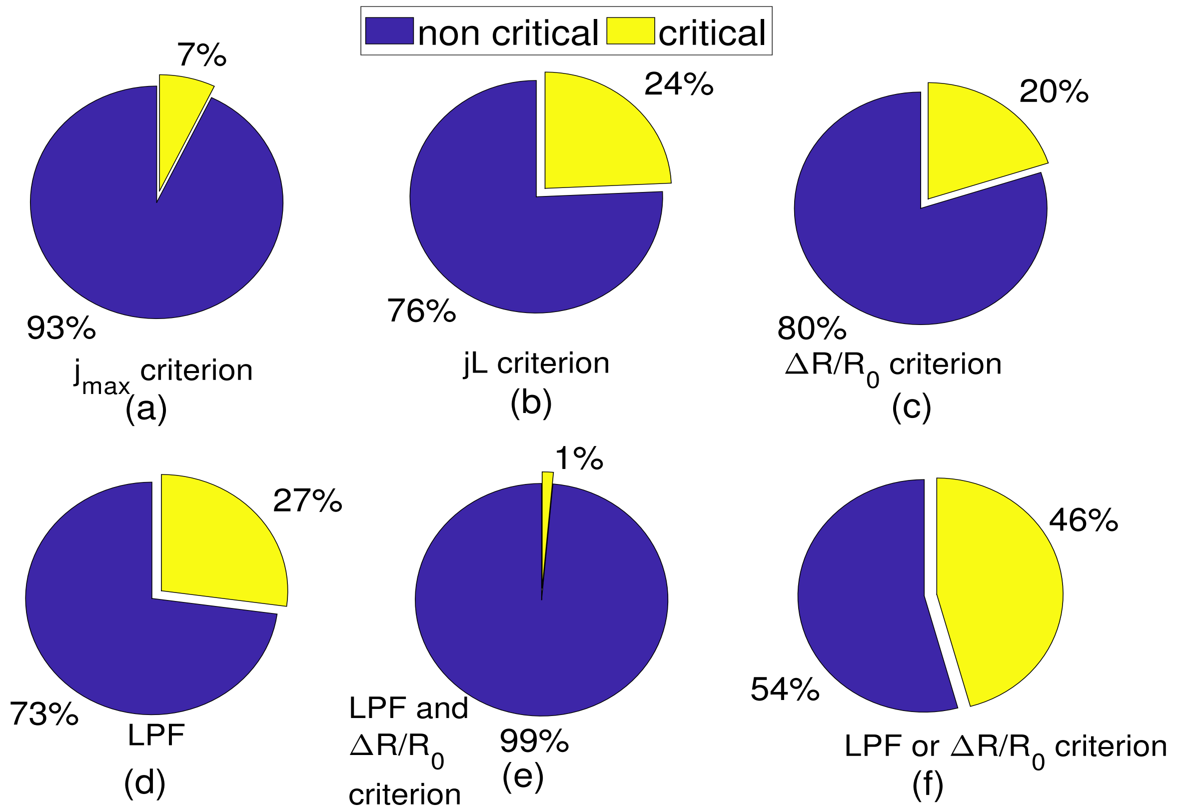

Figure 5.2 – Critical paths from the Vdd line according to: (a) j_{max}. (b) jL. (c) $\Delta R/R_0$. (d) LPF. (e) LPF and $\Delta R/R_0$. (f) LPF or $\Delta R/R_0$.

Figure 5.2 shows the critical and non-critical lines according to the maximum current density (a), the Blech product (b), the resistance change criterion (c), the LPF lines (d), the LPF lines and the resistance change criterion (e) and LPF lines or the resistance change criterion (f). Note that only 7% of the lines are classified as critical for the j_{max}. The number of critical lines increases to 27% when the Blech Product is included in the evaluation. Including the resistance change criterion, the number of critical lines becomes 46%. This clearly shows the importance to evaluate the lines not only based on the traditional criteria.

Observe that only 1% of the lines are classified as a LPF and critical for the resistance change criterion. This indicates that many of the 27% LPF paths do not represent a problem to the IC performance. In turn, from the 20% of the paths that can degrade the IC performance, only one path is classified as a critical due to the current density.

Figure 5.3 shows a Venn diagram with the number of critical interconnects. One path is critical only due j_{max}, 14 paths are critical only to the Blech product, and 13 paths are critical only to the resistance change criterion. Four lines are classified as critical for at least two criteria. In total (N), 38 lines are not critical, while 32 are critical (Nc) concerning EM.

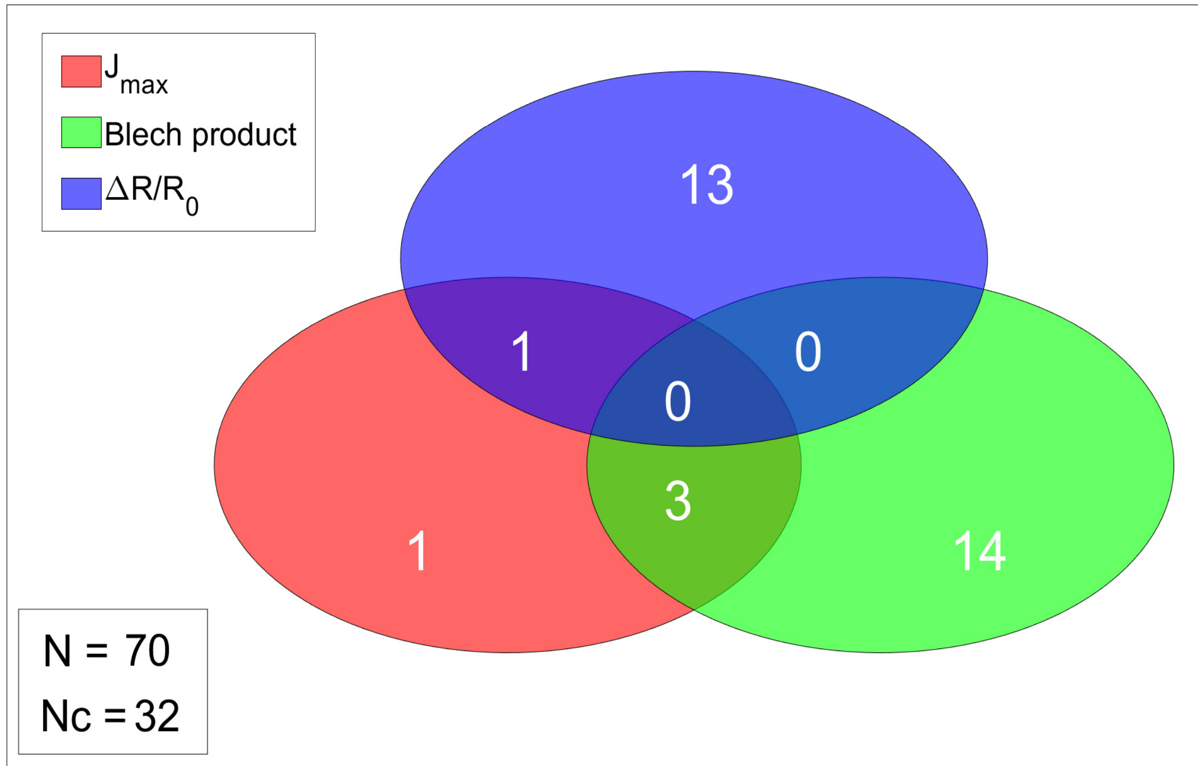

Figure 5.3 – Venn diagram with the critical paths of the Vdd line.

5.3 Tool Application for an Operational Amplifier

A similar analysis with the EM tool is extended to evaluate the other interconnects of the operational amplifier. Figure 5.4 illustrate the evaluated 177 paths designed in three metal layers. The EDA data input to the tool is described in the Appendix G.

Figure 5.5 shows that the critical paths due to j_{max} increases from 8% in (a) to 16% in (b), when considered only the Blech product, to 30% in (c), when considered only the resistance change and 47% when the paths are evaluated with all the three criteria in (f), corresponding to all the paths classified as a critical for at least one criterion. While 20% of the paths are LPF in (d), only 3% of the paths are LPF and also classified as critical with the resistance change criterion in (e). This analysis is summarized in Figure 5.6, which shows the corresponding Venn diagram with 53 critical paths for the resistance change, 29 critical paths for the Blech product, and 15 critical paths for the current density. The circuit have 83 critical (Nc) and 94 non-critical paths.

Figure 5.7 shows the suggested width and the as-designed width of 177 paths of the Opamp. The 27 paths which operate under the highest current densities have wider suggested widths than the as-designed widths, meaning that those paths are undersized. On the other hand, the 127 oversized paths, which operate under lower current densities, have the suggested width smaller than the as-designed widths.

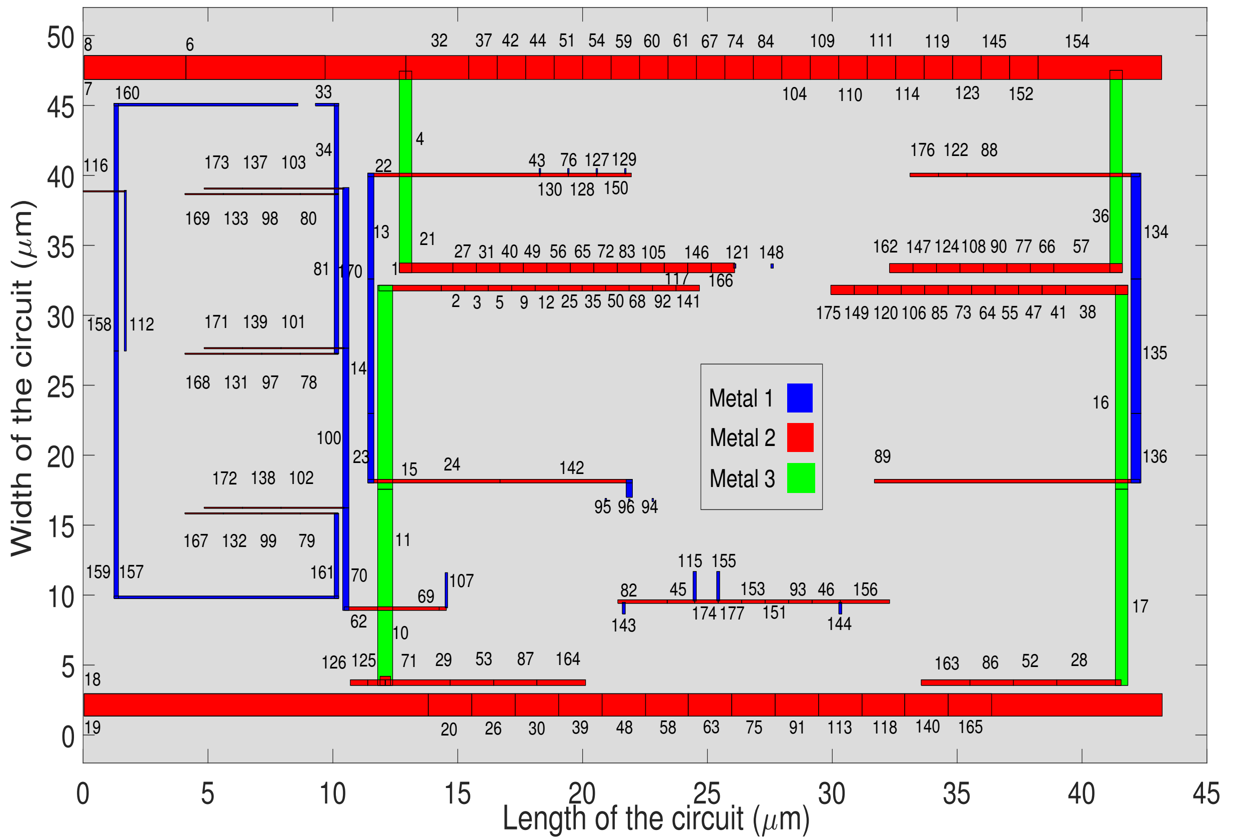

Figure 5.4 – Interconnects with 177 paths of the operational amplifier.

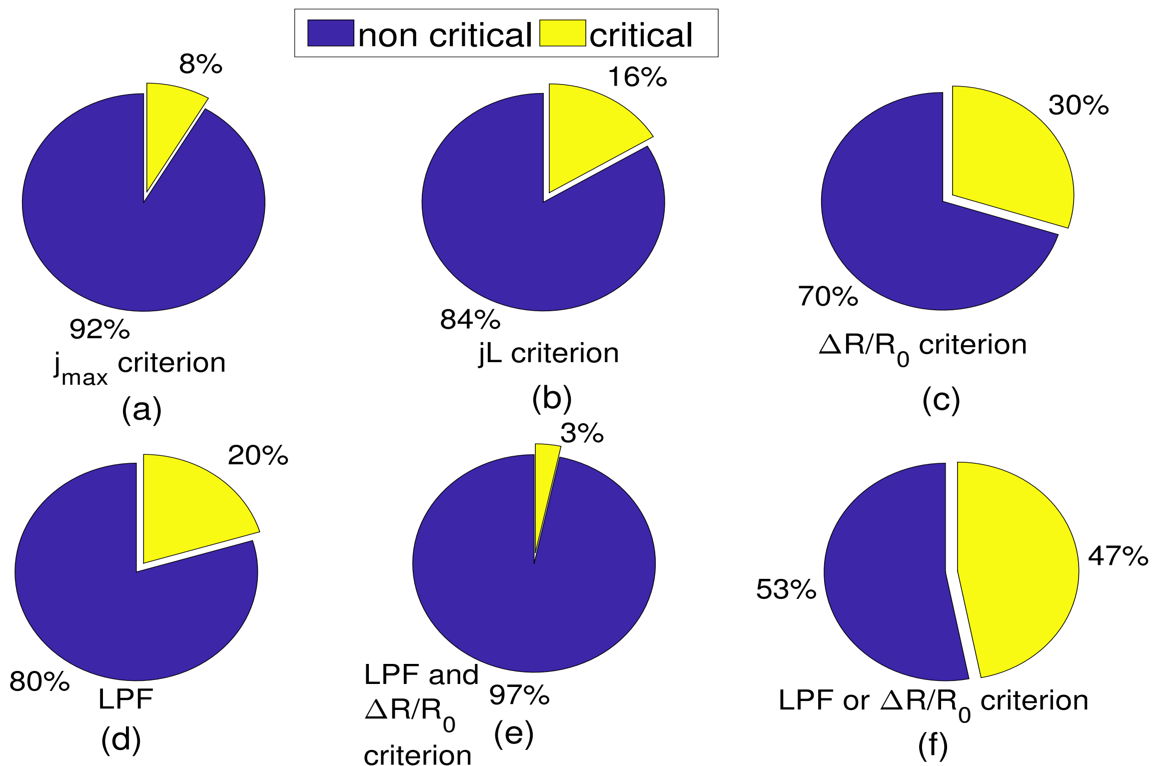

Figure 5.5 – Critical lines from the operational amplifier according to: (a) j_{max}. (b) jL. (c) $\Delta R/R_0$. (d) LPF. (e) LPF and $\Delta R/R_0$. (f) LPF or $\Delta R/R_0$.

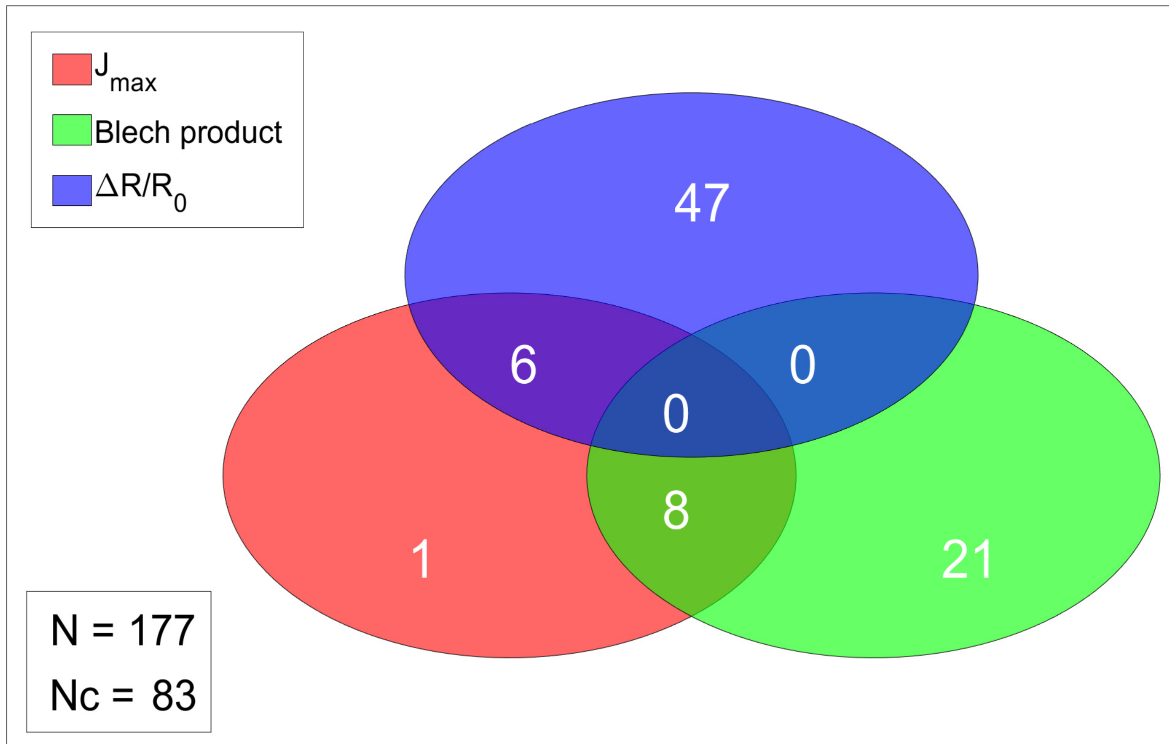

Figure 5.6 – Veen diagram with the critical paths of the operational amplifier.

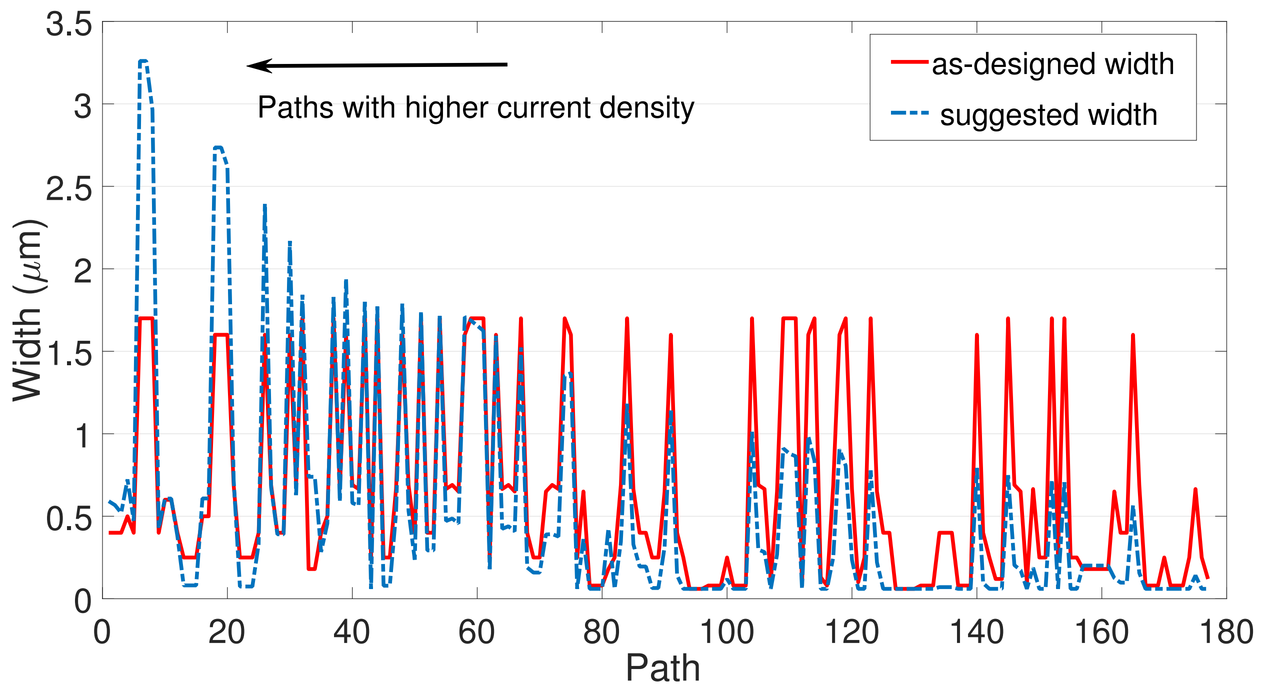

Figure 5.7 – Comparison of the width of the lines and the suggested width.

These results allow the designer to identify the critical paths or interconnects and obtain the suggested dimensions to fix the issues. The 127 oversized lines and the 30 undersized lines, result in a total of 157 lines that need to be resized to improve the reliability, without affecting the circuit performance.

6 Electromigration Impact on Circuits and Technology: Study Cases

In this chapter, we evaluate the performance of an operational amplifier, a bandgap voltage reference, and a ring oscillator circuit under EM. Finally, we compare the EM properties of several technologies including the state-of-the-art technology.

6.1 Evaluation of a Ring Oscillator under Electromigration

The EM methodology is applied to investigate the performance variation of a ring oscillator, considering that the source line VDD (Metal 1, $L = 125\ \mu$m, $w = 0.6\ \mu$m) undergo EM damage. The ring oscillator layout illustrated in Figure 6.1, is composed of 33 inverters, resulting in a frequency of 480 MHz for 300 K, 1.8 V and 100 fF of load for the testbench circuit, designed in XFAB 180 nm technology.

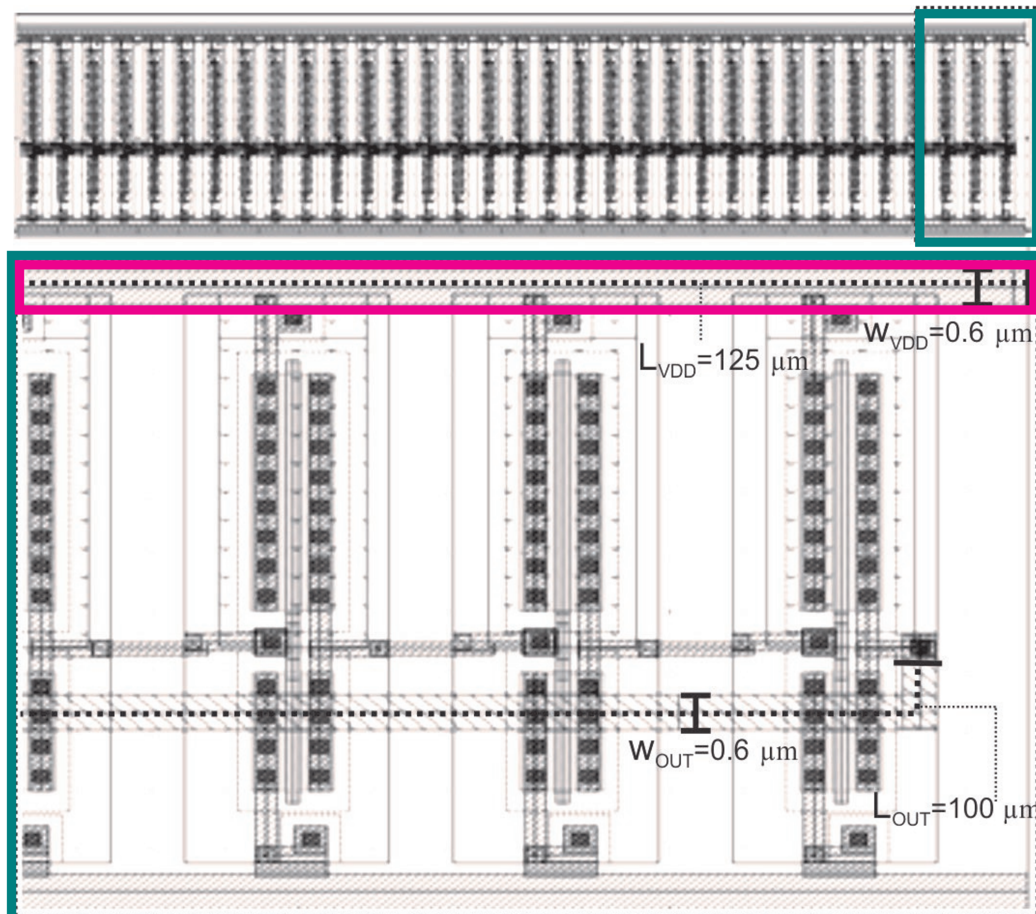

Figure 6.1 – Ring oscillator layout and detailed view showing the evaluated lines.

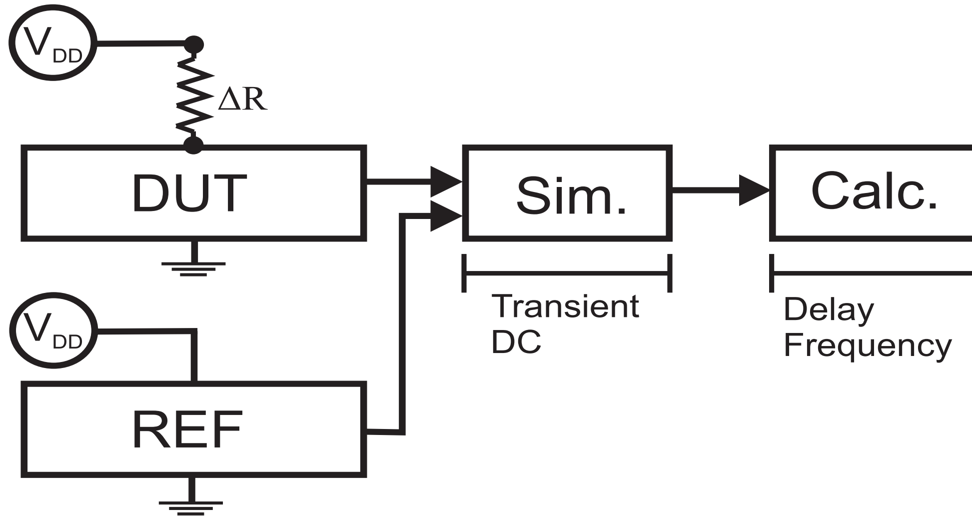

Figure 6.2 – Testbench for lines of a ring oscillator under EM.

Figure 6.2 shows the circuit testbench used to simulate the performance difference between layout extracted view without EM (REF) and with EM (DUT) in VDD line (varying ΔR). The obtained differences are used to calculate the delay and the frequency variation as a function of the $\Delta R/R_0$ ratio. A critical variation of $\Delta R/R_0 = 10\%$ is considered here.

A transient analysis is performed to simulate the delay variation of the ring oscillator as a function of the line resistance increase. The delay is the time difference between output signals from the DUT and the REF circuit when these signals cross the voltage of 0.9 V in the eleventh cycle, which avoids the transitory signals during the earlier cycles. As shown in Fig 6.3, the delay increases around 0.4% of one cycle period, when the VDD line is affected by the EM for $\Delta R/R_0 = 10\%$.

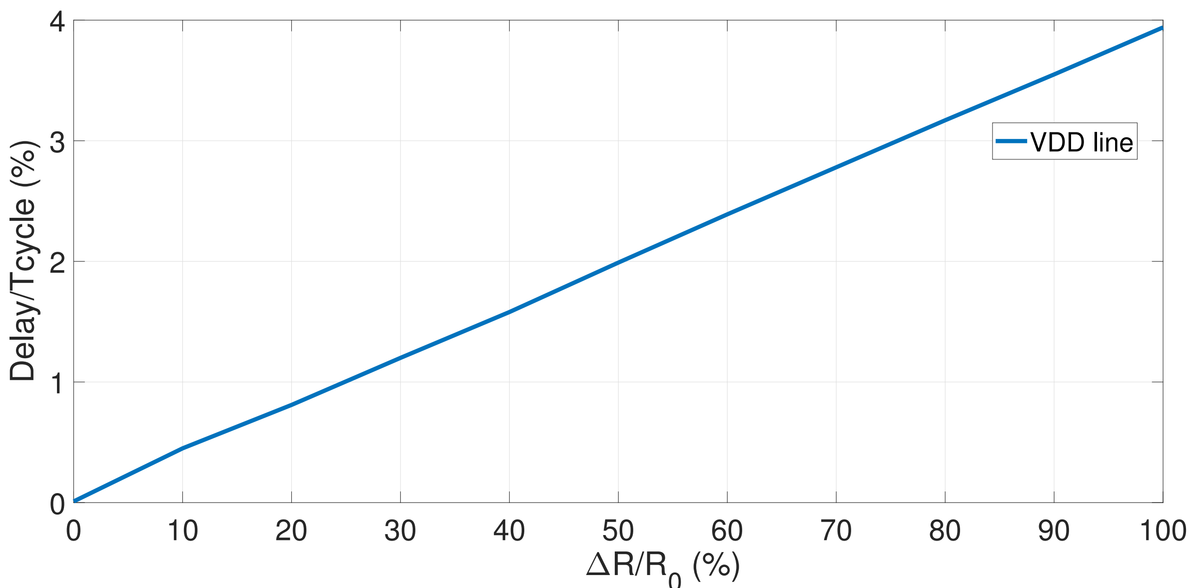

Figure 6.3 – Delay change of the oscillator as a function of the resistance increase.

Table 6.1 – Parameters based on the XFAB 180 nm technology used to calculate the $\Delta R/R_0$ ratio from (2.14).

Symbol	Name	Value	Unit	Ref
ρ_b	Ta resistivity	3x10^{-6}	Ω.m	[146]
D	Cu effective diffusivity	[1]6.7 x10^{-18}	m^2/s	[128]
ρ	Cu resistivity	24x10^{-9}	Ω.m	[162]
I	Current	2.3x10^{-4}	A	-
A_b	Ta barrier area	7.98x10^{-15}	m^2	[145]
w	Line width	0.6	μm	[145]
h	Line heigth	0.17	μm	[145]
E_a	Cu line activation energy	1.0	eV	[165]

[1]353 K.

Figure 6.4 shows that the frequency parameter is less significantly affected by the ΔR variation than the delay. The frequency varies 0.7% for $\Delta R/R_0 = 10\%$. Although $\Delta R/R_0$ variations around 10% can indicate a critical resistance variation, this ratio can assume larger values in some wires without disturbing the circuit performance. For example, the oscillator performance is simulated for the $\Delta R/R_0$ equals to 100% and 200% for VDD line shown in Table 6.2. Despite a substantial resistance increase in the VDD line, its impact on the circuit performance is small.

Table 6.2 – Oscillator performance for $\Delta R/R_0$ of 100% and 200% at 353 K.

Parameter	Delay/Tcycle (%)	$\Delta F/F_0$ (%)
$\Delta R/R_0 = 100\%$	4	0.78
$\Delta R/R_0 = 200\%$	8	1.56

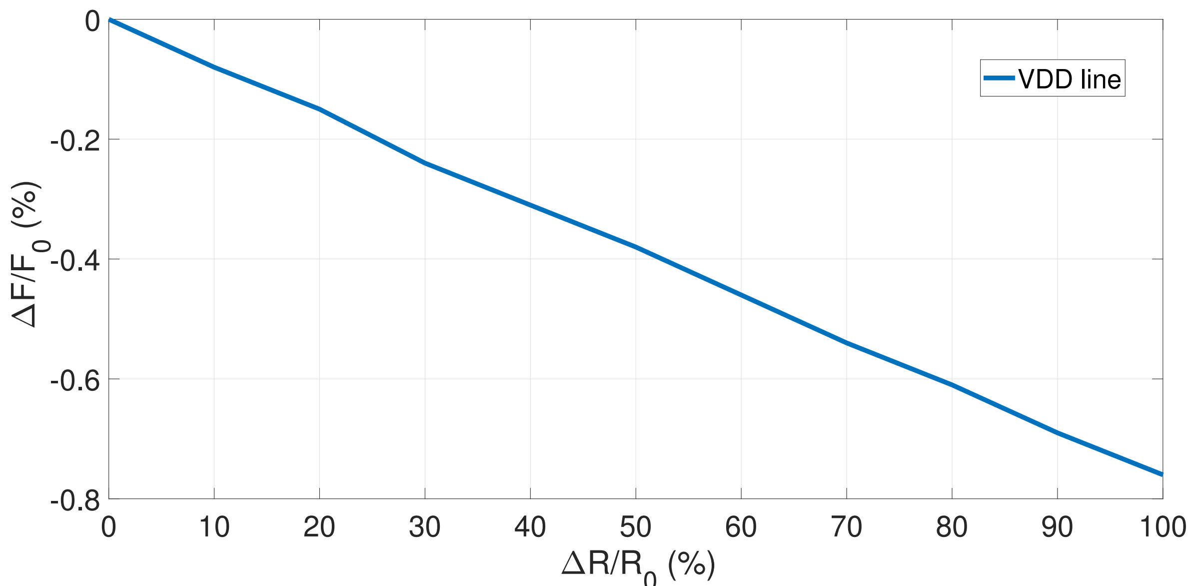

Figure 6.4 – Frequency change in oscillator as a function of the resistance increase.

The faster the ratio $\Delta R/R_0$ of a line increases, and the circuit performance degrade, more critical is the line. Although long interconnects can be more resistive and more susceptible to the formation of voids, a small one affected by a void can deteriorate faster, degrading circuit performance parameters, like frequency response and delay.

6.2 Evaluation of a Bandgap Circuit under Electromigration

Figure 6.5 shows the layout of a bandgap circuit that supplies a reference voltage (VBG) of 1.3 V, under typical conditions, to bias other circuits of a piezoelectric sensor [205, 206]. The circuit, designed in XFAB XC06 technology, has three Al metal layers with TiN barrier layer. For this technology, the minimum width of the Metal 1, Metal 2, and Metal 3 are 0.9 μm, 0.9 μm and 1.1 μm, respectively [207]. In order to evaluate the circuit, two studies are carried out: a) first, we investigate the VDD line and b) we extend the study to evaluate the lines connected to transistors terminals.

The VDD line carries the highest current of the circuit, 630 μA, resulting in a current density of 0.14 mA/μm. The current density is lower than the j_{max} of 1.0 mA/μm from the XFAB XC06 technology [207]. The VDD line presents the Blech product of 0.031 A/μm, which is three times lower than the threshold of 0.1 A/μm for Al interconnects [208]. Thus, the traditional criteria indicate that the VDD line is not an EM critical line.

We evaluate the performance change of the circuit due to EM using the parameters from Table 6.3. The resistance of the VDD line increases from 1.5 Ω to 5.5 Ω after 5 years considering an operation at 80 °C (353 K), a significant increase of 366%. The resistance change reduces the VBG by only 0.13% of the nominal value after 5 years. This result indicates that the line is not critical regarding to the performance change criterion. Table 6.4 summarizes the results.

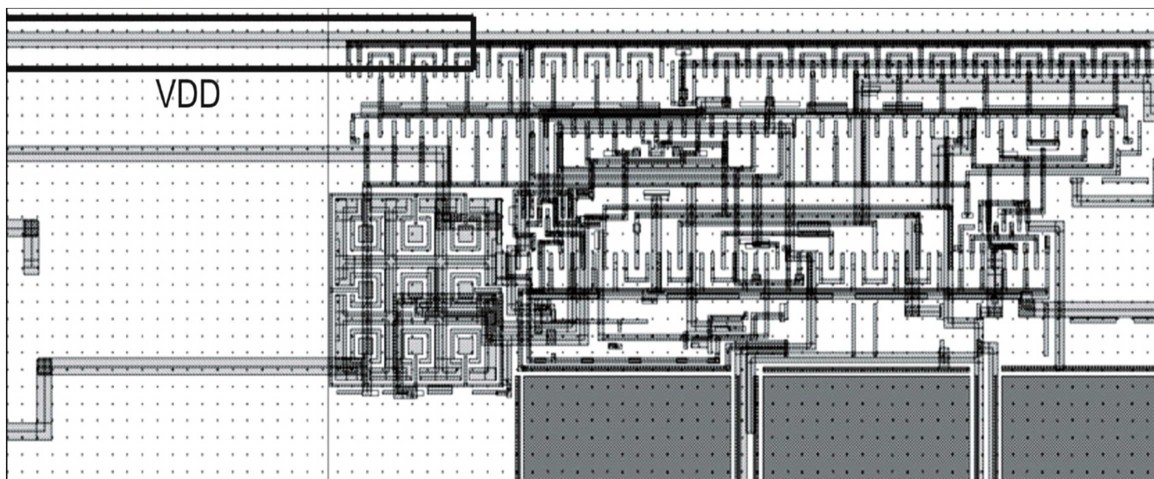

Figure 6.5 – Layout of the bandgap voltage circuit.

Table 6.3 – Parameters used to evalute the Al lines of the bandgap circuit.

Parameter	**Value**	**Unit**	**Ref**
Line width	4.5	μm	-
Line length	113	μm	-
Line heigth	0.5	μm	[207]
Temperature	353	K	-
Al resistivity	29.2x10^{-9}	Ωm	[114]
Barrier height	0.12	μm	[207]
TiN resistivity	0.65x10^{-6}	Ωm	[209]
Al difusivity (353 K)	1.17x10^{-16}	m^2/s	-

Table 6.4 – VDD line evaluation for the bandgap circuit.

Criterion	**Blech Effect**	$\mathbf{j}_{max}$	**VBG in 5 Years**
Limit	0.1 A/μm	1 mA/μm	5%
Designed	0.031 A/μm	0.14 mA/μm	0.13%
Situation	Non-critical	Non-critical	Non-critical

From the above analysis, it is clear that EM is not an issue for the VDD line. In fact, the line width could be reduced without affecting the circuit performance or reliability. This reduction does not bring apparent advantages. However, when a large portion of the BEOL interconnects are considered, resizing such lines can lead to significant area reduction.

The method is now extended to the other lines of the bandgap circuit, evaluating the overall impact of the BEOL interconnects on the bandgap voltage (VBG). Figure 6.6 shows the current density of the lines connected to the drain and source from the 40 transistors of the bandgap circuit. All the lines are subjected to current densities below the j_{max}. In fact, most of them are two orders of magnitude lower than the j_{max}.

Figure 6.7 shows the VBG variation (ΔVBG) in 2, 5, and 10 years due to EM in the 40 drain lines. The highest change of 2.1 mV corresponds to a 0.2 % of the VBG. Note that the line #17 affect the VBG more significantly, even though there are other lines operating with higher current densities. This is an indication that a line can be non-critical due to the traditional criteria, nevertheless, it can eventually degrade the circuit performance.

Figure 6.8 shows a comparison of the current density for the as-designed lines and for the lines resized to the minimum width allowed by the technology. Note that the width reduction results in a minimal current density increase for most of the lines. The current density through the line #17 increases by more than 10% and it is still much lower than the j_{max}.

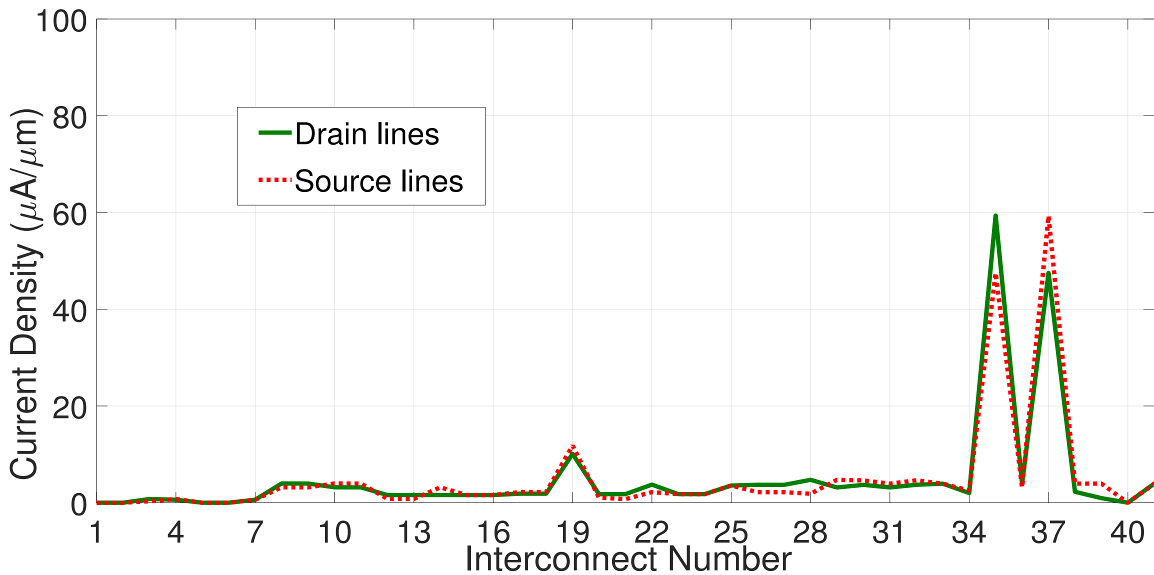

Figure 6.6 – Current density through lines connected to the drain and source of the transistors.

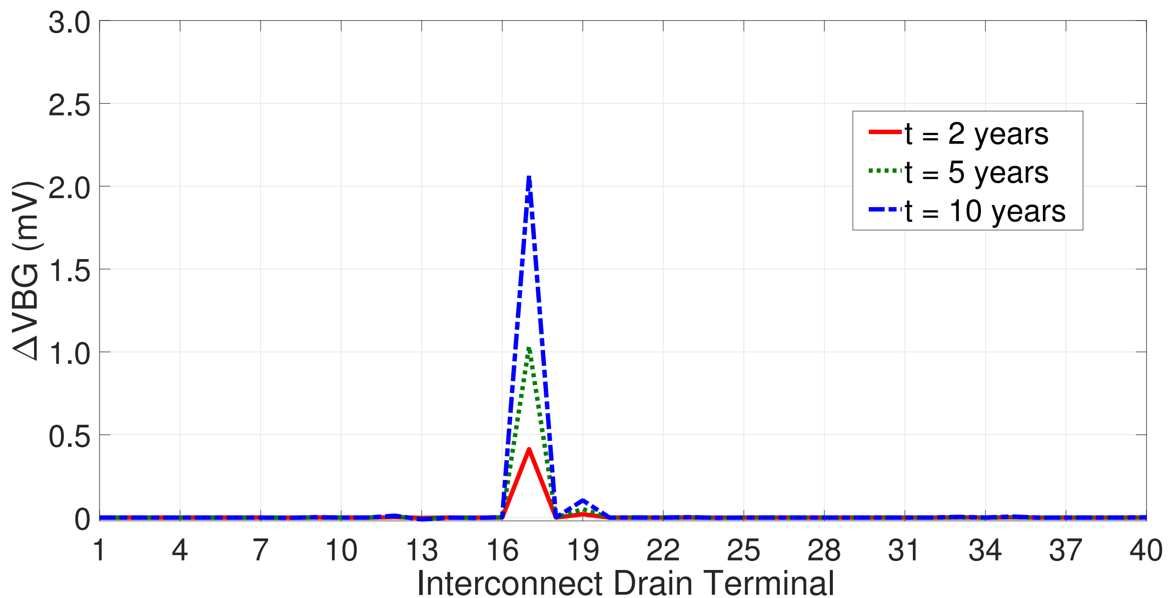

Figure 6.7 – VBG change due to EM in the drain interconnects for different operation times.

Figure 6.9 shows the VBG variation considering the resized lines under EM for 2, 5, and 10 years. The line #17 changes the VBG by 2.8 mV, 0.22% of the nominal VBG, a very small change, similar to the results from the as-designed lines in Figure 6.7. It indicates that the lines can be designed with the minimum dimensions and the reliability and performance of the circuit in terms of EM is still mantained.

So far, the results considered the EM degradation in each line individually. We consider now an extreme case, where the EM affects all the lines simultaneously. The EM

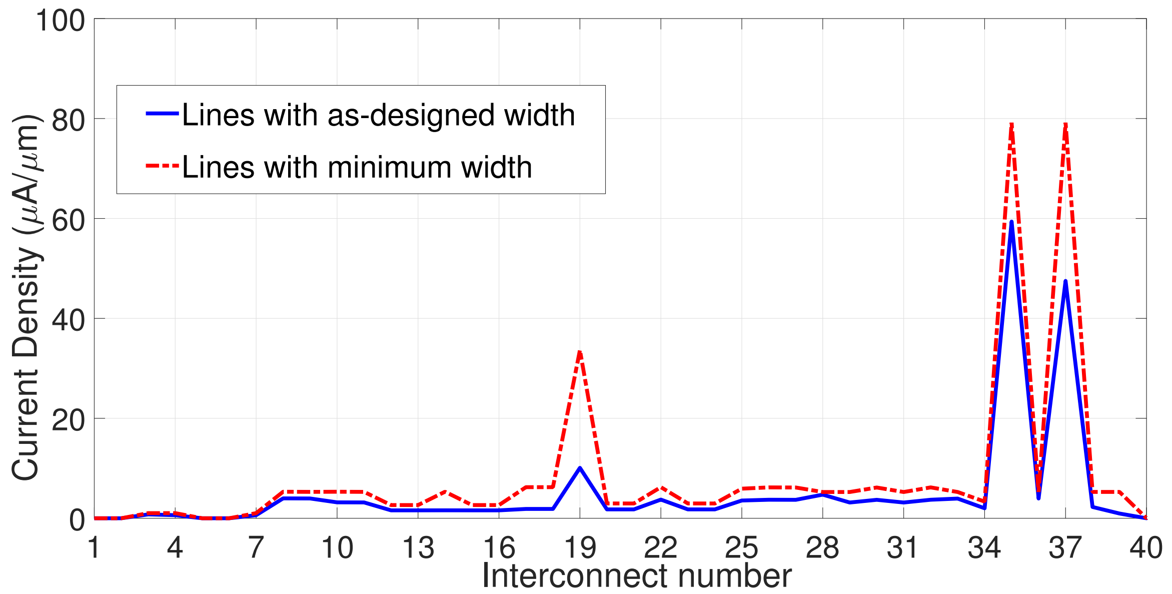

Figure 6.8 – Current density thougth the lines with the designed width and the minimum width.

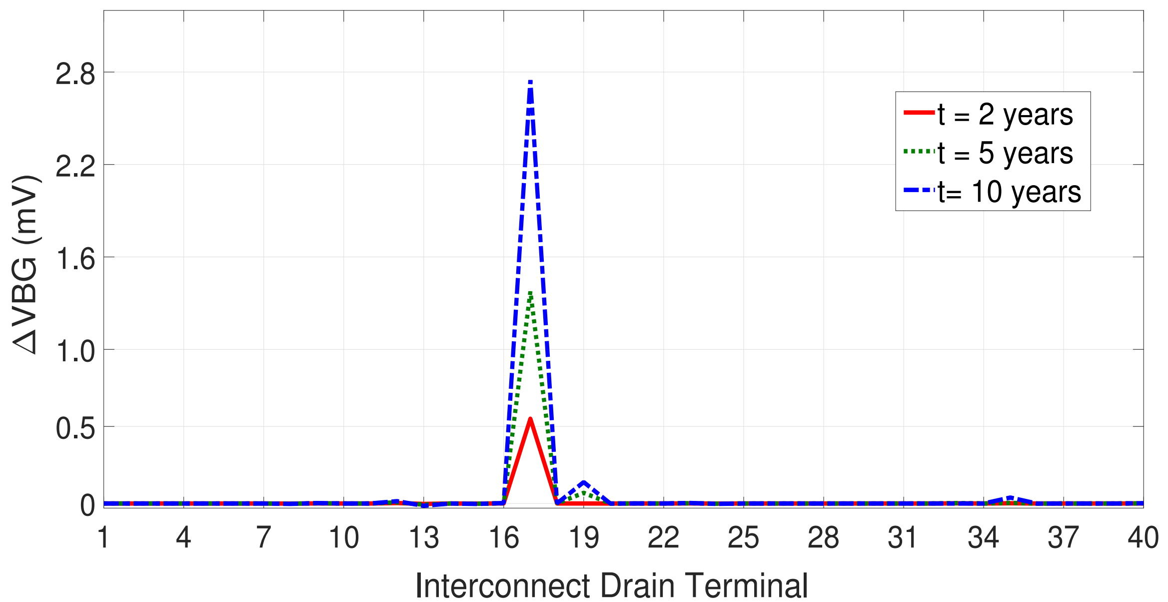

Figure 6.9 – VBG change for the lines with the minimum width.

occurrence in all the lines is improbable to occur, but such an analysis provides a general assessment of the circuit variation regarding multiple resistance variations of the lines.

Figure 6.10 shows the ΔVBG for the as-designed lines and the resized lines with the time. The maximum ΔVBG is below 0.02%, which is even lower than the variation for EM in individual lines (0.22%). The resistance increase due to EM in various lines seems to compensate for the circuit VBG variation.

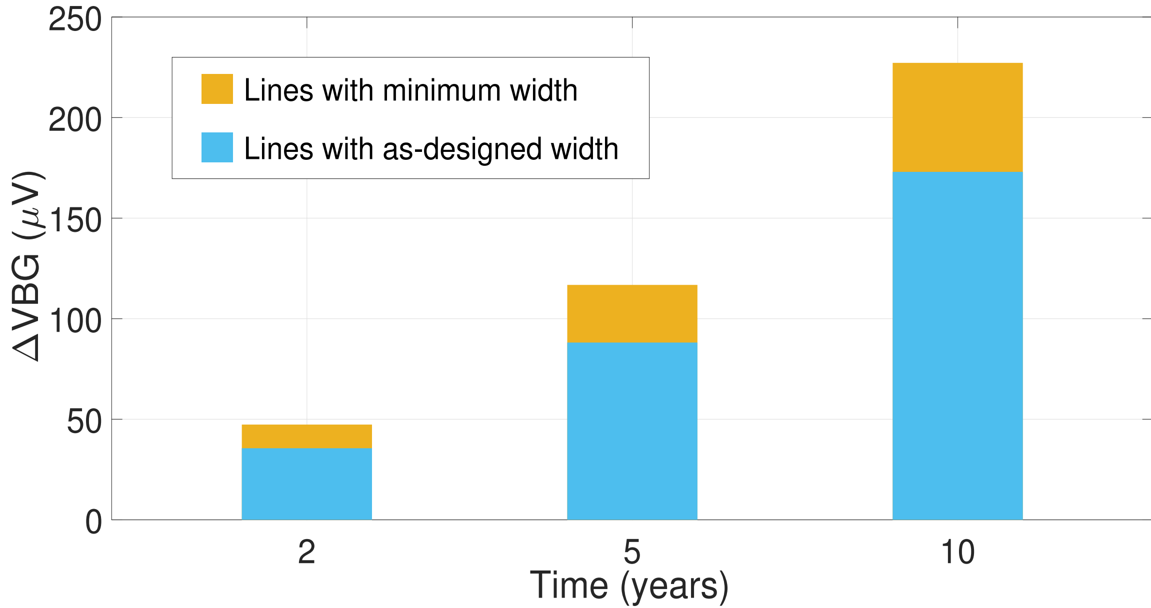

Figure 6.10 – VBG variation when all lines are assumed to be under EM.

6.3 Evaluation of an Operational Amplifier under Electromigration

We apply the proposed method to investigate the EM impact on the performance of an operational amplifier (Opamp). This amplifier contains 20 transistors and 15 interconnects. It is designed to have 40 dB gain at 1 MHz, unit gain frequency (UGF) of 730 MHz, output voltage swing of 2.2 V and maximum settling time of 10 ns, at 125 °C. The amplifier is fed by a 2.6 V differential voltage (|avdd|=|avss|=1.3 V). It is designed in a 45 nm technology, which is composed by three metal layers (M1, M2, and M3) of Cu using a TaN barrier layer. M1 has a minimum width of 60 nm, while M2 and M3 have a minimum width of 80 nm [210]. Figure 6.11 shows the operational amplifier schematics and Figure 6.12 presents the designed layout of the IC.

The "avdd", "avss" and "outp" lines are subjected to the highest "current densities" (here, design nomenclature – current per width – will be used throughout the text), above 2 mA/μm, as simulated with the EAD Cadence tool. The simulated current

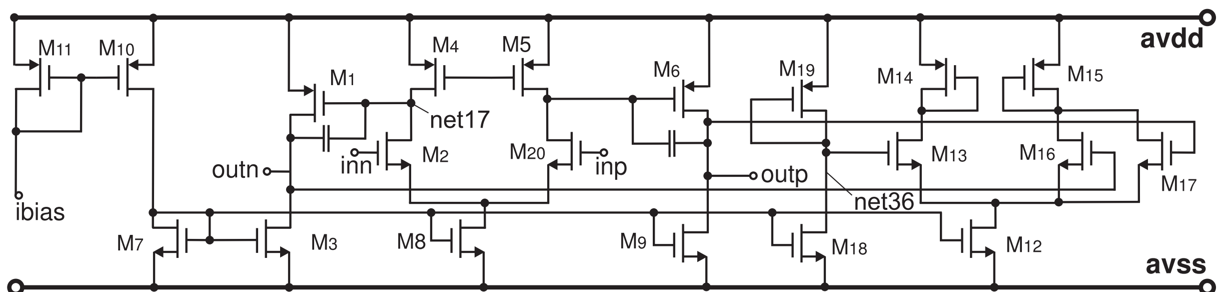

Figure 6.11 – Operational amplifier used to evaluate the EM effect of the lines resistance variation on the circuit performance degradation.

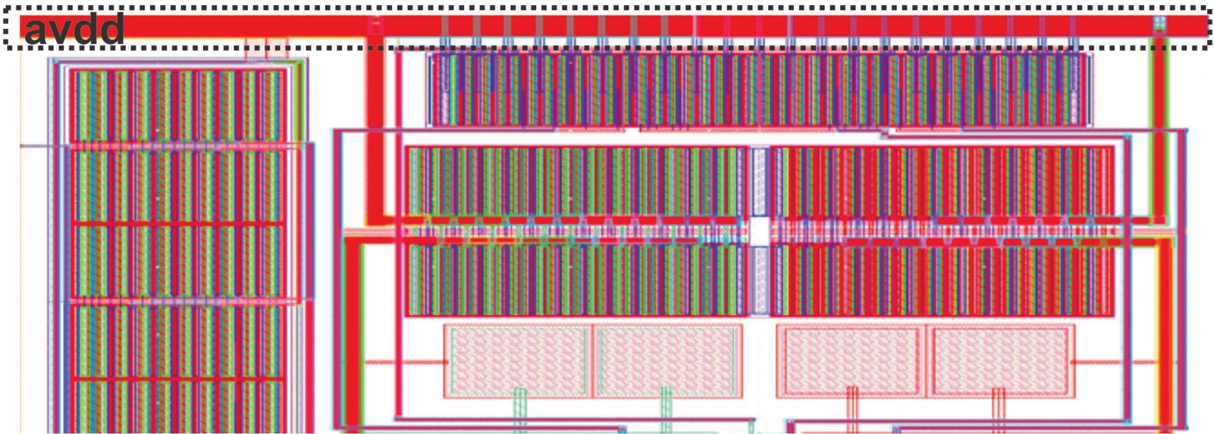

Figure 6.12 – Layout extract from the evaluated differential amplifier with the avdd line highlighted.

for the avdd line is 3.1 mA, which given the line dimensions, represents a maximum current density of 2.9 mA/μm. This is a high current density from an EM point of view, considering that the technology limit is set to 2 mA/μm for M1 in a 45 nm design [210].

The IC performance changes are evaluated due to EM for a time interval and specific temperature. AC, DC and transient analysis are performed to study the variations of the circuit parameters. The results are compared with the obtained with the EAD, an EM Cadence tool that classifies the lines as critical based on the current density threshold from the technology [211].

Figure 6.13 shows the relative void length evolution (l_v/L) for a current density of 2.9 mA/μm, for two different temperatures, 353 K (80 °C) and 398 K (125 °C). While the void needs 5 years to reach 2% of the total line length at 80 °C, the same percentage is obtained in only 51 days at 125 °C. It is interesting to observe that a l_v/L of 2% yields an increase of 31% in the line resistance. From the interconnect point of view, this value is surely large, however, it is the impact of such an increase on the circuit performance that determines the IC robustness and reliability against EM. Then, the IC designer can use the proposed method to identify the lines that affect the chip performance.

Figure 6.14 illustrates the void length evolution for temperatures between 300 K (27 °C) and 400 K (127 °C) for 1 year of operation. While operating in low temperatures, an l_v/L variation lower than 1% is obtained. In a higher temperature, like 390 K (117 °C), the void reaches 8% of the line, increasing the line resistance to 125%, surely causing performance degradation.

Based on the resistance variations calculated above, we investigate the performance change of the amplifier at 125 °C after 5 years of operation. Two studies are carried out: a) first we investigate the EM effect on the transistors' transconductance (g_m) and on the threshold voltage (V_{TH}), b) we evaluate the circuit performance variation.

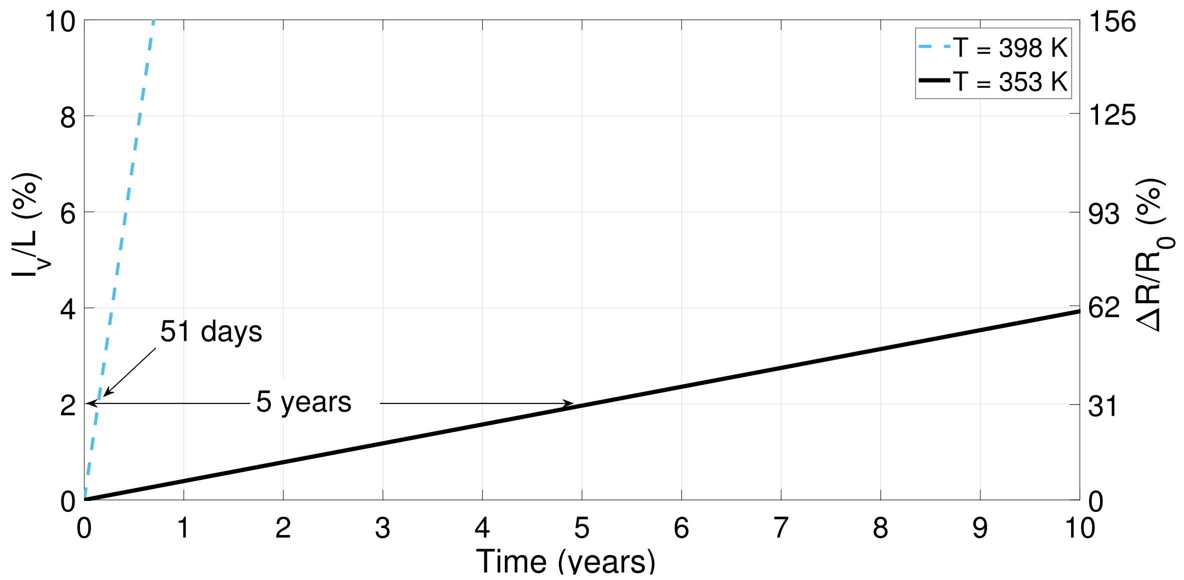

Figure 6.13 – Void length relative to the line length and the line resistance increase as a function of time for 353 K (80°C) and 398 K (125°C).

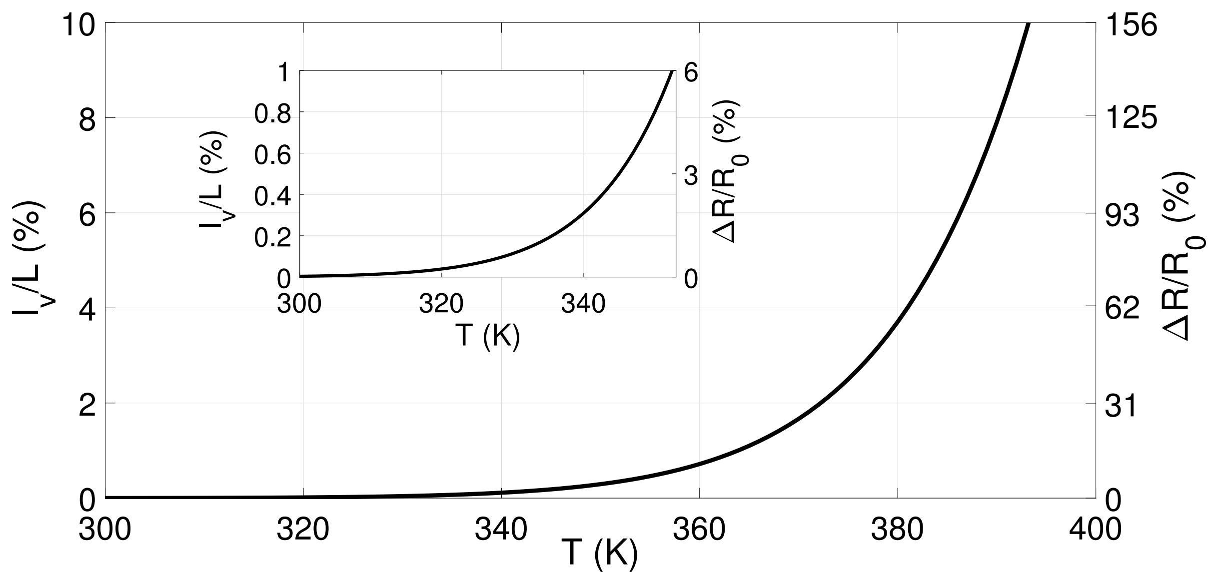

Figure 6.14 – Void length relative to the line length variation with temperature and line resistance change after 1 year.

Figure 6.15 shows the g_m for all the 20 transistors of the Opamp in their initial condition and also after 5 years of operation experiencing EM in several lines of the layout, namely the “avdd”, the “avss” and the “outp” line. Considering the EM damage from the avdd line, except for the M9, the g_m magnitude of all transistors decreased. The transistor M1, for example, presented a variation from 5.5 mS to 2.9 mS, a reduction of 48%. This means that for the same gate voltage signal, only half drain signal current is supplied compared to the initial condition. Such a large reduction of g_m indicates a serious degradation in the gain of the amplifier, as it will be seen later. Similarly to the avdd line, EM in the avss line also leads to a large g_m variation, as shown in Figure 6.15. An

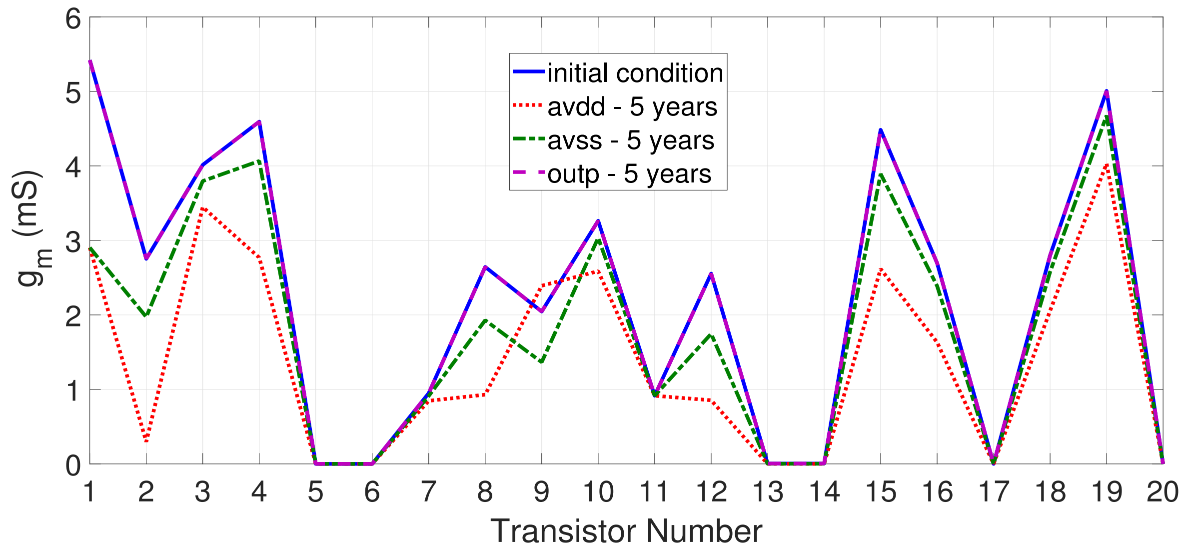

Figure 6.15 – Transconductance variation for the 20 Opamp transistors due to the EM in several lines for 125 °C.

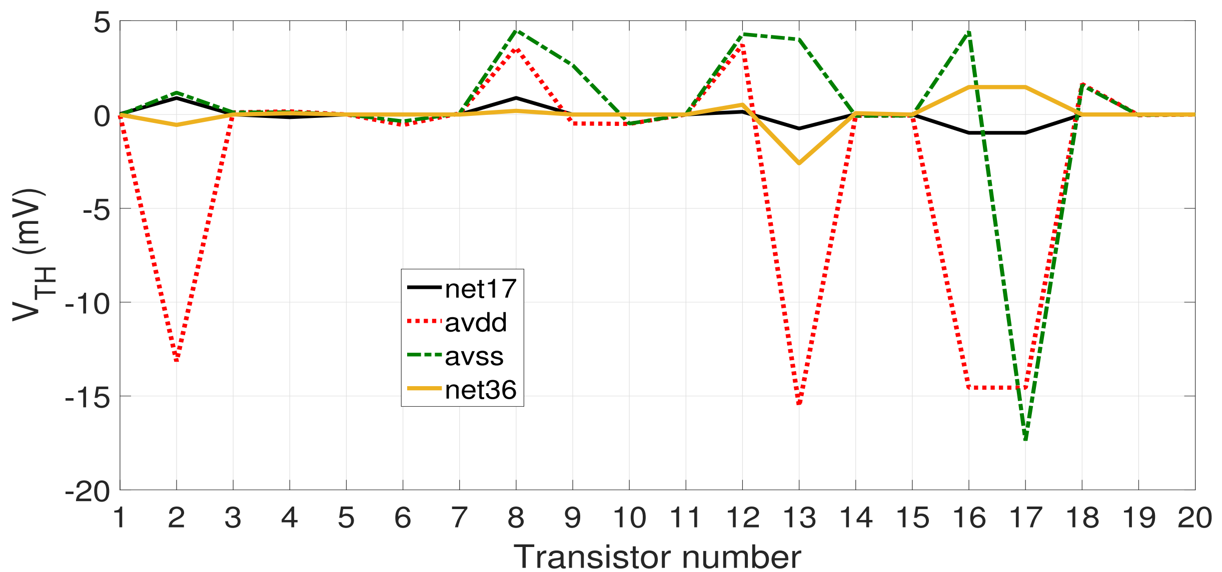

Figure 6.16 – V_{TH} variation for the 20 Opamp transistors due to the EM in several lines for 5 year operating at 125 °C.

interesting result is obtained, however, if we analyze the line outp. This line is subjected to a current density of 2.36 mA/μm, being above the 2 mA/μm threshold. Nevertheless, its corresponding resistance change does not affect the transconductances significantly. After carrying out a similar analysis for the other 12 lines of the layout, we observed negligible g_m changes.

Figure 6.16 shows the threshold voltage (V_{TH}) variation of each transistor. The V_{TH} is a fundamental parameter and it varies with the bias voltages of the transistors [212, 213]. Again, the avss and avdd lines have a more significant effect on this parameter.

Due to the EM in the avss line, the bulk-source voltage of device M17 change and the V_{TH} varies 17.5 mV. This decrease can alter the current flow and the transistor operation region. Differently from the g_m results, the EM effect on the net36 and net17 has a visible influence on the V_{TH}. This degradation is more pronounced for the transistors M13, M16 and M17 for which the bulk-source and the drain-source voltages are changed by the increased resistance in the interconnects due to EM [214]. With the reduction of the V_{TH} the performance of the opamp degrades.

Based on the analysis above, the method is now extended to evaluate the amplifier performance regarding its unit gain frequency (UGF), voltage gain, output voltage swing and settling time (ST). In this way, the overall impact of the EM in the BEOL interconnects on the circuit performance is predicted.

Figure 6.17 shows the amplifier UGF variation with time considering that the avdd, avss, outp, net17, and the other 11 lines are degrading due to EM. As a simplification, the lines with smaller influence on the UGF are named as "other lines". In general, the avss and the avdd degrade the UGF performance the most.

For the avss line the UGF has varied from the initial frequency from 729.4 MHz to 607.3 MHz, a variation of 16.73% in only 8 months. Note that the outp line is also subjected to a large current density, however, its impact on the UGF is clearly much lower than the effect of the avdd and the avss lines.

The net17 line is an interesting case. From the maximum current density evaluation, it is not a critical line, as its current density remains below 2 mA/μm. However, from the UGF degradation point of view, its impact is as significant as the outp line,

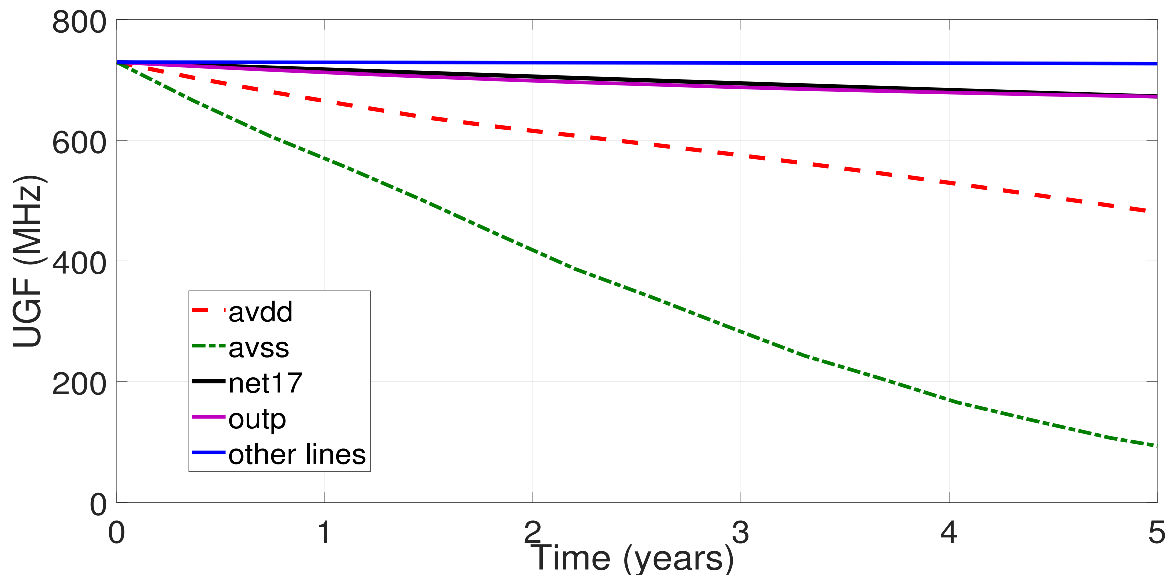

Figure 6.17 – Unit gain frequency variation with time for different interconnects under EM at 125 °C.

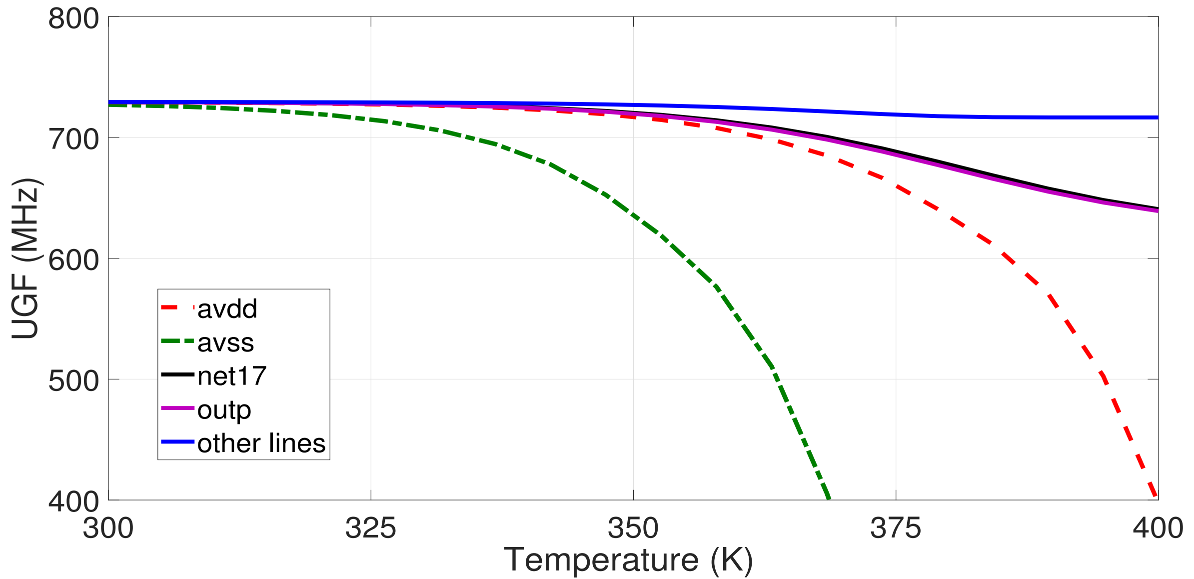

Figure 6.18 – UGF variation with temperature after 7 years.

as shown in Figure 6.17. Thus, even though the outp and the net17 lines have distinct classifications following the standard current density criterion, their impact on the chip performance is similar.

Figure 6.18 illustrates the UGF variation with temperature from 300 K (27 °C) to 398 K (125 °C) in 7 years. Observe that, for the avss operating at 353 K (80 °C) the void increases 3%, but representing a resistance variation of 46.5%. It degrades the UGF to 619 MHz, a reduction of 15% in relation to the nominal value. For a higher temperature the degradation is accelerated, reducing the performance below 400 MHz. The avdd has also a large impact, although not as strong as the avss line. Note that the lines outp and net17 lead to a relatively small change for this parameter, even for higher temperatures.

Figure 6.19 shows the voltage gain variation after 5 years of operation at 125 °C. Here, the EM in net17 is responsible for the larger gain degradation, reducing 30% in 1.2 years, decreasing from 40 dB to 37 dB. After 2 years the gain decrease reaches 52%. This large gain variation makes the Opamp useless. The lines avss and avdd do not cause a critical gain variation, being less than 3 dB in 5 years. It is important to emphasize that the net17 operates with a lower current density than the avss and avdd lines, nevertheless, it affects the circuit gain more significantly. The net17 connects the differential pair to the output of the opamp. An increase in the resistance of the net17 changes the polarization of the transistors and affects the gain.

Figure 6.20 presents the cutoff frequency (f_c) evolution with time highlighting the lines net17 and avss as the most relevant. While the avss under EM produces a decrease in the f_c, the net17 leads to an increase of this performance. Note that other

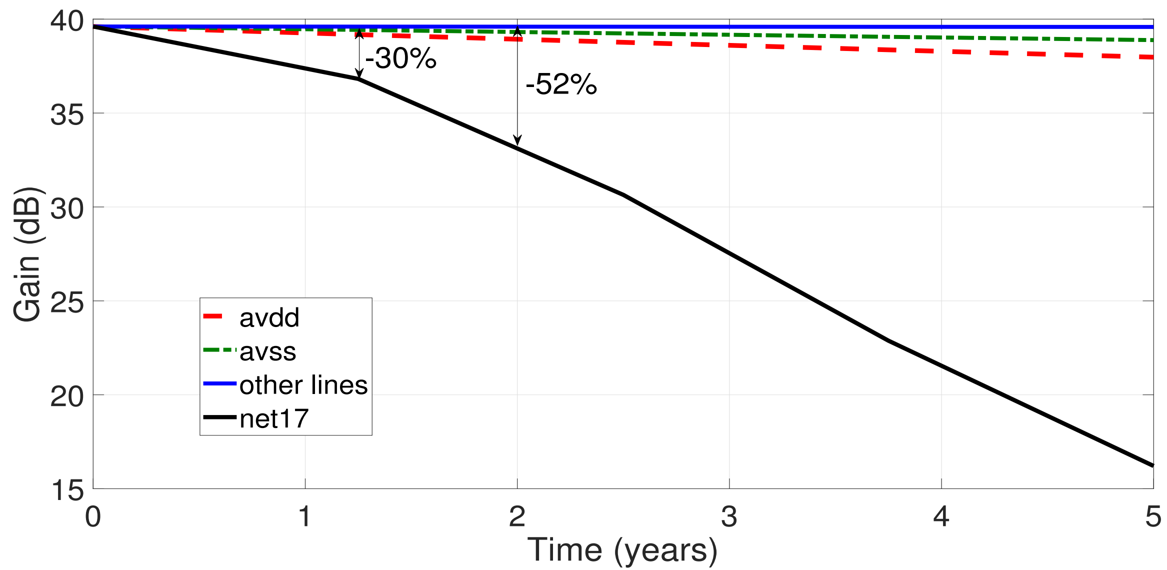

Figure 6.19 – Gain variation in 5 years of operation at 125 °C.

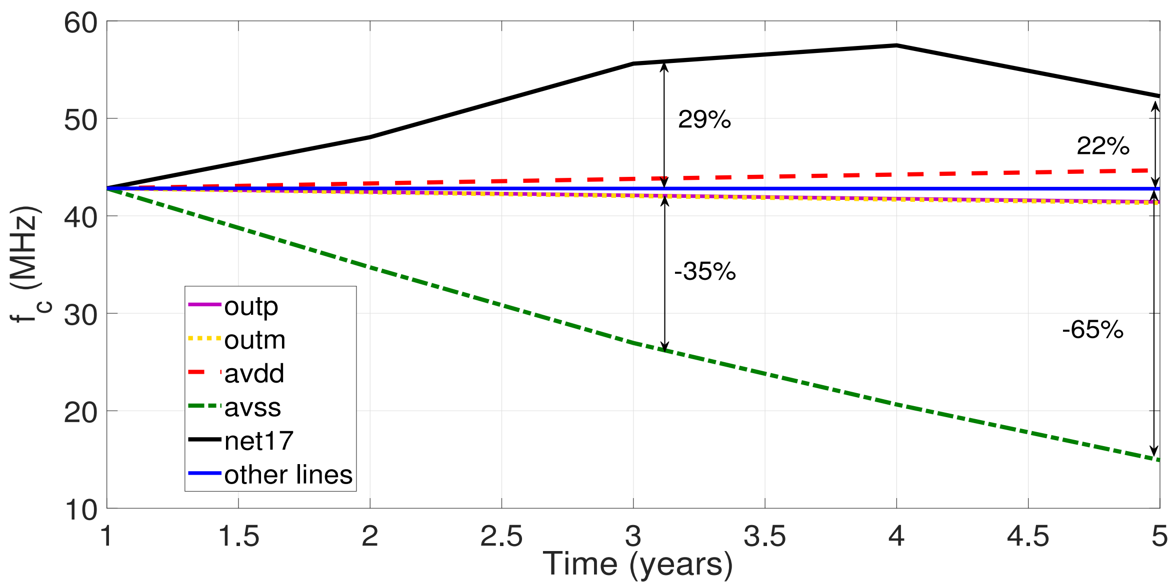

Figure 6.20 – Cutoff frequency variation in 5 years of operation at 125 °C.

interconnects result in a slight change in the cutoff frequency. This is true even for the avdd and outp lines, both of which subjected to the highest current densities.

The voltage gain, unit gain frequency and cutoff frequency have been evaluated with an AC analysis. Two other parameters of the Opamp are investigated using a transient analysis: the settling time and the output voltage swing.

Figure 6.21 shows the voltage swing variation with operation time. Note that five interconnects have a significant impact in this parameter. The largest decrease is observed for the avdd and net17 lines, resulting in a decrease of 14.07% after 5 years. It should be noted that the line “outm”, which has not been critical so far, appears now as a source of measurable parameter deviation.

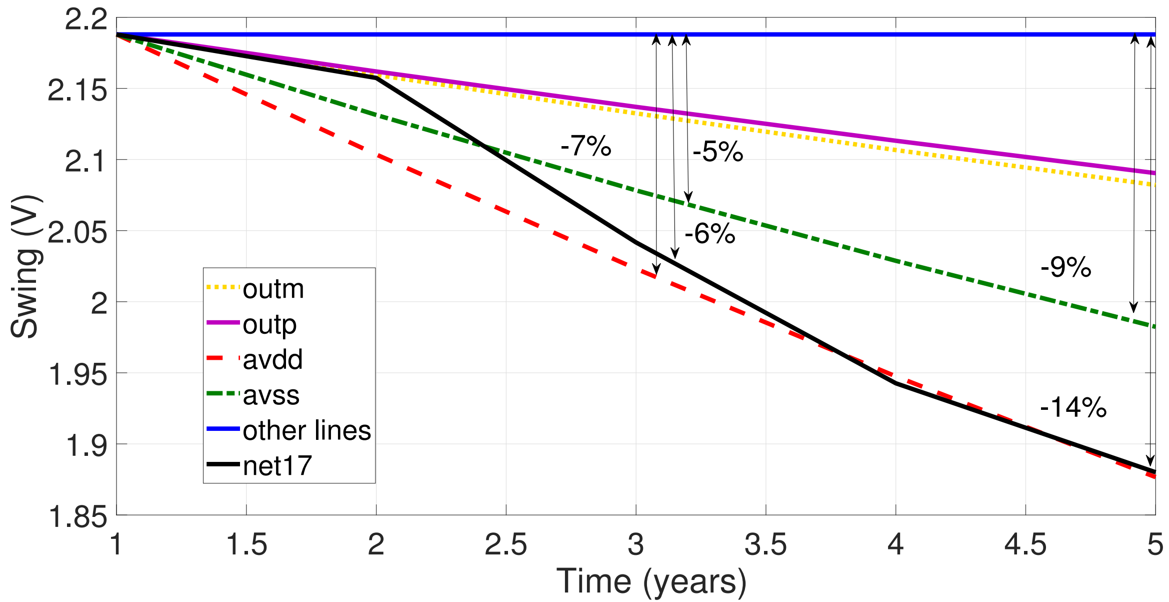

Figure 6.21 – Swing voltage variation in 5 years of operation at 125 °C.

Figure 6.22 presents the settling time variation. As before, the lines avdd, avss and net17 influence the performance more significantly than the other lines. However, an interesting difference appears here. While the degradation of net17 leads to an increase of the settling time by 8.91% after 5 years, a critical situation, as the expected settling time should be below 10 ns, the avss and avdd lines resulted in a time decrease of 11.95% and 16.74%, respectively.

The previous analysis considered that the EM occurs in just one of each line at a time. Thus, the performance variation is evaluated due to the resistance change of a single interconnect. However, during circuit operation several, if not all, lines can suffer EM simultaneously. This simultaneous degradation of multiple lines is analyzed next. The resistances increases are included in all lines at once and a combined study of the circuit is carried out.

Figure 6.23 depicts the gain and the UGF temporal evolution. They vary by 27% and 14%, respectively, within 5 years (T= 125°C). Interestingly, the gain reduction here is lower than the largest decrease observed in Figure 6.19 due to the net17 degradation alone in 2 years (52%). The UGF variation is also smaller than the worst case measured in Figure 6.17. A possible explanation for this behavior is that the bias of the devices is partially compensated by the set of resistance changes, reducing their impact on the circuit performance.

Figure 6.24 shows the settling time and swing voltage variations in a transient evaluation. Observe that the swing voltage becomes worse by the EM effect in all the lines. It decreases by 31.28% in 5 years, a much larger reduction than that of 14.07%

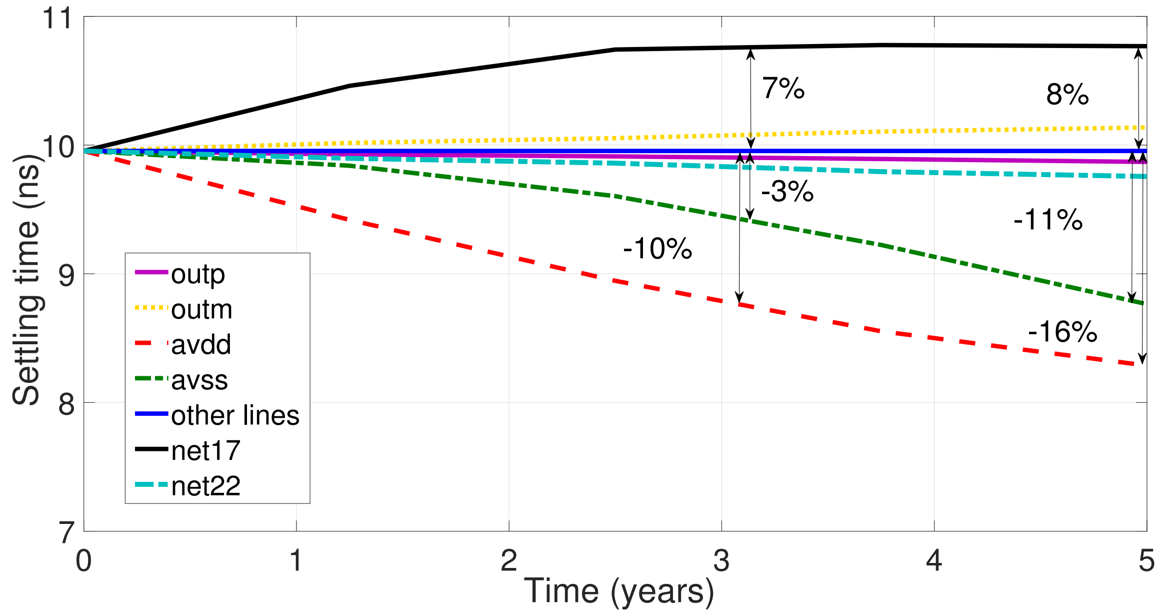

Figure 6.22 – Settling time variation in 5 years of operation at 125 °C.

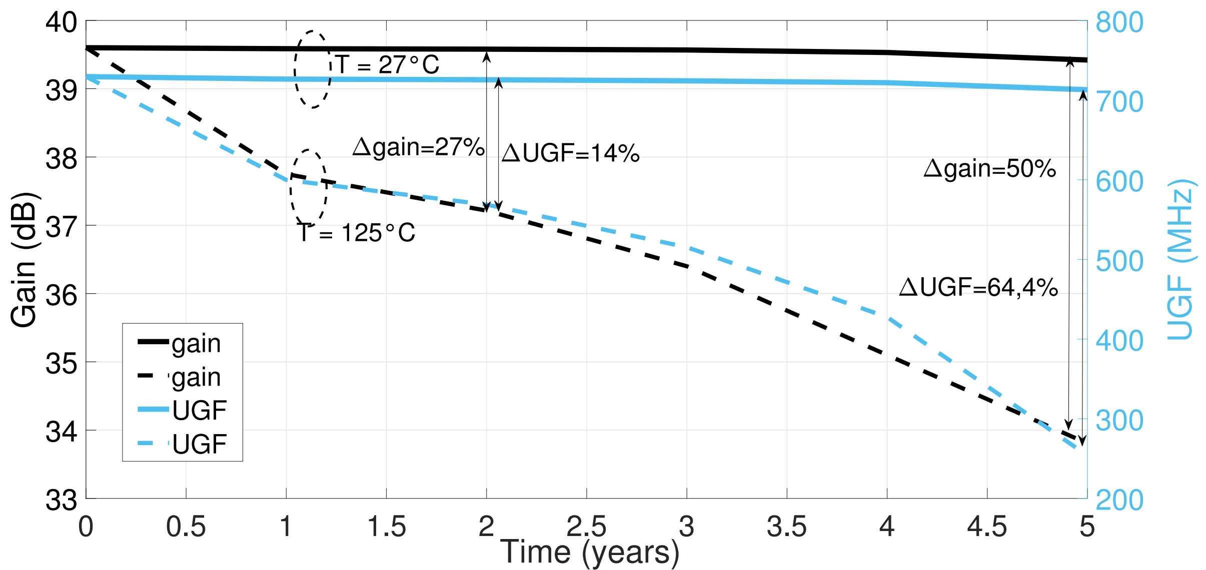

Figure 6.23 – Gain and UGF variation considering all interconnects under EM simultaneously.

observed in Figure 6.21.

Table 6.5 summarizes the above results and shows the lines that affect more significantly the performance parameters of the Opamp. Observe that the avss and avvd are critical by the current density criterion and they have the highest impact on the UGF and f_c parameters. The net17 leads to a larger degradation of the gain, ST and swing, even though it is classified as non-critical by the traditional method, since it has a current density below the 2 mA/μm.

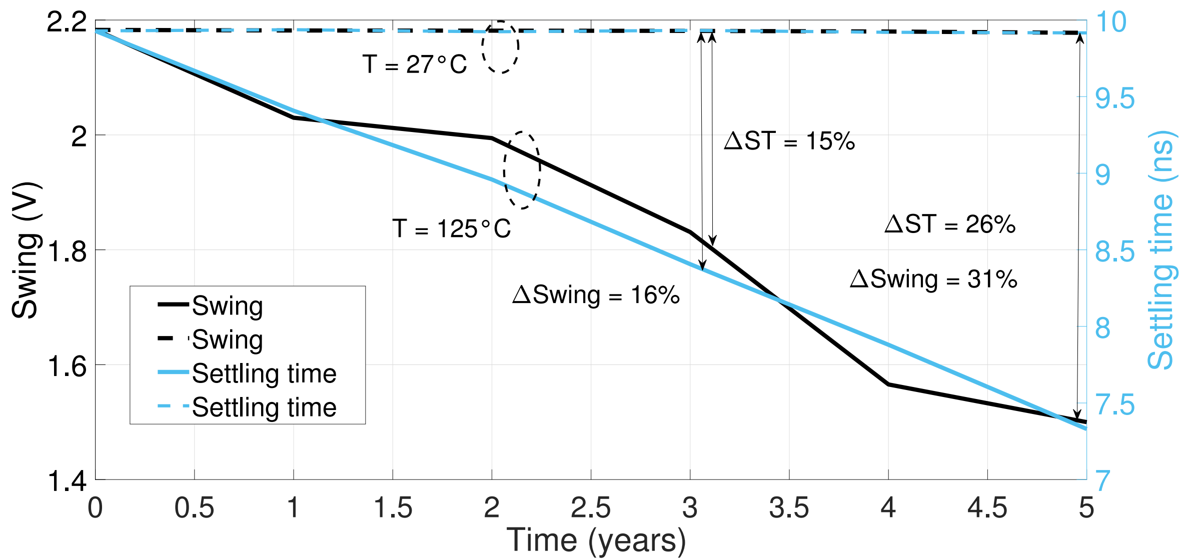

Figure 6.24 – Settling time and swing voltage variation for all lines affected simultaneously by EM.

Table 6.5 – Summary of performance parameters indicating the most critical interconnect and the line condition from the traditional evaluation.

Parameter	Main line	j (mA/µm)	EAD condition
UGF	*avss*	5.4	Critical
gain	*net17*	1.9	Non-critical
f_c	*avss*	5.4	Critical
ST	*net17*	2.9	Critical
swing	*net17*	1.9	Non-critical

An interesting view about the IC lifetime is that it depends on the time for a crucial parameter to vary by a given magnitude in relation to the nominal value. If the gain is the most significant performance parameter for the Opamp, the circuit lifetime is then determined by the gain variation, i.e. the time for the gain to decrease by 3 dB. Therefore, depending on the application, the UGF or the settling time can be more critical than the swing voltage, for example, even if the latter suffers a larger change during the same period. In this case, the UGF and the settling time would determine the circuit lifetime. This same reasoning can be extended to other parameters and circuits. The methodology developed in this work is an innovative design tool applied for such investigations.

6.4 Evaluation of the Temperature in a 45nm Technology

Recent works [133, 215] have evaluated the influence of the BEOL layers on the temperature distribution based on the estimation of the thermal conductivities of each interconnect layer. The volume fraction of the metallic and via layers affect directly

Table 6.6 – Thickness and width of the lines and via layers from FreePDK45 technology.

Layers	Thickness (nm)	Minimum metal/via width (nm)
Contact	85	4.5
Metal 1	130	65
Via 1-2	120	65
Metal 2,3	140	70
Via 2-3, 3-4	120	70
Metal 4,5,6	280	140
Via 4-5, 5-6, 6-7	290	140
Metal 7, 8	800	400
Via 7-8, 8-9	820	400
Metal 9, 10	2000	800
Via 9-10	2000	800

the BEOL thermal conductivity. An increase in the number of vias and metallic layers provides more paths for easier heat flow and reduces the ΔT_{PT} in regions next to the heat source [133].

We evaluate an interconnect structure formed by ten metallization layers and 9 via layers of the FreePDK45 technology [216], described in Table 6.6. Three analyses are performed: 1) the temperature of the local layers is evaluated considering a different number of vias in Via 2-3 layer and metal in Metal 2 layer; 2) the temperature of the BEOL is evaluated considering the thermal conductivity of the metallic and the via layers; 3) the impact of the temperature on the resistance of the lines due to EM are calculated, taking into account the temperature distribution previously obtained. The lines are set to the same length of 10 μm and operate with the maximum current density allowed by the technology, which corresponds to a current of 2 mA/μm [171].

6.4.1 Temperature Change of the Local Layers with Volume Fraction Variation on a Single Layer

Figure 6.25(a) shows part of the structure used to evaluate the temperature change in the local layers as a function of the via and metal layer volume fraction. It is composed by three metallization levels, M1, M2, and M3 and two via layers, Via12 and Via23. The ΔT_{PT} is evaluated for different values of the volume fraction of M2 (V_{INT}M2) and Via23 (V_{VIA}23), represented in Fig.6.25(b) and Fig.6.25(c), respectively.

Figure 6.26 shows the ΔT_{PT} for the local layers for different values of V_{INT}M2. For a V_{INT}M2 of 50%, superior to a typical V_{INT} value from 28% to 40% [133], the temperature increase in M1 and M2 is 102.5 K and 81 K, respectively. For a V_{INT}M2 of 10% the temperature increase in M1 is 104.2 K, a change of 1.7 K. For M2 the ΔT_{PT}

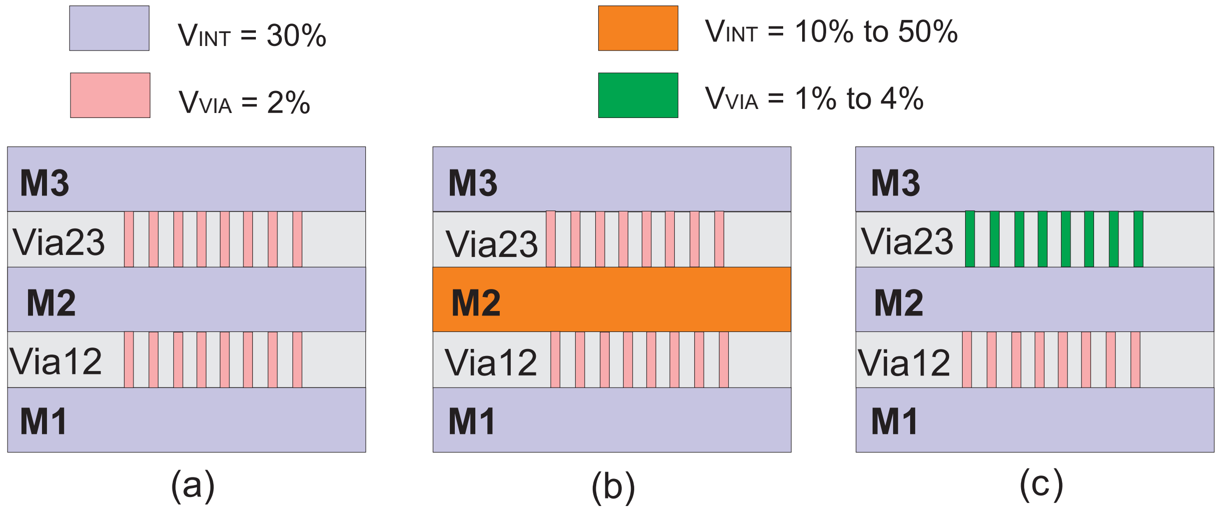

Figure 6.25 – (a) Structure used to evaluate the temperature change in local layers with the changes in: (b) metal volume fraction in V_{INT}M2 from 10% to 50% and (c) via volume fraction in V_{VIA}23 from 1% to 4%.

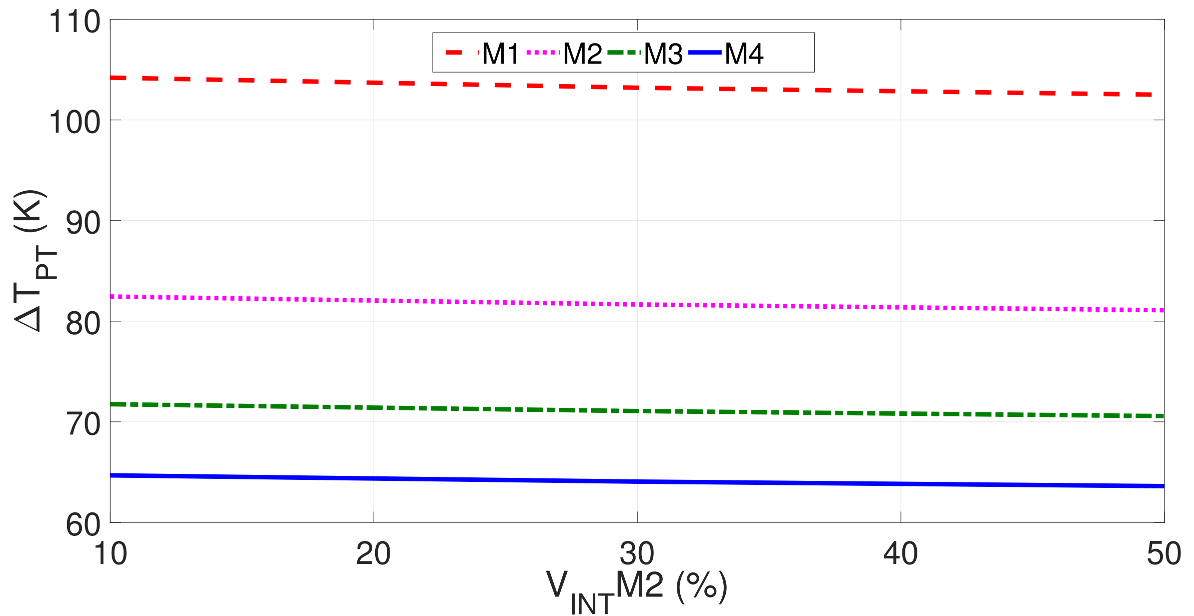

Figure 6.26 – ΔT_{PT} in local layers for different V_{INT}M2 for $P_T = 500$ W/m.

increases to 82.5 K. Observe that the difference in ΔT_{PT} is small, below to 2%, as the alteration occurs only in the M2 layer, while the other 9 layers from the BEOL have a V_{INT} of 30% and a V_{VIA} of 2%.

Figure 6.27 shows the ΔT_{PT} for the local layers as a function of the V_{VIA}23 with V_{INT} of 30%. For a V_{VIA}23 of 4% the temperature increase in M1 and M2 is 103.2 K and 81.6 K, respectively. For a V_{VIA}23 of 1%, the ΔT_{PT} in M1 is 103.7 K. The ΔT_{PT} in M2 is 82.1 K. In the section 6.4.3 we shows that increasing the number of vias in all the layers, not only in V_{VIA}23 layer, results in a higher k_{eff}^{BEOL} and a more significant ΔT_{PT} reduction is obtained in the layers near the heat source. Note that the M1 layer shows

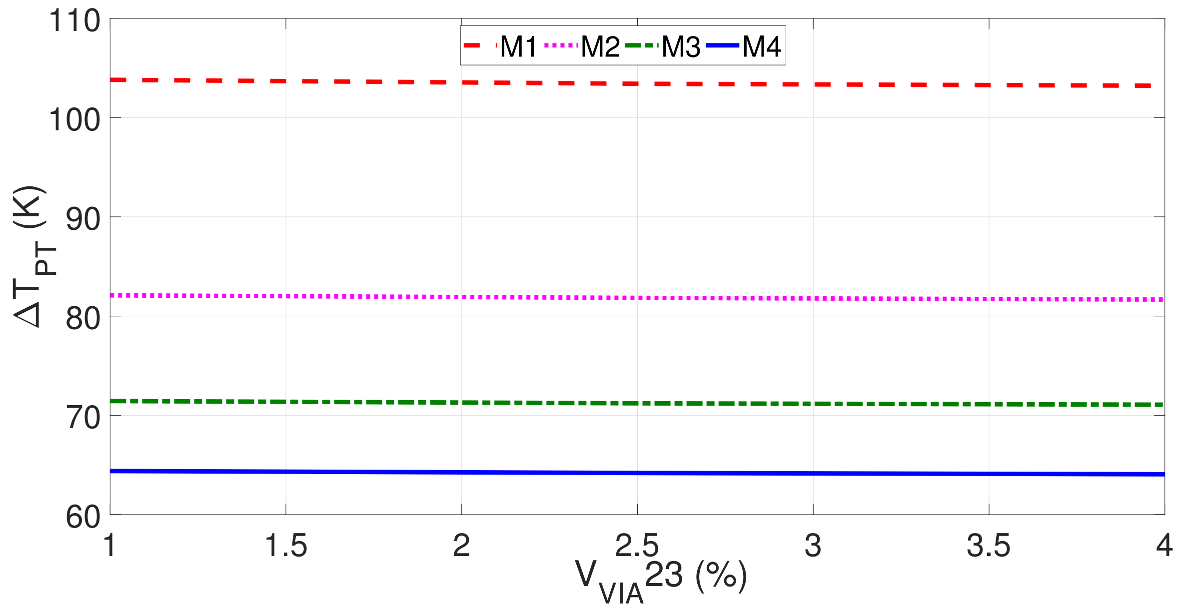

Figure 6.27 – ΔT_{PT} in local layers for different fractions of $V_{VIA}23$ for P_T = 500 W/m.

the highest temperature variation, a significant difference of 20 K and 30 K higher than the M2 and M3 layers, respectively.

6.4.2 Effective Thermal Conductivity of the BEOL

Figure 6.28 shows the effective thermal conductivity of the vias layers (k_{eff}^{VIA}) in FreePDK45 technology, given by (2.10), as a function of their volume fraction (V_{VIA}) for V_{INT} of 30%, k_m = 401 W/(m.K) and k_i = 1.4 W/(m.K). A typical V_{VIA} value from

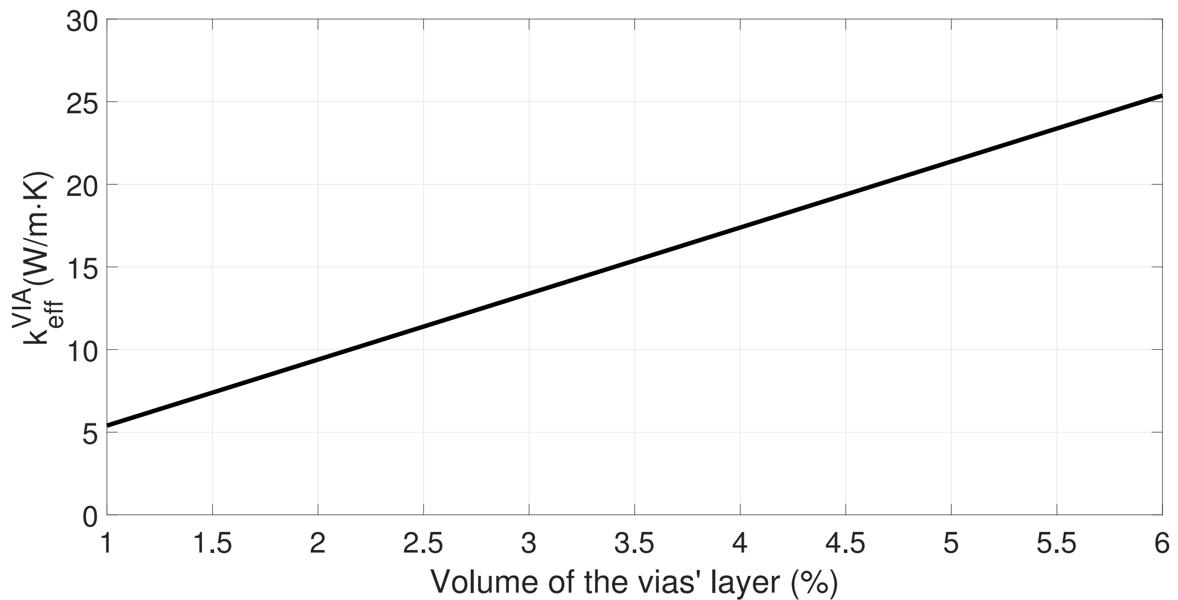

Figure 6.28 – Effective thermal conductivity variation of the via layers as a function of the via volume fraction.

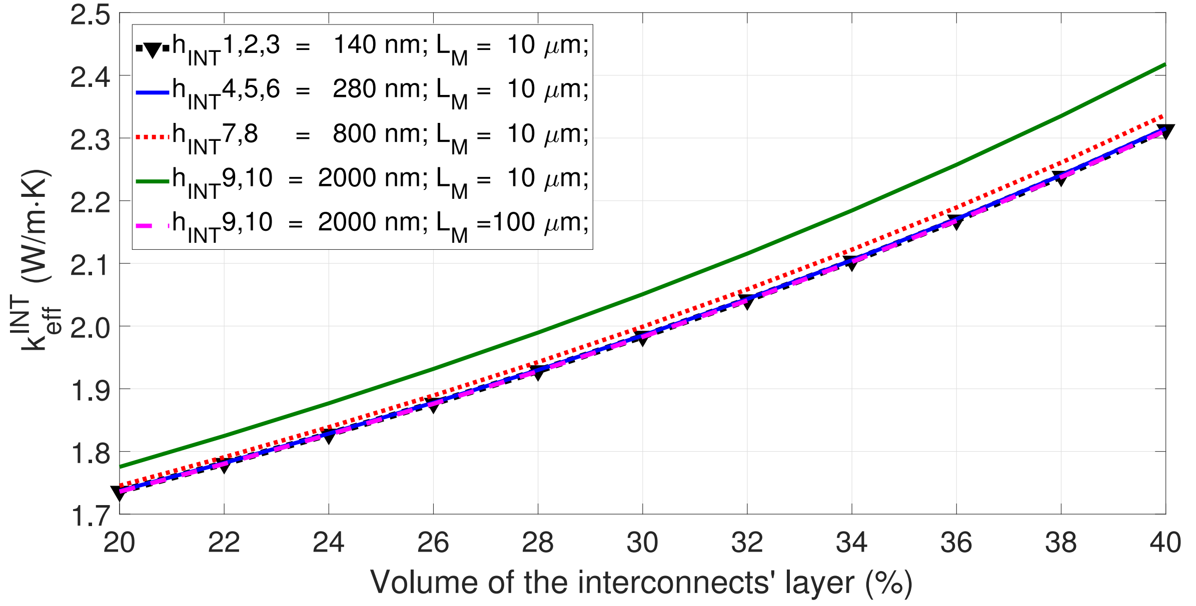

Figure 6.29 – Effective thermal conductivity variation of the interconnect layers as a function of volume fraction.

1% to 6% is considered [133]. The k_{eff}^{VIA} increases with a larger V_{VIA}, obtained with the addition of more vias in the BEOL. For example, a thermal conductivity of 7.4 W/m.K is obtained for a V_{VIA} of 1.5%. Increasing V_{VIA} to 2.5%, which corresponds to an increase of 66% in the number of vias, k_{eff}^{VIA} is increased to 11.4 W/m.K, 54% higher. This proves the importance of the number of vias in the k_{eff}^{VIA} and, consequently, in the temperature distribution. In this case, all the layers have the same conductivity value, as their shape is similar, with the same volume fraction of metallic and isolating materials.

Figure 6.29 shows the effective thermal conductivity of the interconnect layers (k_{eff}^{INT}) as a function of the volume fraction (V_{INT}). k_{eff}^{INT} increases for a larger V_{INT}, which is obtained by enlarging the lines of the BEOL. The evaluated technology has lines with four different thicknesses, as described in Table 6.6, resulting in four k_{eff}^{INT} variations. The global layers, M9 and M10, with dimensions of 10 μm have the largest height, 2000 nm. For a V_{INT} variation from 26% to 36%, the thermal conductivity from M9 given by (2.11) increases from 1.93 to 2.25 W/m.K, a change of 16.5%. The k_{eff}^{INT} for the global layers with dimensions of 100 μm have a lower change, as the aspect ratio increase 10 times, given by (F.7). For a V_{INT} variation from 26% to 36% the thermal conductivity of M9 increases 15.6%. Note that the local layers, M1, M2 and M3 also suffer a significant variation. Comparing with the via layers, the interconnect layer has a smaller influence on the thermal distribution, as the k_{eff}^{VIA} is higher than k_{eff}^{INT}.

Figure 6.30 shows the effective thermal conductivity of the BEOL (k_{eff}^{BEOL}) varying with the volume fraction of the lines (V_{INT}) and vias (V_{VIA}). It should be noted that the impact of the vias number on the BEOL thermal conductivity is more significant

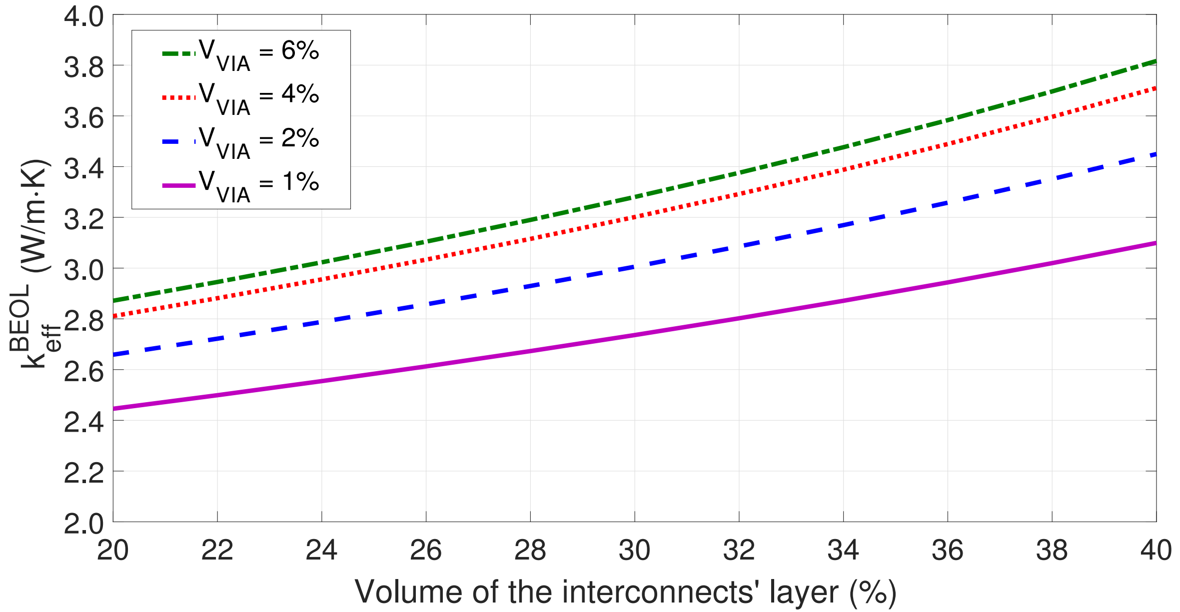

Figure 6.30 – Effective thermal conductivity variation of the BEOL as a function of interconnect layer volume fraction for various via layer volume fraction.

when V_{VIA} changed from 1% to 2% than the doubling from 2% to 4%. Considering a V_{INT} of 26%, in the first case k_{eff}^{BEOL} increases from 2.61 to 2.85 W/m.K, an increase of 9.2%. In the second case, it varies from 3.03 to 3.1 W/m.K, a lower change of 2.3%. This analysis indicates that an excessive number of vias does not necessarily result in a significant gain for the thermal conductivity of the BEOL. On the other hand, the impact of V_{INT} becomes higher for the BEOL with a larger V_{VIA}. Considering, for example, a situation with 1% of V_{VIA}, the k_{eff}^{BEOL} increases only 0.33 W/m.K or 12.6% for a V_{INT} increase from 26% to 36%. In a second situation, with a 6% of fraction volume of vias, the change in k_{eff}^{BEOL} is of 0.48 W/m.K, or 15.4%. These results suggest that the number of vias in each layer can be sized to allow a higher thermal conductivity in BEOL and then a better temperature distribution.

6.4.3 Temperature Change of the Local Layers with Volume Fraction Variation on All Layers

Differently from Sub-section 6.4.1, where the via and the metallic layer volume fraction change is considered for only one layer, in this section the volume fraction variation in all layers of the BEOL is analyzed.

Figure 6.31 shows the temperature variation of each of the 10 layers in the 45 nm technology calculated by (2.8). A k_{eff}^{BEOL} simulated before with V_{VIA} equal to 1% and 6% and V_{INT} of 20% and 40% is considered here. The modes A, B, C and D have V_{INT} equal to 40%, 40%, 20%, 20% and V_{VIA} equal to 6%, 1%, 6%, 1%, respectively,

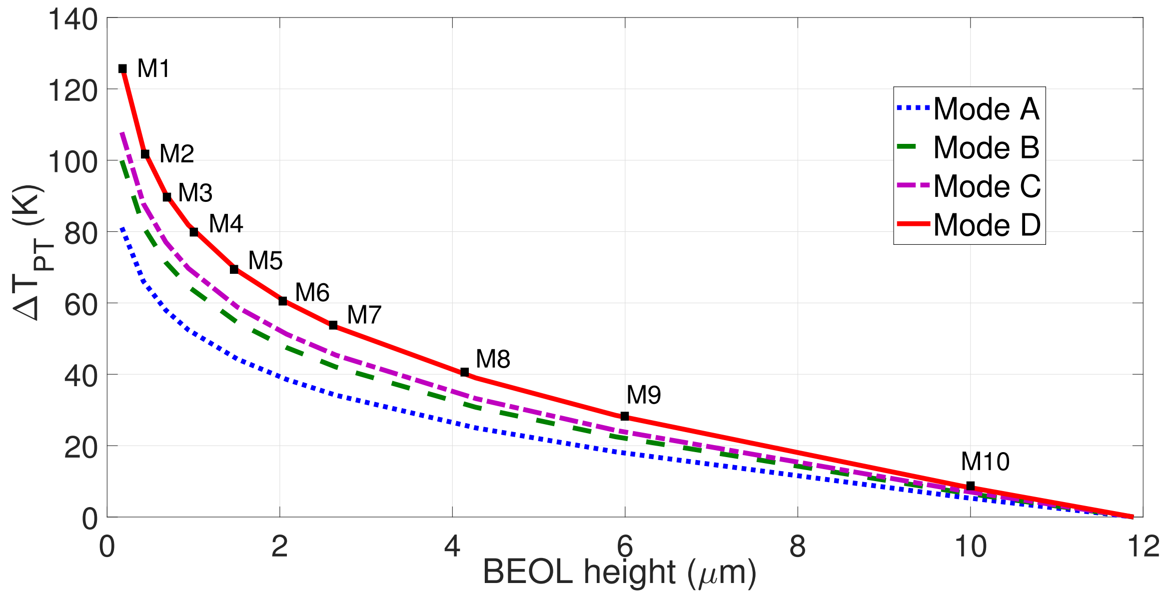

Figure 6.31 – Temperature variation in the BEOL layers for a 45 nm technology due transistors self-heating for a dissipated power of 500 W/m.

Table 6.7 – The modes A, B, C and D used to evaluate the ΔT_{PT}.

Mode	A	B	C	D
V_{VIA}(%)	6	1	6	1
V_{INT}(%)	40	40	20	20

as summarized in Table 6.7. The conditions for mode A yield the lower temperatures in the BEOL, mainly in the local interconnects (M1, M2, and M3). Mode D represents the worst case, resulting in the highest temperatures. Note that the temperature at the top of BEOL, whose height is 11.89 μm, has a small variation. On the other hand, the layers close to the FEOL undergo very significant temperature variations. Interestingly, even for a higher layer such as M9, the temperature change of 28.5 K (28.5°C) for mode D is a significant value.

Figure 6.32 illustrates two cases of ΔT_{PT} differences due the power dissipated by transistors ($DIFF(\Delta T_{PT})$): 1) between the modes D and C; 2) between the modes D and A. Observe that in the first case, the temperature in the local and intermediate lines reduce significantly. M1 for example, has a temperature reduction of 19.5 K. Considering the second case, an extra reduction is obtained with a larger volume of metal (40%), the M1 temperature decreases by 45 K. The presence of additional vias and enlarged lines allows a better temperature distribution, and the layers nearest the transistors are the most benefited ones.

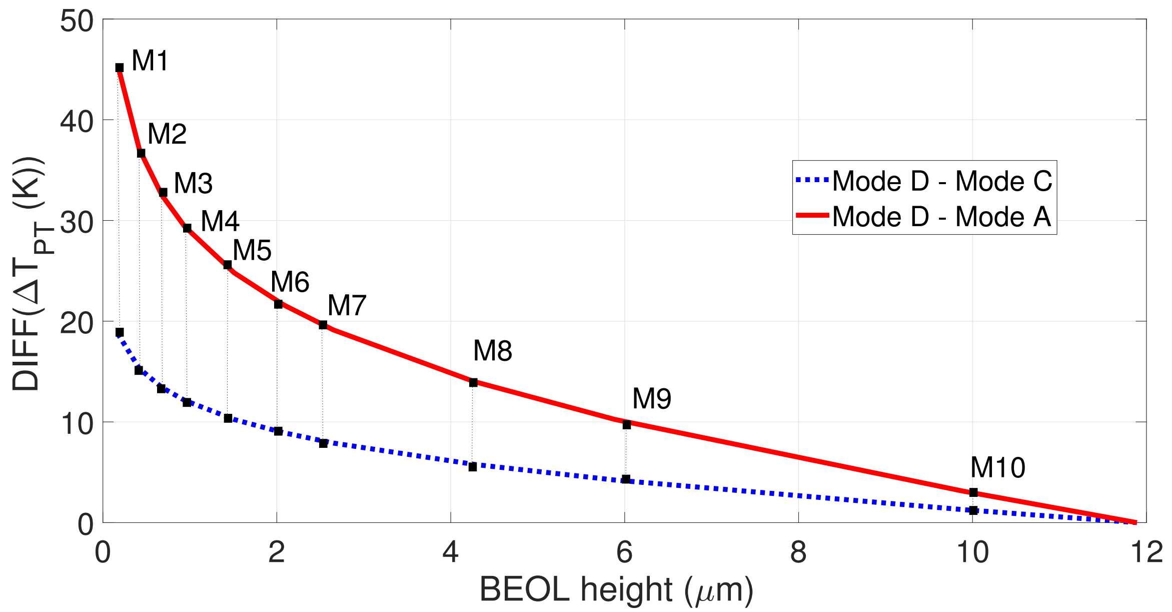

Figure 6.32 – Temperature variation difference in the BEOL layers for two cases of volume via and interconnect variation for $P_T = 500$ W/m.

6.5 Comparision of Technologies and the State of the Art

In this section, a comparison of the expected temperature distribution on the metallic layers of different technologies, namely the 45 nm, 22 nm, 14 nm, and 10 nm is presented. In particular, we discuss the results for the 10 nm node, which is the state-of-the-art technology. As expected, the technologies with smaller dimensions suffer a larger temperature change and, consequently, the EM becomes more critical as the interconnects' lifetimes are shortened [217–220].

Figure 6.33 shows the minimum interconnect pitch of the latest technologies. The Intel 10 nm process has an interconnect pitch of 36 nm, 1.44 times smaller than the Intel 14 nm and 2.22 times smaller than the Intel 22 nm [44, 221, 222]. The minimum interconnect cross-sectional area for these technologies is shown in Figure 6.34. While the copper lines dimensions are significantly reduced in each technology node, the thickness of the diffusion barriers does not scale as fast [153, 223–226]. For example, the Intel 14 nm technology has the minimum metal width of 28 nm, 1.57 times smaller than the Intel 22 nm [227, 228]. In turn, these technologies have a TaN/Ta diffusion barrier/liner close to 2-3 nm [228]. Since the diffusion barrier does not scale as the metal lines, the barrier occupies an increasing volume portion of the lines and the wires become more resistive.

Figure 6.35 shows the temperature variation of the metallic layers for the different technologies, considering a power dissipation of 200 W/m. Here, we apply (2.8) for a metal and a via volume fraction of 32% and 4%, respectively. As expected, the layers that are closer to the transistors undergo a more significant temperature increase.

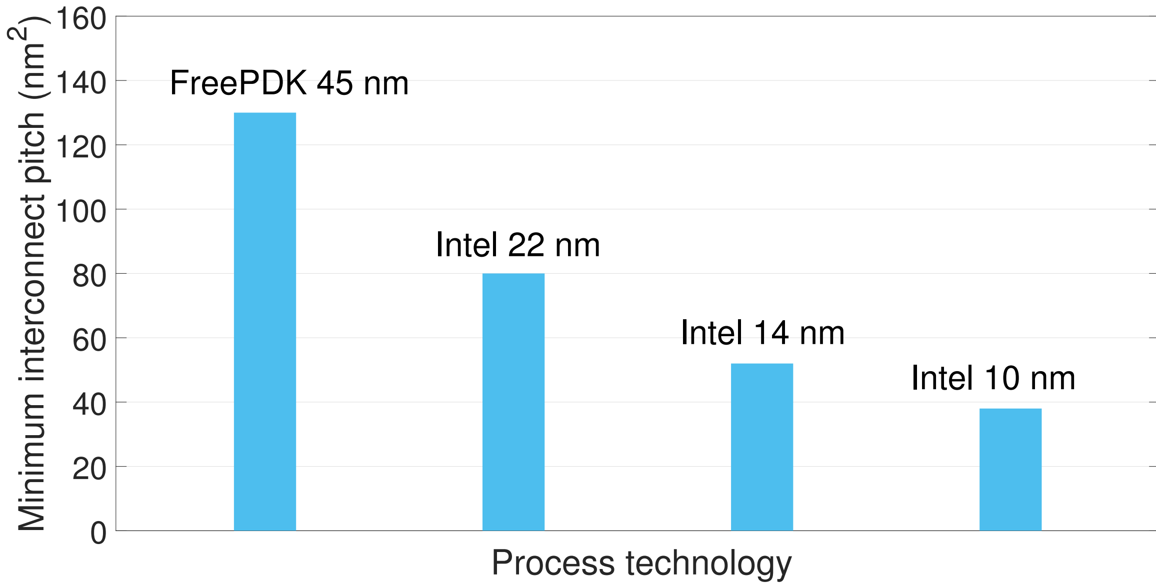

Figure 6.33 – Minimum interconnect pitch of modern technologies [44, 171, 221, 222].

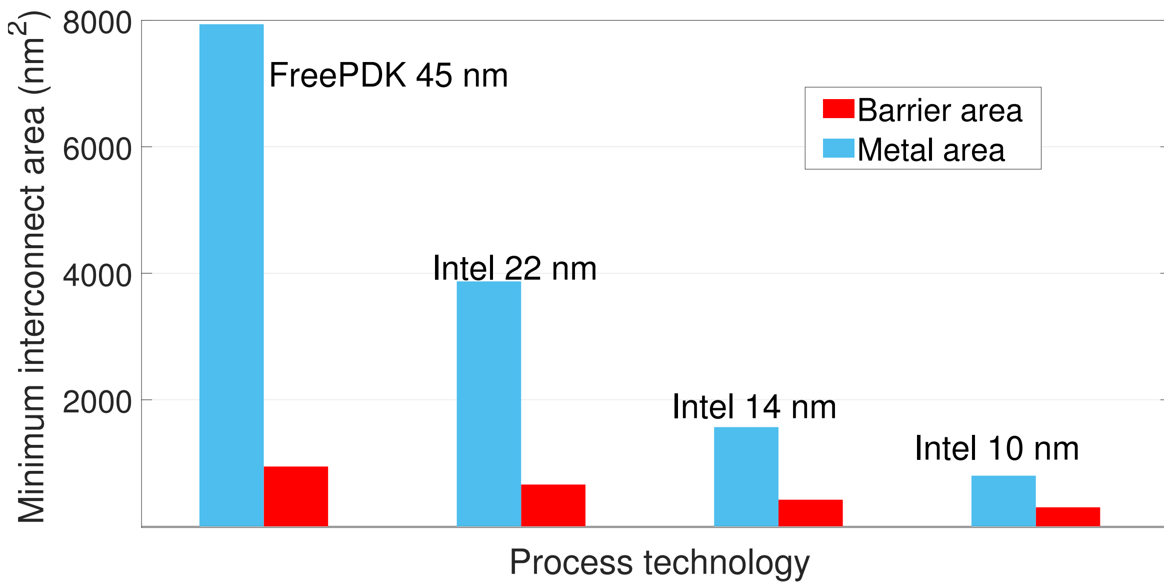

Figure 6.34 – Minimum interconnect cross-sectional area of modern technologies [229].

For the Metal 1 of the Intel 10 nm, the ΔT_{PT} is 75 K, 12 K higher than in the Metal 2. Even in the Metal 4, we observe a large increase of 54 K. For comparison, the ΔT_{PT} in Metal 1 of the Intel 14 nm technology is 18 K lower than in the Intel 10 nm process. A more significant difference is obtained comparing with the FreePDK 45 nm. In this case, the ΔT_{PT} difference is 34 K, for the Metal 1 and 30 K for the Metal 2 layer. It is important to mention that in this comparison, we consider the same power dissipation on the FEOL. In a real situation, the new technologies operate with a large density of transistors, with each transistor individually dissipating a lower power when compared with the older technologies.

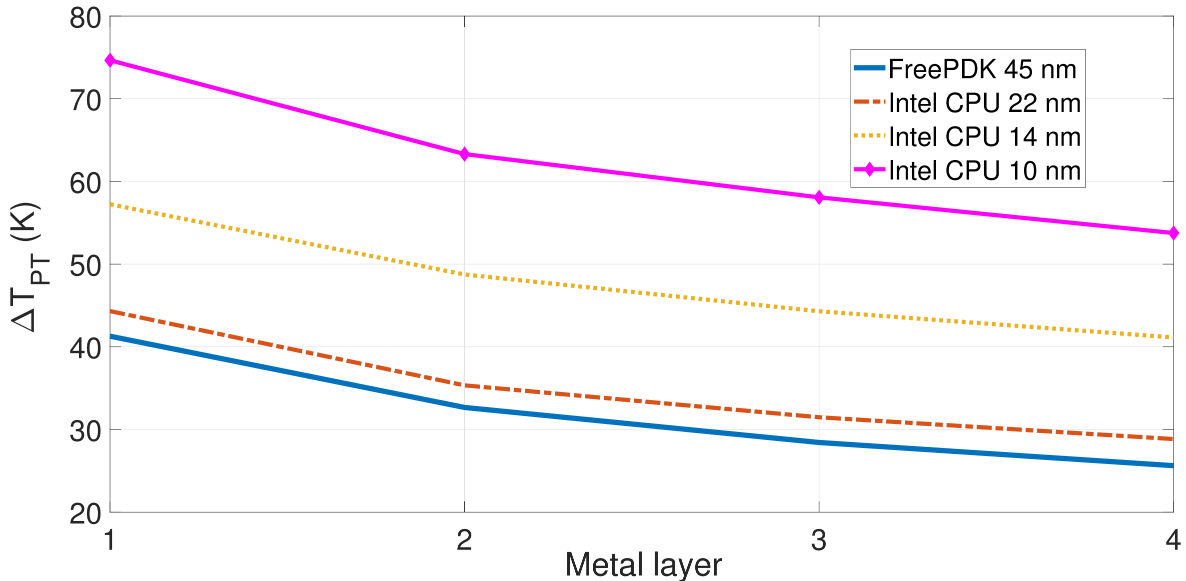

Figure 6.35 – Temperature change of the metallic layers for different technologies. A power dissipation of 200 W/m is considered.

A high temperature affects the performance of a circuit leading to changes in the transistors operation and to increase the metal lines resistance. The lines resistance is expected to be larger as the dimensions reduce in each new technology. However, in addition, the temperature increases the lines resistance even more, which strongly affects the power consumption, operation frequency, and signals delay of circuits. The temperature increase due to the Joule heating and to the dissipated power from transistors makes the circuit operation slower.

Figure 6.36 shows the $\Delta R/R_0$ variation of the Metal 1 interconnects due to the EM considering the temperature increase from Figure 6.35. Here, (2.14) is applied for a current density of 2 MA/cm^2, an activation energy of 1.0 eV, and resistivity of the Ta/TaN and the Cu of 60 $\mu\Omega$-cm and 1.7 $\mu\Omega$-cm, respectively. Note that with the technology evolution, the $\Delta R/R_0$ increase becomes more and more pronounced with time. In particular, for the 10 nm technology, the resistance increase is significantly larger. The $\Delta R/R_0$ increase is a consequence of the higher ΔT_{PT} and the thinner Ta/TaN barrier.

Figure 6.37 shows a comparison between the estimated lifetimes of the Metal 1 for different technologies, where the MTTF of the FreePDK 45 nm is normalized to 1. The MTTF reduces to 0.2 in the 10 nm technology, a significant reduction of 80%. As the MTTF reduces 60% after each line interconnect scaling, the lifetime improvement is a priority for the next technology nodes. These results indicate that EM failures become a more serious issue with the interconnect scaling, which agrees with the experimental observation.

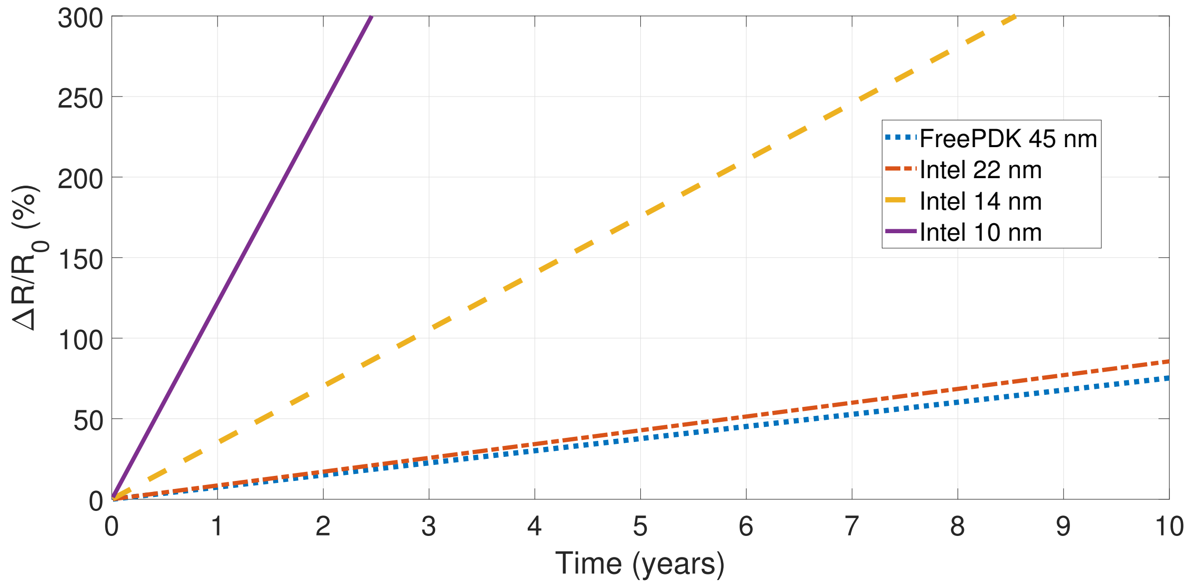

Figure 6.36 – $\Delta R/R_0$ variation of the Metal 1 lines of modern technologies considering the temperature increase from Figure 6.35.

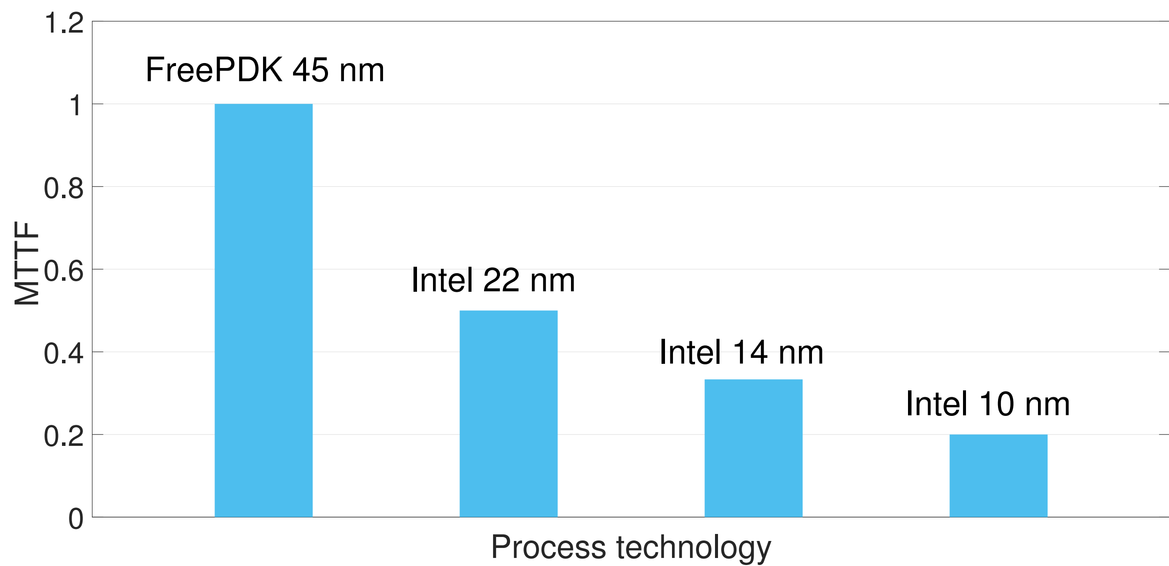

Figure 6.37 – Mean-time-to-failure of interconnects of modern technologies under a current density of 2 MA/cm^2.

The above analysis makes clear that Cu poses severe limitations to further improve interconnects performance and reliability. The Cu limitations drive the research to new materials, such as Co and Ru, as alternative metals to replace Cu lines. As Intel has already announced, the Co filling improve the performance and reliability, at least for the local interconnect lines which have very narrow pitches [60].

7 Conclusion and Outlook

Electromigration induced failure is one of the main reliability issues for the microelectronics industry. Since its detection as a potential damage mechanism in metallization of integrated circuits, the semiconductor industry has made efforts in order to design more resistant interconnects against EM. The continuous scaling of the metal lines geometry leads to higher current densities through the lines and higher temperatures, which accelerates the EM failure process. As a consequence, the new technology nodes require the development of new fabrication processes, the research of materials which yield adequate properties, and the design of specific geometrical features to improve the reliability of the lines.

The continuous reduction of the metal line dimensions in the new technology nodes is accompanied by an increase in the density of interconnections in modern integrated circuits. Therefore, the scaling of the line geometry and the reduction of the distance between transistors and metal layers make the lines to operate at high temperatures and conduct high current densities, accentuating the atom displacement due EM. As a consequence, the EM becomes more challenging for the development of the new nodes and the lifetime of interconnects have decreased from generation to generation, despite all the knowledge gained and efforts made since 1960.

In order to study interconnect failure behavior the use of accelerated EM tests is necessary, in which the lifetime of an interconnect can be reduced by either increasing the current density and/or by increasing the temperature. Since EM tests are conducted at elevated temperatures and current densities, extrapolations are needed to assess reliability at operating conditions. The maximum current density supported by the lines are determined and used as criterion to design the interconnects of the integrated circuits. The Blech product is another criterion to check if the interconnects are prone to failure as a function of the current density and the interconnect length.

The EM analysis for integrated circuits is challenging and limited by the conventional EM criteria. Moreover, the peculiarities of each circuit and the process variation creates more uncertainty to the EM analysis. However, the performance of a circuit is not necessarily affected by such a criterion and a more complex analysis is required to relate the interconnect and the circuit reliability. Therefore, an investigation of the EM impact on the circuit operation as an interconnect resistance changes is crucial for a circuit reliability evaluation.

The evaluation of a chip performance degradation due to the EM allows the designer to identify more accurately if the chip performance is satisfactory, even if the interconnect lines operate with an elevated current density or to verify if a single line is critical even when operating with a current density which is below the maximum one given by the foundry's rule. To evaluate the EM, the resistance change of the lines has to be calculated considering mainly the temperature and the current density. With the EM evolution, the circuit performance changes. Nevertheless, as the EM evolution is an extended time process, the circuit can operate with the interconnects suffering a large resistance change and still maintain an adequate performance.

We applied the proposed resistance change method to investigate the EM on the performance of an operational amplifier. We observed that some interconnects can operate with large current densities, larger than the maximum acceptable by the technology. Yet, they still do not have a significant influence on the IC performance as a whole. Other lines, however, can have a larger impact on the performance, even though they carry a current density which is below the technology limit. This shows the importance of computing the resistance change to understand the EM impact on the circuit performance.

An adequate estimation of the temperature distribution on the circuit and on the interconnect structure is essential to a better understanding of the interconnect reliability. This is accomplished by estimating the temperature of each layer of the BEOL. The temperature estimation becomes more relevant for the new technologies which have reduced pitches and are more compact, so the BEOL experiences a higher temperature due to self-heating of the transistors. Such a temperature distribution is of great importance to the IC and layout designer, and has to be considered for the performance evaluation at circuit level.

A method to calculate the temperature distribution on the BEOL structure and its impact on the EM in a design environment has been developed and implemented in MATLAB. The study for a 45 nm technology indicates a large temperature variation from the local to the global interconnects, which should be considered for the EM induced resistance increase of the interconnects, in contrast to the standard analysis through a fixed operation temperature throughout the BEOL.

An accurate analysis of the temperature distribution on the interconnect structure is essential to a better assessment of the interconnect reliability. Therefore, a model to compute the temperature on each metallization level of the interconnect structure is implemented. The temperature distribution on the metallization layers of different technologies is investigated. It is shown that the temperature in the Metal 1 of the Intel 10 nm can increase by 75 K, 12 K higher than in the Metal 2. As expected, the layers that

are closer to the transistors undergo a more significant temperature increase.

The importance of investigating the temperature distribution on the BEOL becomes more evident for the new technologies, in particular for the state of the art 10 nm technology node, which operates under a higher current density and temperature. This leads to an accelerated EM and, consequently, a significant reduction of the interconnect lifetime. Thus, EM failures become a more serious issue with the interconnect scaling, which agrees with the experimental observation. The results indicate clear that Cu poses severe limitations to further improvement of the interconnects' performance and reliability. This has driven the research of new materials, such as Co and Ru, as alternative metals to replace Cu, at least for the smallest interconnect layers.

We have developed a tool to calculate the resistance change and the temperature on the BEOL metallization to evaluate the electromigration in integrated circuits at design level. We have implemented methods which allow to: 1) evaluate the IC performance degradation; 2) identify the critical lines; 3) size the dimensions of interconnects; 4) determine the lifetime of the circuits.

When applied to evaluate the performance change of a ring oscilator, a bandgap voltage reference circuit and an operational amplifier, we observed the importance of the resistance change criterion to obtain a more accurate EM analysis. While the traditional methodology based on the Blech criterion indicates that longer lines are more critical, the shorter ones are the bottleneck, being more sensible to small resistance variations.

The tool was applied to study the impact of the electromigration on the performance of an operational amplifier. Some interconnects were classified as critical due to the large current density they carry, above the maximum limit set by the technology. The most surpreendent is that it was identified lines that normally are not critical, nevertheless degrades the performance significantly, leading to reduction of the voltage gain and voltage swing, of about 30% and 14% in 1.2 and 5 years.

This work brings the study of the reliability of the interconnects and ICs to the design stage, which allows the evaluation of the circuit performance degradation within an electromigration environment. The proposed tool allows the designer identify the critical interconnects which would not be detected using the maximum current density criteria, leading to more reliable analysis. In summary, the proposed tool identified that from the 20% paths with a critical current density, only 3% degrades significantly the circuit performance.

We used a model to represent the resistance change of the lines due to the void growth after it reaches the barrier of the lines. Nevertheless, there are still several points which should be improved, and they are suggestions for future work. From the

EM resistance change model a natural extension of this work is to develop a model which incorporates the period before the void reaches the barriers, i.e. the void nucleation phase. This is a challenging task, since the void nucleation problem requires the consideration of additional physical phenomena.

From the temperature change model an interesting improvement is to consider the joule heating effect. This will provide a more accurate temperature estimation and the electromigration lifetime, which can ultimately contribute to better lifetime estimation of the circuit.

7.1 Future work perspectives

An experimental work to calibrate and to refine the models and the parameters is important to validate the methodology. The automations of the simulation flow to obtain the circuit performance curves and of the method to obtain the maximum resistance change ratio for each interconnect line has to be developed, giving a more accurate and faster analysis. The application of this work in a professional circuit design could brings challenges to mainly to reduce the time and cost of the analysis.

7.2 Publications

Scientific Journals

- Nunes, R. O. and R. L. de Orio. "Effect of Lines and Vias Density on the BEOL Temperature Distribution." Journal of Integrated Circuits and Systems 14 n.2 (2019): 1-9. DOI: 10.29292/jics.v14i2.63
- Nunes, R. O. and R. L. de Orio. "Study of the impact of electromigration on integrated circuit performance and reliability at design level." Microelectronics Reliability 76 (2017): 75-80. DOI: 10.1016/j.microrel.2017.06.027

Conference Proceedings

- Nunes, R. O., J. L. R. Bohorquez, and R. L. de Orio. "Analysis of Vias Position on the BEOL Temperature Distribution." 2019 Latin American Electron Devices Conference (LAEDC). Vol. 1. IEEE, 2019. DOI: 10.1109/LAED.2019.8714745
- Nunes, Rafael Oliveira, and Roberto Lacerda de Orio. "Effect of Lines and Vias Density on the BEOL Temperature Distribution." 2018 33rd Symposium on Micro-

electronics Technology and Devices (SBMicro). IEEE, 2018. DOI: 10.1109/SBMicro.2018.8511319

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APPENDIX A – Resistance Change of a Metal Line due to EM

Figure A.1 shows a Cu interconnect with a TaN barrier under EM. Figure A.1(a) shows a small void nucleated in the metal, while Figure A.1(b)-(d) show the void growth through the metal line. When the void reaches the barrier layer at a time t_1, as shown in Figure A.1(c), the current is forced to pass through a portion of the barrier layer, l_{EM}. As the void continues to grow the path through the barrier increases. Since the barrier layer has a much higher resistivity then the Cu, the resistance of the interconnect line increases.

The drift velocity of metal atoms is calculated by [115]

$$v_{EM} = \frac{D(T)\,|Z^*|\,e\rho(T)j}{kT}, \tag{A.1}$$

where $D(T)$ is the copper diffusivity, Z^* is the effective valence, e is the electric charge,

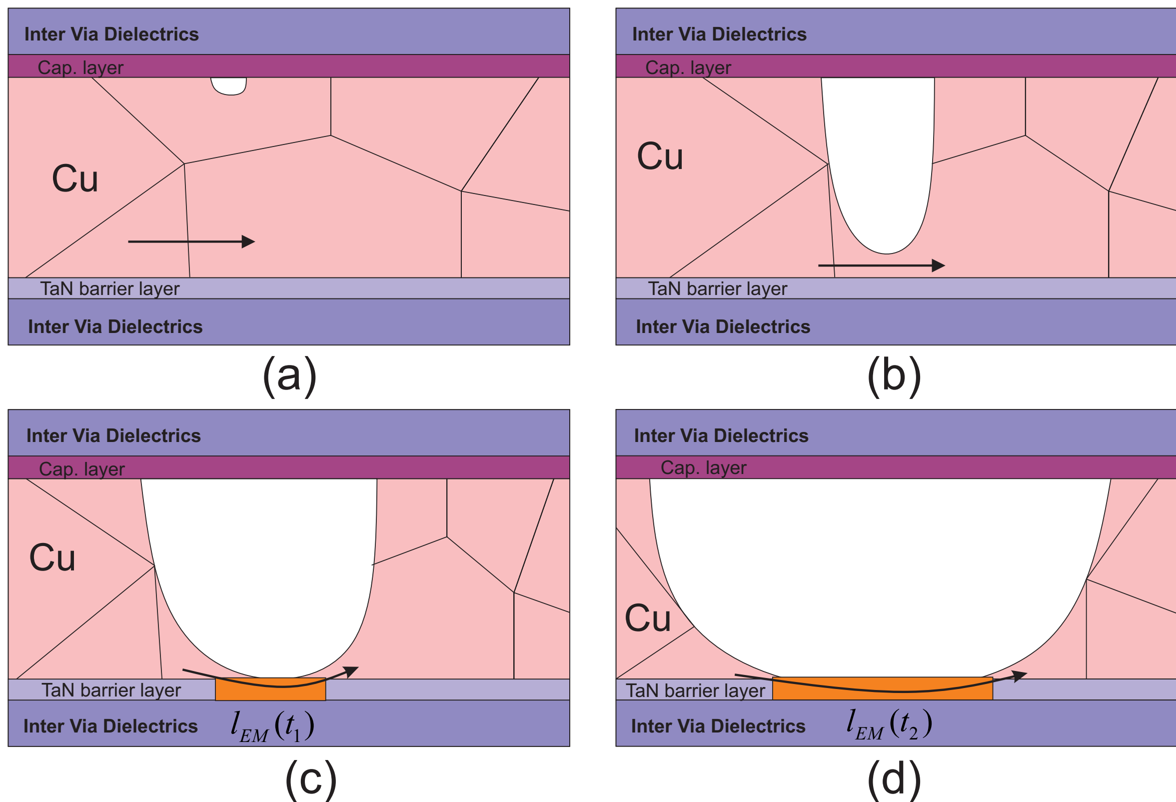

Figure A.1 – Void growth in a interconnect. (a) Initial nucleated void. (b), (c), and (d) Void growth through the metal until it reached the barrier layer.

$\rho(T)$ is the resistivity from line, j is the current density, T is the temperature, and k is the Boltzmann constant.

The drift velocity can be also expressed by

$$v_{EM} = \frac{l_{EM}}{\Delta t}, \tag{A.2}$$

where Δt is the time interval at which the current passes through the TaN barrier.

From (A.1) and (A.2) the l_{EM} is given by

$$l_{EM} = \frac{D\,|Z^*|\,e\rho j\Delta t}{kT}. \tag{A.3}$$

The initial resistance of the Cu line is given by

$$R_0 = \frac{\rho L}{A}, \tag{A.4}$$

where L is the length, A is the cross-sectional area and ρ is the resistivity of the line.

After the void reaches the barrier, the resistance and resistance change (ΔR) of the line are calculated by

$$R = \frac{\rho L}{A} + \Delta R, \tag{A.5}$$

and

$$\Delta R(t) = \frac{-\rho l_{EM}(t)}{A} + \frac{\rho_b l_{EM}(t)}{A_b}, \tag{A.6}$$

where A and A_b are the Cu and TaN cross-sectional areas and ρ and ρ_b are the resistivities of the Cu and TaN, respectively.

As the TaN resistivity is higher than the Cu resistivity, and the TaN cross-section is significantly smaller than the Cu cross-section, (A.6) can be reduced to

$$\Delta R(t) = \frac{\rho_b l_{EM}(t)}{A_b}. \tag{A.7}$$

From (A.3) and (A.7), the ΔR of a line due to EM is given by

$$\Delta R(t) = \frac{De\rho \left| Z^* \right| \rho_b j \Delta t}{k A_b T}. \tag{A.8}$$

From (A.8) and (A.4), the ratio between (ΔR) and the initial resistance (R_0) is calculated by

$$\frac{\Delta R(t)}{R_0} = \frac{De \left| Z^* \right| \rho_b I \Delta t}{k A_b T L}. \tag{A.9}$$

APPENDIX B – Blech Product

Electromigration is the migration of atoms caused by the electrostatic and the "electron wind" forces on a metal. Figure B.1 illustrates the forces forces in a top view from an interconnect. A direct electrostatic force results from atoms and electrons interactions. The conducting electrons are scattered by the atoms resulting in a momentum transfer called "wind force". The resultant force is given by [230]

$$F = Z_{eff} e E, \tag{B.1}$$

where e the electric charge, E is the electric field, and Z_{eff} is the so-called effective valence corresponding to the forces. The electric field is given by

$$E = \rho j, \tag{B.2}$$

where ρ is the metal resistivity and j is the current density.

The atomic flux resulting from the EM driving forces is given by [177]

$$J_{EM} = N \mu F, \tag{B.3}$$

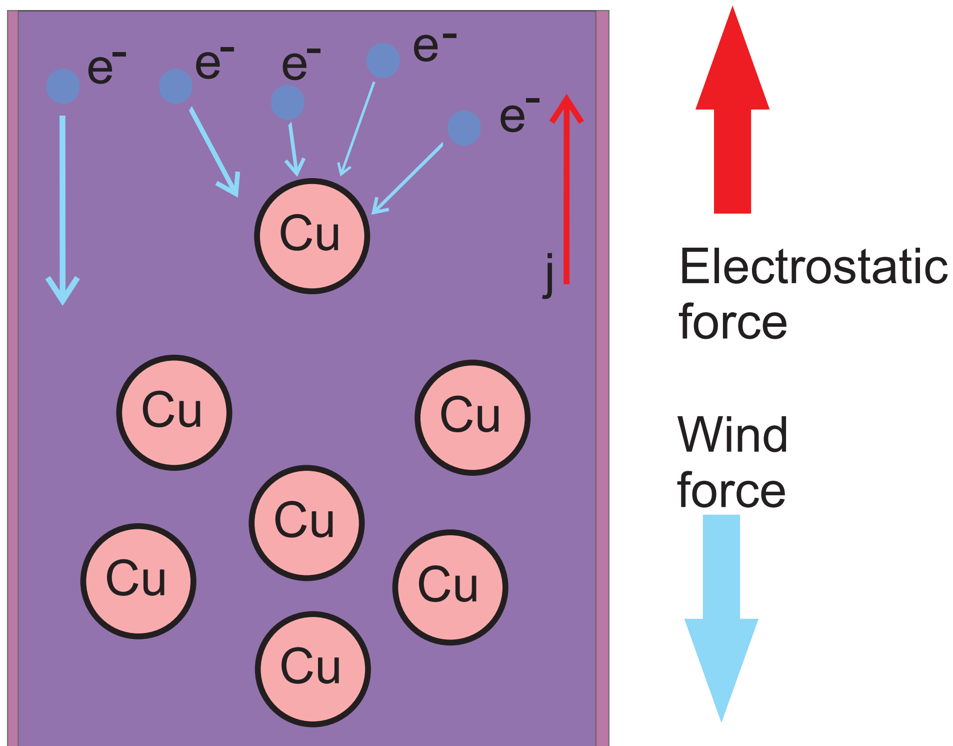

Figure B.1 – Illustration of electrostatic and "electron wind" forces on a metal.

where N is the atomic density and μ is the mobility of the metal ions according to the Einstein relation [231]

$$\mu = \frac{D_{eff}}{kT}, \tag{B.4}$$

where D_{eff} is the effective diffusivity of the metal ions, k is Boltzmann's constant and T is the temperature.

From (B.4) and (B.3) the atomic flux is calculated by

$$J_{EM} = \frac{N \cdot D_{eff}}{kT} Z_{eff} e \rho j, \tag{B.5}$$

where the drift velocity of the ions (v_d) is formulated by

$$v_d = \mu F = \frac{D_{eff}}{kT} Z_{eff} e \rho j. \tag{B.6}$$

Blech observed that the atoms displaced create a stress gradient between the end of the lines causing a back-flux in opposition to the EM-induced flux. Figure B.2(a) shows that the electron flow from the cathode to the anode terminals of the segment leads to a compressive stress at the anode and a tensile stress at the cathode terminal. This effect is commonly referred to as the Blech effect [114, 120]. The back-flux due to the stress gradient is given by [232]

$$J_b = -\frac{N D_{eff}}{kT} \left(\Omega \frac{\partial \sigma}{\partial x} \right), \tag{B.7}$$

where Ω is the atomic volume and $\partial \sigma / \partial x$ is the stress gradient along the line.

With the back-flux stress taken into account, the EM-induced flux is given by

$$J_{EM} = \frac{N \cdot D_{eff}}{kT} \left(Z_{eff} e \rho j - \Omega \frac{\partial \sigma}{\partial x} \right). \tag{B.8}$$

At steady state, the electromigration and the stress gradient induced fluxes are equal in magnitude, but with opposing signs, which results in

$$Z_{eff} e \rho j = \Omega \frac{\Delta \sigma}{L}, \tag{B.9}$$

where $\Delta\sigma$ is the stress difference between the terminals of the segment and L is the length

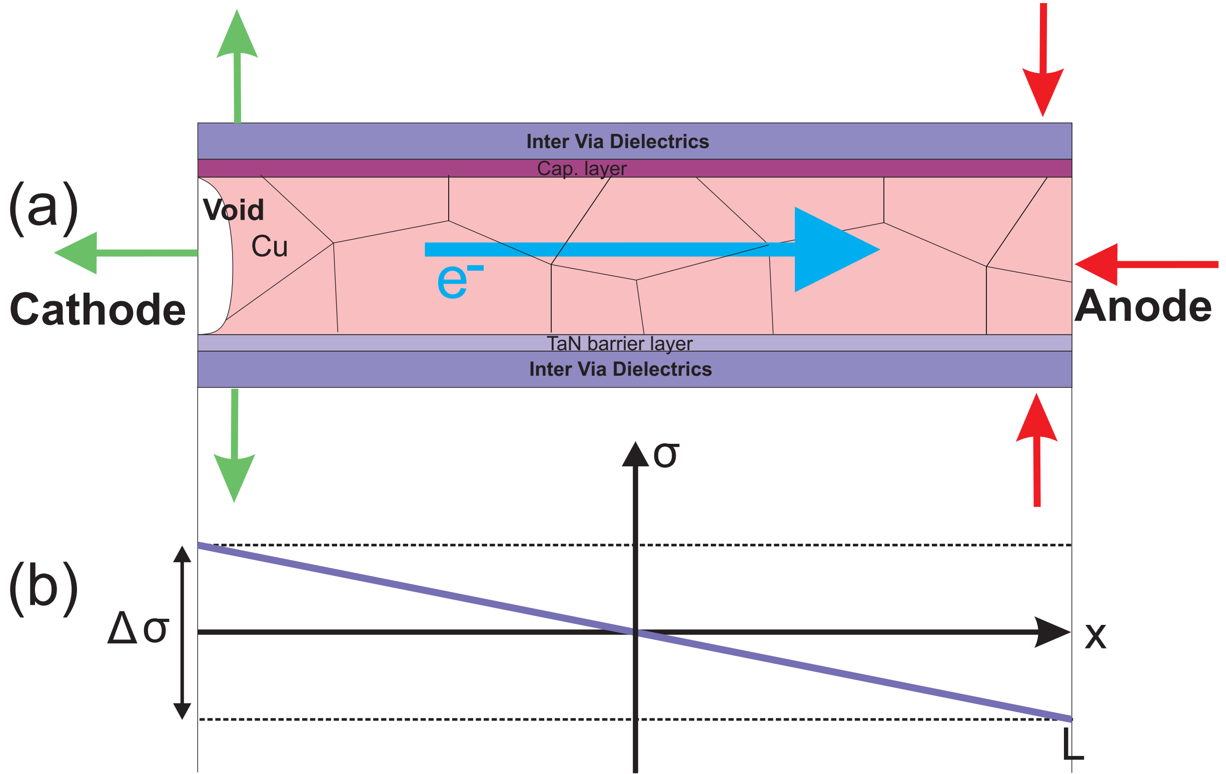

Figure B.2 – The stress difference $\Delta\sigma$ in a segment of length L. The arrows in the line indicates the tensile stress in the cathode and the compressive stress in the anode. Electron flow direction is from cathode to anode.

of the segment. The stress profile is illustrated in Figure B.2(b). At this condition the total mass ceases and the drift velocity is zero. This effect is observed in short lines and thus is referred to as the short length effect.

The Blech effect is explained by the existence of a maximum stress difference $\Delta\sigma_c$ that can be sustained by the interconnect. This implies that a threshold value for jL exists,

$$(jL)_c = \frac{\Omega \Delta\sigma_c}{Z_{eff} e\rho}, \tag{B.10}$$

below which the generated stress is lower than that required one to nucleate a void in the metal. The expression $(jL)_c$ is called the Blech Product. For a given current density, a critical length, or for a given segment length, a critical current density is required to generate the EM damage [114].

From (B.8) and (B.10), the electromigration drift velocity (B.6) is written as

$$v = \frac{D_{eff} Z_{eff} e\rho (j - j_c)}{kT}. \tag{B.11}$$

APPENDIX C – ITRS Roadmap

The International Technology Roadmap for Semiconductors (ITRS) documents the trends of the semiconductor industry for the development of new technologies, including the interconnects. The ITRS was terminated in 2017 and was succeeded by the IEEE International Roadmap for Devices and Systems (IRDS).

Figure C.1 shows the maximum allowed current density (j_{max}) reported by the ITRS from 2014 to 2024, for the technologies from 16 nm to 3 nm [229]. This estimation indicates that in 10 years the j_{max} increases 2.23 times, from 1.68 MA/cm^2 to 3.76 MA/cm^2. Table C.1 shows that for the same period the minimum width, the thickness, and the aspect ratio of the interconnect lines, which is the ratio between the thickness and the width of the line.

Table C.1 – Aspect ratio, minimum wire width, and metal thickness of different technologies.

Year	2014	2016	2018	2020	2022	2024
Technology (nm)	16	14	10	7	5	3
Aspect ratio [229]	1.9	2.0	2.0	2.0	2.1	2.1
Minimum width (nm) [233]	24	19	15	12	10	7
Thickness	45.6	38.0	30.0	24.0	21.0	14.7

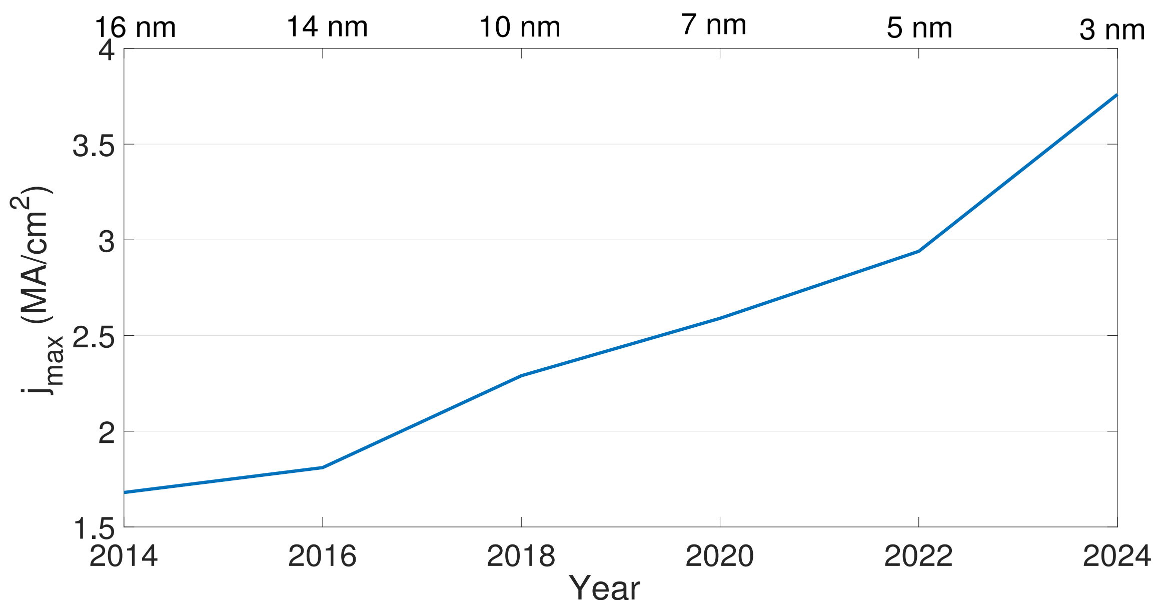

Figure C.1 – Maximum allowed current density prediction of different technologies [229].

Figure C.2 – Maximum allowed current density prediction converted to design nomenclature [229].

Figure C.2 shows the j_{max} converted to the design nomenclature, i.e., the ratio of the current and the width of the interconnect line. Note that the j_{max} for design reduces with the technology advance, as the thickness reduces by a factor of 2.71, larger than the increase of the j_{max} in Figure C.1.

The IRDS suggests that the technology downscaling will continue beyond the 3nm node to the technologies of 2.1 nm, 1.5 nm, and 1.0 nm [234, 235]. Nevertheless, there are limiting issues that can hinder inviable the scaling below 3 nm, in particular the *RC* delay. The RC delay corresponds to the signal propagation delay due to the parasitics of the interconnects.

The reduction of the width and the of the inteconnects has resulted a more resistive line and in an increased capacitance between adjacent metal lines, leading to significant increase of the *RC* delay in the advanced technologies [113, 236–238]. As the scaling has continued, the interconnects have become a bottleneck regarding the performance in most advanced chips.

Figure C.3 shows the effective resistivity of the interconnect metal with the technology advance [229]. For small dimensions, the resistivity of metals is increased due to scattering at interfaces and grain boundaries [239, 240]. Thus, the line resistance per unit length increases even faster than due to geometry reduction.

Figure C.4 shows the evolution of the total length of the interconnects from 2012 to 2026. Figure C.5 shows the evolution of the pitch of the wiring in intermediate layers [229]. From 2020 to 2026 the ITRS estimates an increase of 112% in the intercon-

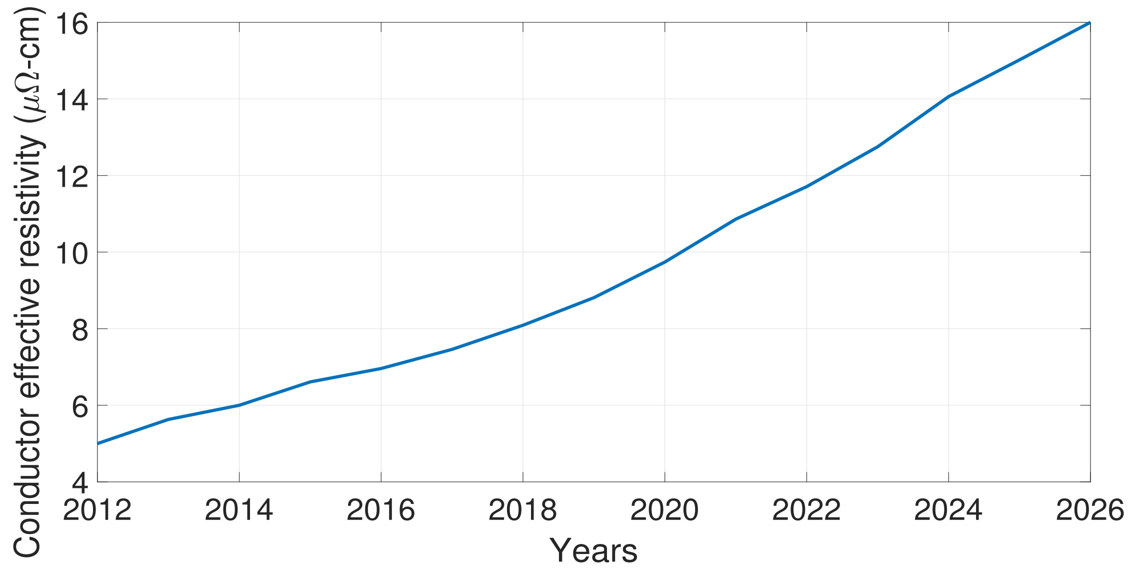

Figure C.3 – Effective resistivity of the metal lines estimated from 2012 to 2026 [229].

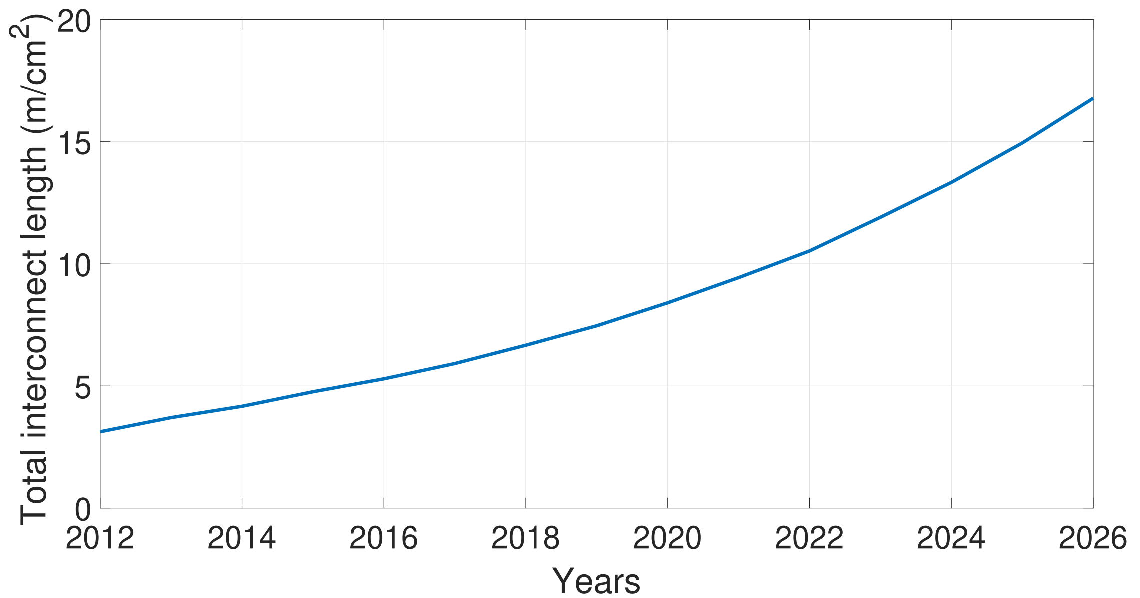

Figure C.4 – Total interconnect length evolution estimated for MPU [229].

nect length in an advanced microprocessor and a reduction of 52% in the pitch of the intermediate interconnect lines. These predictions imply an increase of the resistance and of the capacitance of the interconnects and, consequenty, an increase of the RC delay and of the joule heating.

Figure C.6 shows the thickness of the barrier/cladding estimated by ITRS until 2026 [229]. Such layers are already only 1-3 nm thick and it is very challenging to reduce their thickness further.

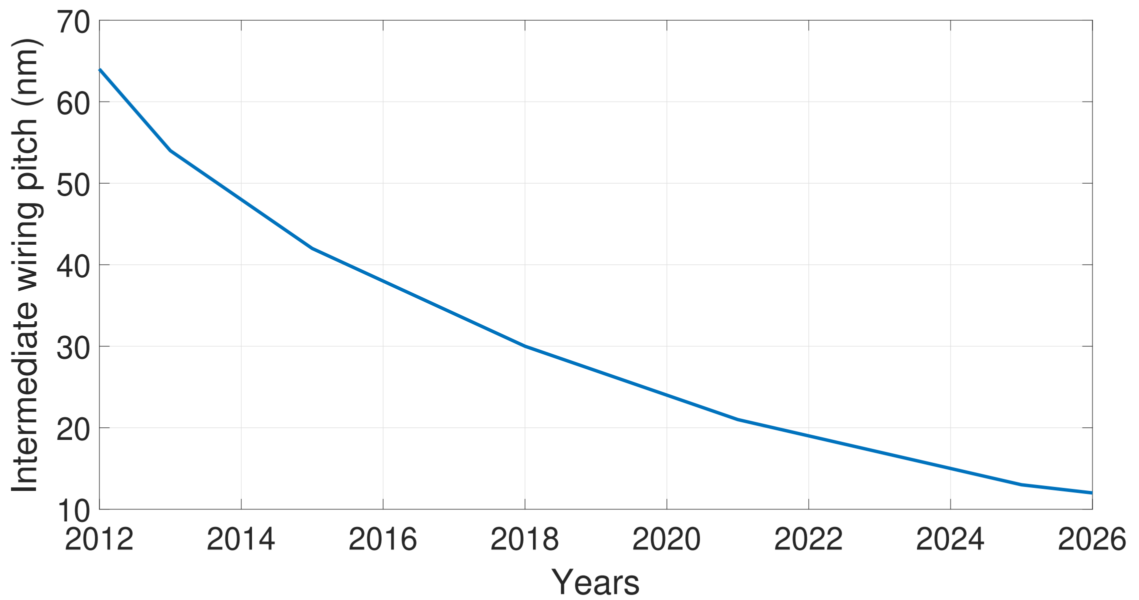

Figure C.5 – Pitch evolution of the intermediate lines estimated from 2012 to 2026 [229].

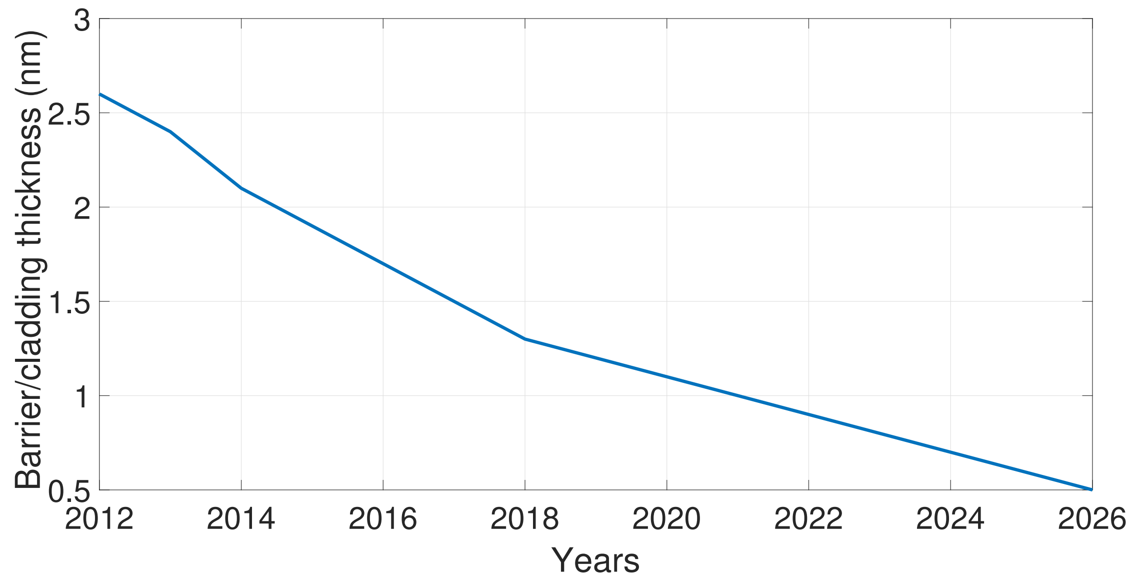

Figure C.6 – Barrier and cladding thickness evolution estimated from 2012 to 2026 [229].

When the wire width becomes thinner than 10 nm, the diffusion barrier occupies a large volume portion of the interconnect, reducing the volume of the main conducting metal. Therefore, the scientists are really looking for materials to replace the barrier or the liner layer. The adhesion with the surronding dielectrics is still an issue. This is not a trivial task since many metals typically show very poor adhesion with dielectrics.

APPENDIX D – Algorithm

```
% Tool to evaluate the critical lines from an integrated circuit due to the
% EM effects
% Fifth  version - 21 february 2020
%-------------------------------------------------------------------------%
clear
clc
%=====================    Input parameters    =========================%
% Input parameters extracted from the PDK, layout and bibliographies to
% calculate the resistance change from the lines.

% -----------------------  Extracted from PDK  ------------------------%

% -------------------    45 nm technology node     ---------------------%
% Contain 11 metal layers - GPDK 45_nm
Hcontact1=120E-9;% Thickness of the contact between transistors and metal 1
L_int0 = [150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 1000E-9
1000E-9 1400E-9 0 0 0]; % Thickness of the interconnects
L_via0 = [150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 150E-9 1000E-9
1000E-9 0 0 0 0]; % Thickness of the vias
L_total0 = sum(L_via0) + sum(L_int0); % Thickness of interconnects and vias
%n1=size(L_int1,2); % Dimension of the interconnect vector
n0=11;
wmin0=[60E-9 80E-9 80E-9 80E-9 80E-9 80E-9 80E-9 80E-9 80E-9 220E-9 220E-9
0 0 0]; % Minimum width from interconnect of 45 nm.


% -------------------    45 nm technology node     ---------------------%
% Contain 10 metal layers - Free PDK45nm

Hcontact1=85E-9;% Thickness of the contact between transistors and metal 1
L_int1 = [130E-9 140E-9 140E-9 280E-9 280E-9 280E-9 800E-9 800E-9 1600E-9
1600E-9 0 0 0 0]; % Thickness of the interconnects
L_via1 = [120E-9 120E-9 120E-9 290E-9 290E-9 290E-9 820E-9 820E-9 2000E-9 0
```

```
0 0 0 0];  % Thickness of the vias
L_total1 = sum(L_via1) + sum(L_int1); % Thickness of interconnects and vias
%n1=size(L_int1,2); % Dimension of the interconnect vector
n1=10;
wmin1=[65E-9 70E-9 70E-9 140E-9 140E-9 140E-9 400E-9 400E-9 800E-9 800E-9 0
0 0 0];  % Minimum width from interconnect of 45 nm.

% -------------------    22 nm technology node    ---------------------%
% Contain 9 metal layers
Hcontact2=76E-9;% Thickness of the contact between transistors and metal 1
L_int2 = [76E-9 68E-9 68E-9 110E-9 160E-9 240E-9 310E-9 468E-9 6000E-9 0 0 0
0 0];  % Thickness of the interconnects
L_via2 = [76E-9 68E-9 68E-9 110E-9 160E-9 240E-9 310E-9 468E-9 0 0 0 0 0 0];
% Thickness of the vias
L_total2 = sum(L_via2) + sum(L_int2); % Thickness of interconnects and vias
%n2=size(L_int2,2); % Dimension of the interconnect vector
n2=9;
wmin2=[45E-9 40E-9 40E-9 55E-9 80E-9 120E-9 163E-9 180E-9 4615E-9 0 0 0 0 0];
% Minimum width from interconnect of 22 nm.

% -------------------    14 nm technology node    ---------------------%
% Contain 14 metal layers
Hcontact3=56E-9;% Thickness of the contact between transistors and metal 1
L_int3 = [40E-9 42E-9 40E-9 37E-9 75E-9 110E-9 180E-9 200E-9 200E-9 260E-9
375E-9 1080E-9 6000E-9 0]; % Thickness of the interconnects
L_via3 = [30E-9 39E-9 33E-9 39E-9 70E-9 100E-9 130E-9 180E-9 200E-9 280E-9
300E-9 690E-9 0]; % Thickness of the vias
L_total3 = sum(L_via3) + sum(L_int3); % Thickness of interconnects and vias
%n3=size(L_int3,2); % Dimension of the interconnect vector
n3=14;
wmin3=[28E-9 35E-9 26E-9 28E-9 39E-9 50E-9 78E-9 80E-9 80E-9 123E-9 125E-9
540E-9 4600E-9 0]; % Minimum width from interconnect of 14 nm.

% -------------------    10 nm technology node    ---------------------%
% Contain 13 metal layers
Hcontact4=40E-9;% Thickness of the contact between transistors and metal 1
L_int4 = [33E-9 30E-9 37E-9 37E-9 37E-9 43E-9 70E-9 93E-9 93E-9 133E-9 133E-9
900E-9 9167E-9 0]; % Thickness of the interconnects
```

```
L_via4 = [33E-9 30E-9 37E-9 37E-9 37E-9 43E-9 70E-9 93E-9 93E-9 133E-9 133E-9
900E-9 0 0]; % Thickness of the vias
L_total4 = sum(L_via4) + sum(L_int4); % Thickness of interconnects and vias
%n4=size(L_int4,2); % Dimension of the interconnect vector
n4=13;
wmin4=[60E-9 100E-9 140E-9 180E-9 220E-9 260E-9 300E-9 400E-9 500E-9 600E-9
700E-9 800E-9 900E-9 1000E-9]; % Minimum width from interconnect of 45 nm.

% ---------------------  Extracted from the layout  ---------------------%
% Inserir aqui valores obtidos pela ferramenta EDA. ( No caso seria:
%%
% <http://www.mathworks.com MathWorks> load('vdd.mat');
%load('all_lines.mat');

jmax = 2000; % A/m Maxima densidade de corrente
j1 = vdd.j*jmax;    % A/m - Densidade de corrente
w1 = vdd.w*1E-6;    % m - Largura
ll1 = vdd.l*1E-6;   % m - Comprimento dos paths
ll2 = vdd.eml*1E-6; % m - COmprimento maior caminho com um path
layer = vdd.layer;  % Camadas
net1 = vdd.net;     % Nome das interconexões
i1=j1.*w1;          % Corrente das linhas
% -----------------  Choose the technology evaluated  -------------------%
% prompt = 'Choose the technology [1]45nm[2]22nm[3]14nm[4]10nm ->  ';
% tec = input(prompt);
tec=0;
if tec==0
wmin=wmin0;
L_int=L_int0;
L_via=L_via0;
L_total=L_total0;
n=n1;
end
if tec==1
wmin=wmin1;
L_int=L_int1;
L_via=L_via1;
L_total=L_total1;
```

```
n=n1;
end
if tec==2
wmin=wmin2;
L_int=L_int2;
L_via=L_via2;
L_total=L_total2;
n=n2;
end
if tec==3
wmin=wmin3;
L_int=L_int3;
L_via=L_via3;
L_total=L_total3;
n=n3;
end
if tec==4
wmin=wmin4;
L_int=L_int4;
L_via=L_via4;
L_total=L_total4;
n=n4;
end

for(cont2=1:1:length(layer))
if layer(cont2)==1
t(cont2)=L_int(1);
end

if layer(cont2)==2
t(cont2)=L_int(2);
end
if layer(cont2)==3
t(cont2)=L_int(3);
end
if layer(cont2)==4
t(cont2)=L_int(4);
end
```

```
if layer(cont2)==5
t(cont2)=L_int(5);
end
if layer(cont2)==6
t(cont2)=L_int(6);
end
if layer(cont2)==7
t(cont2)=L_int(7);
end
if layer(cont2)==8
t(cont2)=L_int(8);
end
if layer(cont2)==9
t(cont2)=L_int(9);
end
if layer(cont2)==10
t(cont2)=L_int(10);
end
if layer(cont2)==11
t(cont2)=L_int(11);
end
if layer(cont2)==12
t(cont2)=L_int(12);
end
if layer(cont2)==13
t(cont2)=L_int(13);
end
if layer(cont2)==14
t(cont2)=L_int(14);
end
end
% ==============  Cálculo tradicional da densidade de corrente ===========%

j11=i1./(w1.*t'); % Representação típica da densidade de corrente
% Falta inserir o arquivo com os dados  do leiaute

% --------------------  Extracted from the layout  --------------------%
% Data to calculate the temperature change in the interconnects
```

```
km = 401;    % Thermal conductivity from metal - Wm/K
ki = 1.4;    % Thermal conductivity from insulator - Wm/K
Vint=[0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3 0.3];
% Interconnect fraction volume (Pode ser calculado)
Vvia=[0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04 0.04];
% Via fraction volume (Pode ser calculado)
PT=230;      % Power dissipated by the transistors

% =======================  Cálculo do aspect ratio =======================%

Nl1=0; Nl2=0; Nl3=0; Nl4=0; Nl5=0; Nl6=0; Nl7=0; Nl8=0; Nl9=0; Nl10=0; Nl11=0;
Nl12=0; Nl13=0; Nl14=0; % Número de interconexões para cad metal
l1=0; l2=0; l3=0; l4=0; l5=0; l6=0; l7=0; l8=0; l9=0; l10=0; l11=0; l12=0;
l13=0; l14=0;
for cont3=1:1:length(ll2)
if layer(cont3)==1
l1=l1+ll2(cont3); % Length of Metal 1 lines
Nl1=Nl1+1; % Number of Metal 1 lines
end

if layer(cont3)==2
l2=l2+ll2(cont3);  % Length of Metal 2 lines
Nl2=Nl2+1; % Number of Metal 2 lines
end

if layer(cont3)==3
l3=l3+ll2(cont3);  % Length of Metal 3 lines
Nl3=Nl3+1; % Number of Metal 3 lines
end

if layer(cont3)==4
l4=l4+ll2(cont3);  % Length of Metal 4 lines
Nl4=Nl4+1; % Number of Metal 4 lines
end

if layer(cont3)==5
l5=l5+ll2(cont3);  % Length of Metal 5 lines
```

```
Nl5=Nl5+1; % Number of Metal 5 lines
end

if layer(cont3)==6
l6=l6+ll2(cont3);  % Length of Metal 6 lines
Nl6=Nl6+1; % Number of Metal 6 lines
end

if layer(cont3)==7
l7=l7+ll2(cont3);  % Length of Metal 7 lines
Nl7=Nl7+1; % Number of Metal 7 lines
end

if layer(cont3)==8
l8=l8+ll2(cont3);  % Length of Metal 8 lines
Nl8=Nl8+1; % Number of Metal 8 lines
end

if layer(cont3)==9
l9=l9+ll2(cont3);  % Length of Metal 9 lines
Nl9=Nl9+1; % Number of Metal 9 lines
end

if layer(cont3)==10
l10=l10+ll2(cont3);  % Length of Metal 10 lines
Nl10=Nl10+1; % Number of Metal 10 lines
end

if layer(cont3)==11
l11=l11+ll2(cont3);  % Length of Metal 11 lines
Nl11=Nl11+1; % Number of Metal 11 lines
end

if layer(cont3)==12
l12=l12+ll2(cont3);  % Length of Metal 12 lines
Nl12=Nl12+1; % Number of Metal 12 lines
end
```

```
if layer(cont3)==13
l13=l13+l12(cont3);  % Length of Metal 13 lines
Nl13=Nl13+1; % Number of Metal 13 lines
end

if layer(cont3)==14
l14=l14+l12(cont3);  % Length of Metal 14 lines
Nl14=Nl14+1; % Number of Metal 14 lines
end

end

% Average length of the interconnect lines

ar_1=(l1/Nl1)/L_int(1); %ar -> % Metal 1 average length.
ar_2=(l2/Nl2)/L_int(2); %ar -> % Metal 2 average length.
ar_3=(l3/Nl3)/L_int(3); %ar -> % Metal 3 average length.
ar_4=(l4/Nl4)/L_int(4); %ar -> % Metal 1 average length.
ar_5=(l5/Nl5)/L_int(5); %ar -> % Metal 1 average length.
ar_6=(l6/Nl6)/L_int(6); %ar -> % Metal 1 average length.
ar_7=(l7/Nl7)/L_int(7); %ar -> % Metal 1 average length.
ar_8=(l8/Nl8)/L_int(8); %ar -> % Metal 1 average length.
ar_9=(l9/Nl9)/L_int(9); %ar -> % Metal 1 average length.
ar_10=(l10/Nl10)/L_int(10); %ar -> % Metal 1 average length.
ar_11=(l11/Nl11)/L_int(11); %ar -> % Metal 1 average length.
ar_12=(l12/Nl12)/L_int(12); %ar -> % Metal 1 average length.
ar_13=(l13/Nl13)/L_int(13); %ar -> % Metal 1 average length.
ar_14=(l14/Nl14)/L_int(14); %ar -> % Metal 1 average length.

ar=[ar_1 ar_2 ar_3 ar_4 ar_5 ar_6 ar_7 ar_8 ar_9 ar_10 ar_11 ar_12 ar_13 ar_14];
% Aspect ratio from all the interconnects

% ======================  Temperature calculation  =======================%

% ----------------------Fixed for the technonologies----------------------%
for cont4 = 1:1:n
L11(cont4)=(ar(cont4))^2/(2*(ar(cont4)^2-1))-(ar(cont4))/
(2*(ar(cont4)^2-1)^1.5)*acosh(ar(cont4)); %  L11 of the layers
```

```
Bxy(cont4)=(km-ki)/(ki+L11(cont4)*(km-ki)); %  Bxy of the layers
alfa(cont4)=Bxy(cont4)*(1-L11(cont4)); % Alpha of the layers
beta(cont4)=Bxy(cont4)*L11(cont4); % Beta of the layers
keffInt(cont4)=beta(cont4)*ki*((1+alfa(cont4)*Vint(cont4))/(1-Vint(cont4)));
%keffInt of the layers
keffVia(cont4)=km*Vvia(cont4)+ki*(1-Vvia(cont4)); %  keffVia of the layers
a(cont4)=L_int(cont4)/keffInt(cont4); % a is the first term of the Keff_BEOL
b(cont4)=L_via(cont4)/keffVia(cont4); % b is the second term of the Keff_BEOL
end
L_total=750E-9;
Keff_BEOL=((sum(a,'omitnan')+sum(b,'omitnan'))^-1)*L_total;

%-------------------------------------------------------------------------%

% -------------------  Metal position calculation  ----------------------%
% Cálculo da altura em cada camada metálica
hmetal1=[Hcontact1;Hcontact2;Hcontact3;Hcontact4]; % Thickness of the contact
%L_total=[L_total1 L_total2 L_total3 L_total4];

% ---------------------  Temperatura em cada camada  --------------------%
zo=0;
for camada=1:1:n

zo=zo+L_int(camada);
Delta_T(camada)=-(PT/(2*pi*Keff_BEOL))*log(zo/(2*L_total-zo))

end

%Initial temperature in K;
T_metal=300 +(Delta_T) %Temperature in the interconnect lines

% ----------------  Resistance change of the lines ------------------%
% --------  Parameters to obtain thre resistance change  ---------%

w_b=3E-9; % Barrier width
t_b=3E-9;
T = T_metal; % Temperature changed with power dissipated
A=w1.*t'; % m² - metal area
```

```
A_b=2*w_b*t'+t_b*w1+2*w_b*t_b; % Barrier area
rho_b=60E-8; % Metal resistivity
Do=3.1E-5; % Cu diffusivity
k=8.61733E-5; % Boltzman constant
Ea=1.0; % Activation energy
e=1.6E-19; % electron charge
Z=1; % Number of valence
ZB=1.38E-23; % Boltzman constant
dia=24*60*60; % days
ano = 365*dia; % years

% =============  Diffusivity and Temperature by layer ==============%

for count =1:1:length(layer)
if  layer(count)==1
T(count)=T_metal(1);
D(count)=Do*(exp(-Ea/(k*T_metal(1)))); % Diffusivity
end
if  layer(count)==2
T(count)=T_metal(2);
D(count)=Do*(exp(-Ea/(k*T_metal(2)))); % Diffusivity
end
if  layer(count)==3
T(count)=T_metal(3);
D(count)=Do*(exp(-Ea/(k*T_metal(3)))); % Diffusivity
end
if  layer(count)==4
T(count)=T_metal(4);
D(count)=Do*(exp(-Ea/(k*T_metal(4)))); % Diffusivity
end
if  layer(count)==5
T(count)=T_metal(5);
D(count)=Do*(exp(-Ea/(k*T_metal(5)))); % Diffusivity
end
if  layer(count)==6
T(count)=T_metal(6);
D(count)=Do*(exp(-Ea/(k*T_metal(6)))); % Diffusivity
end
```

```
if  layer(count)==7
T(count)=T_metal(7);
D(count)=Do*(exp(-Ea/(k*T_metal(7)))); % Diffusivity
end
if  layer(count)==8
T(count)=T_metal(8);
D(count)=Do*(exp(-Ea/(k*T_metal(8)))); % Diffusivity
end
if  layer(count)==9
T(count)=T_metal(9);
D(count)=Do*(exp(-Ea/(k*T_metal(9)))); % Diffusivity
end
if  layer(count)==10
T(count)=T_metal(10);
D(count)=Do*(exp(-Ea/(k*T_metal(10)))); % Diffusivity
end
if  layer(count)==11
T(count)=T_metal(11);
D=Do*(exp(-Ea/(k*T_metal(11)))); % Diffusivity
end
if  layer(count)==12
T(count)=T_metal(12);
D(count)=Do*(exp(-Ea/(k*T_metal(12)))); % Diffusivity
end
if  layer(count)==13
T(count)=T_metal(13);
D=Do*(exp(-Ea/(k*T_metal(13)))); % Diffusivity
end
if  layer(count)==14
T(count)=T_metal(14);
D(count)=Do*(exp(-Ea/(k*T_metal(14)))); % Diffusivity
end
% Resistance change calculation
deltaR_Ro(count)=((A(count).*j11(count)*rho_b*D(count)*e*Z*1*ano)./
(A_b(count).*l12(count)*ZB*T(count)));
% Percentual Resistance change calculation
deltaR_Ro_porcentagem(count)=100*((A(count).*j11(count)*rho_b*D(count)
*e*Z*2*ano)./(A_b(count).*l12(count)*ZB*T(count)));
```

```
end

deltaR_Ro= deltaR_Ro'; % Matriz transposed
deltaR_Ro_porcentagem=deltaR_Ro_porcentagem'; % Matriz transposed

max(100*deltaR_Ro); % Maximum resistance change
min(100*deltaR_Ro); % Minimum resistance change

%%%%%%%%%%%%%% Evaluation of the interconnect %%%%%%%%%%%%%%%%

%Table with the interconnect data
dados3b = table(net1,layer,ll1,w1,i1,j1,deltaR_Ro,deltaR_Ro_porcentagem) %

% --------------    Evaluation of the critical lines    ---------------%
% ----------- CRITERION 1: Comparation with the Jmax ------------------%

nj = 0; % Number of critical interconnects due to current density criterion
%jmax=2E10;
jmax=2E3 % Ampere por metro;
for c=1:1:length(layer)
if (j1(c)>(1*jmax))
condicao_j(c) = 1;
nj = nj + 1;
else
condicao_j(c) = 0;
end
end

% ----------- CRITERION 2: Comparation with the Blech Product-----------%

nb = 0;
%JLmax=1E5; % Ampere per meter - Aluminum
JLmax=3.7E5; % Ampere per meter - Cooper

for d=1:1:length(layer)
if (j11(d)*ll2(d)>(JLmax))
condicao_b(d) = 1;
nb = nb + 1;
```

```
else
condicao_b(d) = 0;
end
end

% -------------------        Two criteria above      --------------------%
njb0 =0;
margem=1.0;
for cf=1:1:length(layer)
if ((j1(cf)>(margem*jmax))||(j11(cf)*l12(cf)>margem*(JLmax)))
condicao_jb0(cf) = 1;
njb0 = njb0 + 1;
else
condicao_jb0(cf) = 0;
end
end

g=0;

% -----------------        Lines Prone to Failure      -----------------%
njb =0;
margem=1.0;
for cf=1:1:length(layer)
if ((j1(cf)>(margem*jmax))||(j11(cf)*l12(cf)>margem*(JLmax)))
condicao_jb(cf) = 1;
njb = njb + 1;
else
condicao_jb(cf) = 0;
end
end

% ---------- CRITERION 3: Comparation with the delta_R_critico---------%

nr = 0;
delta_R_critical=0.1;

for c=1:1:length(layer)
if (deltaR_Ro(c)>delta_R_critical)
```

```
condicao_r(c) = 1;
nr = nr + 1;
else
condicao_r(c) = 0;
end
end

% -------------------- Critical based on the 3 criteria----------------%
for g=1:1:length(layer)

% Critical for the 3 criteria
A1(g)= condicao_j(g)*condicao_b(g)*condicao_r(g);

% Critical for the jmax and resistance change criteria
B1(g)= condicao_j(g)*condicao_r(g)-A1(g);

% Critical for the resistance change and Blech criteria
C1(g)= condicao_b(g)*condicao_r(g)-A1(g);

% Critical for the jmax and Blech criteria
D1(g)= condicao_b(g)*condicao_j(g)-A1(g);

end

% Number of critical lines for each criterion

A1=sum(A1); B1=sum(B1); C1=sum(C1); D1=sum(D1);
E1 = nr - A1 - B1 - C1;
F1 = nj - A1 - B1 - D1;
G1 = nb - A1 - C1 - D1;

% --------------------          REPORT          ----------------------%
report1=table(net1,condicao_j',condicao_r', condicao_b');

% -----------  Width of the lines based on the EM criteria  -----------%

a=1;
aa=1;
```

```
njbr=0;
tempo=2*ano;
for ddd=1:1:length(layer)

% Width based on the Jmax (nm)
w_j(ddd)=i1(ddd)/jmax;

% Width based on the Blech (nm)
w_bl(ddd)=((i1(ddd)*ll2(ddd))/t(ddd))/JLmax;

% Width based on the resistance change (nm)
alfa(ddd)=((Z*e*rho_b*D(ddd)*i1(ddd)*tempo)/(T(ddd)*ll2(ddd)*ZB*t_b))
*delta_R_critical;
beta(ddd)=-2*w_b*(1+t(ddd)/t_b)
w_r(ddd)=alfa(ddd)-beta(ddd);

% Width based on the jmax and Blech (nm)
w_m1(ddd)=max(w_j(a),w_bl(a))

% Width based on the jmax, Blech and resistance change (nm)
w_m(ddd)=max(w_m1(a),w_r(a))

% Width recommended based EM criteria (nm)
if ((condicao_j(ddd)||condicao_r(ddd))||condicao_b(ddd) )
situacao(ddd)=1;
net_critica(a)=net1(ddd);
w_rec1(a)=max(w_j(ddd),w_bl(ddd))
w_rec(a)=1E9*max(w_rec1(a),w_r(ddd))
njbr=njbr+1;
else
situacao(ddd)=0;
end
if (condicao_j(ddd)||condicao_b(ddd) )
aa=aa+1;
end
a=a+1;
end
```

```
% ------------    Report of the interconnect dimensions    -------------%

report2=table( net1, w_j'*1E9, w_bl'*1E9, w_r'*1E9,w_m'*1E9);
report2.Properties.VariableNames = {'Critical_net' 'w_j_nm' 'w_bl_nm'
'w_r_nm' 'recommended_w_nm'}

% -------     Design to mantain the expected circuit lifetime     --------%
% ---------------     DeltaR/Ro = delta_R_critical     ------------------%

h=L_int(1);
for ddd=1:1:length(layer)

% -------     Design to mantain the expected circuit lifetime     --------%
% -------     1 year     --------%
tempo=1*ano;
alfa(ddd)=((Z*e*rho_b*D(ddd)*i1(ddd)*tempo)/(T(ddd)*ll2(ddd)*ZB*t_b))
*delta_R_critical;
beta(ddd)=-2*w_b*(1+t(ddd)/t_b)
w_em_1(ddd)=1E9*(alfa(ddd)-beta(ddd));  % Largura em nano
if w_em_1(ddd)<60
w_em_1(ddd)=60;
end
% -------     2 years     --------%
tempo=2*ano;
alfa(ddd)=((Z*e*rho_b*D(ddd)*i1(ddd)*tempo)/(T(ddd)*ll2(ddd)*ZB*t_b))
*delta_R_critical;
beta(ddd)=-2*w_b*(1+t(ddd)/t_b)
w_em_2(ddd)=1E9*(alfa(ddd)-beta(ddd)); % Largura em nano
if w_em_2(ddd)<60
w_em_2(ddd)=60;
end
% -------     5 years     --------%
tempo=5*ano;
alfa(ddd)=((Z*e*rho_b*D(ddd)*i1(ddd)*tempo)/(T(ddd)*ll2(ddd)*ZB*t_b))
*delta_R_critical;
beta(ddd)=-2*w_b*(1+t(ddd)/t_b)
w_em_5(ddd)=1E9*(alfa(ddd)-beta(ddd)); % Largura em nano
```

```
if w_em_5(ddd)<60
w_em_5(ddd)=60;
end
end
report3=table( net1, w_em_1', w_em_2', w_em_5');
report3.Properties.VariableNames = {'Critical_net' 'one_year'
'two_years' 'five_years'}

% ========  Evaluate if the line is oversized or undersized  ========%
% -----    Compare the width as the designed with the suggested     ----%

h=L_int(1);
cont_under=0;
cont_over=0;
cont_normal=0;
for ddd=1:1:length(layer)

if (w_m(ddd)> w1(ddd))
undersized(ddd) = 1;
normal(ddd)=0;
cont_under=cont_under+1;
end

if (w_m(ddd)< w1(ddd))
undersized(ddd) = 0;
oversized(ddd) = 1;
cont_over=cont_over+1;
normal(ddd)=0;
end

if(w_m(ddd)== w1(ddd))
undersized(ddd) = 0;
oversized(ddd) = 0;
normal(ddd)=1;
cont_normal=cont_normal+1;
end
end
```

```
% ------------------       Width suggested      --------------------%
margem=1.0;
line_over=0;
line_under=0;
for cf=1:1:length(layer)
if condicao_jb(cf)*condicao_r(cf) == 1
w_recom2(cf)=max(w_j(cf), w_bl(cf));
w_recom1(cf)=max(w_recom2(cf), w_r(cf));
w_recom(cf)=max(w_recom1(cf), wmin(1));
line_over=1+line_over;
elseif condicao_jb(cf)*condicao_r(cf) == 0
w_recom1(cf)=max(w_j(cf), w_bl(cf));
w_recom(cf)=max(w_recom1(cf), wmin(1));
line_under=line_under+1;
end
end

% ----------------- Report with the widths ----------------------%
dados_resultados.Properties.VariableNames =
{'net' 'l_um' 'w_um' 'i_uA' 'Jmax' 'R_R0' 'Bl' 'Crit' 'w1_um' 'w2_um'
'w5_um' 'under'}
createfigure2
net_critica'
"number of critical interconnects = "
cut=[1 0];
figure(1);
% Número de linhas críticas devido ao critério da densidade de corrente
%labels={'Non-critical', 'Critical'};
ax1=subplot(2,3,1);
X1 = [length(layer)-nj nj];
pie(ax1,X1,cut);

% Create textbox
%annotation('textbox', [0.2 0.47 0.06 0.26],'String', {'J_m_a_x criterion'},
'LineStyle','none');

% Número de linhas críticas devido a um dos critérios
%labels={'Non-critical', 'Critical'};
```

```
ax2=subplot(2,3,2);
X2 = [length(layer)-nb nb];
pie(ax2,X2,cut);

% Número de linhas críticas devido ao critério do produto de Blech
%labels={'Non-critical', 'Critical'};
ax3=subplot(2,3,3);
X3 = [length(layer)-njb0 njb0];
pie(ax3,X3,cut);

% Número de linhas críticas devido ao critério da resistência crítica
%labels={'Non-critical', 'Critical'};
ax4=subplot(2,3,4);
X4 = [length(layer)-njb njb];
pie(ax4,X4,cut);

% Número de linhas oversized
%labels={'Non-critical', 'Critical'};

ax5=subplot(2,3,5);
X5 = [length(layer)-nr nr];
pie(ax5,X5,cut);

% Número de linhas críticas devido a densidade de corrente
%labels={'Non-critical', 'Critical'};
ax6=subplot(2,3,6);
X6 = [length(layer)-njbr njbr];
pie(ax6,X6,cut);

"number of undersized interconnects = "
cont_under
figure(2);
venn([4,4,4], [1 1 1 1])
lgd = legend({'J_m_a_x','Blech product','\DeltaR/R_0'},'FontSize',24,
'TextColor','black')
axis off

% Plotar o número de criticas devido a resistência
```

```
text(0.65,1.7,num2str(E1),'Color',[1 1 1],'FontSize',40)

% Plotar o número de criticas devido a jmax
text(-0.4,-0.5,num2str(F1),'Color',[1 1 1],'FontSize',40)

% Plotar o número dr criticas devido ao produto de Blech
text(1.7,-0.5,num2str(G1),'Color',[1 1 1],'FontSize',40)

% Interseção de dois pontos_blech_jmax
text(0.6,-0.2,num2str(D1),'Color',[1 1 1],'FontSize',40)

% Interseção de dois pontos_deltaR_jmax
text(0.0,0.7,num2str(B1),'Color',[1 1 1],'FontSize',40)

% Interseção de dois pontos_deltaR_blech
text(1.1,0.7,num2str(C1),'Color',[1 1 1],'FontSize',40)

% Interseção de três pontos
text(0.6,0.4,num2str(A1),'Color',[1 1 1],'FontSize',40)

% Plotar o número total de linhas
text(-2,2.0,'N = ','Color',[0 0 0],'FontSize',32)
text(-1.7,2.0,num2str(length(layer)),'Color',[0 0 0],'FontSize',32)

% Plotar o número total de linhas criticas devido aos três critérios
text(-2,1.6,'Nc = ','Color',[0 0 0],'FontSize',32)
text(-1.6,1.6,num2str(length(layer)-sum(situacao)),'Color',[0 0 0],
'FontSize',32)

under_1b=0;
for count=1:1:length(layer)
if w1(count)<0.95*w_m(count)
under_1b=under_1b+1;
v_a(count)=2;

elseif w1(count)>1.05*w_m(count)
over_1b=under_1b+1;
v_a(count)=1;
```

```
else
v_a(count)=0;
end
end
```

APPENDIX E – Dual-Damascene Fabrication Process

The copper interconnects introduced by IBM with the assistance from Motorola in 1997 required the introduction of barrier metal layers to isolate the silicon from the copper atoms, since diffusion of copper into silicon forms deep-level traps.

In a damascene process the dielectric is first deposited onto the substrate, which is then patterned and filled by metal deposition. The dual-damascene process is characterized by patterning the vias and trenches, in such a way that the metal deposition fills both at the same time [4,6]. Figure E.1 depicts the process steps for fabricating a typical copper dual-damascene interconnect.

A new technique named Dual damascene was created to reproduce interconnect structures based on conductive copper metal lines inlaid into an oxide or low dielectric constant nonconductive layer. In this process, the underlying insulating layer is patterned with open trenches, as illustrated in Figure E.1(a). This is followed by the deposition of a diffusion barrier which is typically a Ta-based layer, Figure E.1(b). After the deposition of the diffusion barrier, a thin Cu seed is deposited by physical vapor deposition (PVD) followed by the electroplating of Cu, which fills the via and trench. The excess Cu is removed by a chemical mechanical polishing process (CMP) and an etch stop layer (also called capping layer), typically SiN based, is deposited. In this way, the complete interconnect structure can be produced by repeating these process steps for each level of metallization. With successive layers of insulator and copper, a multilayer interconnect structure is created.

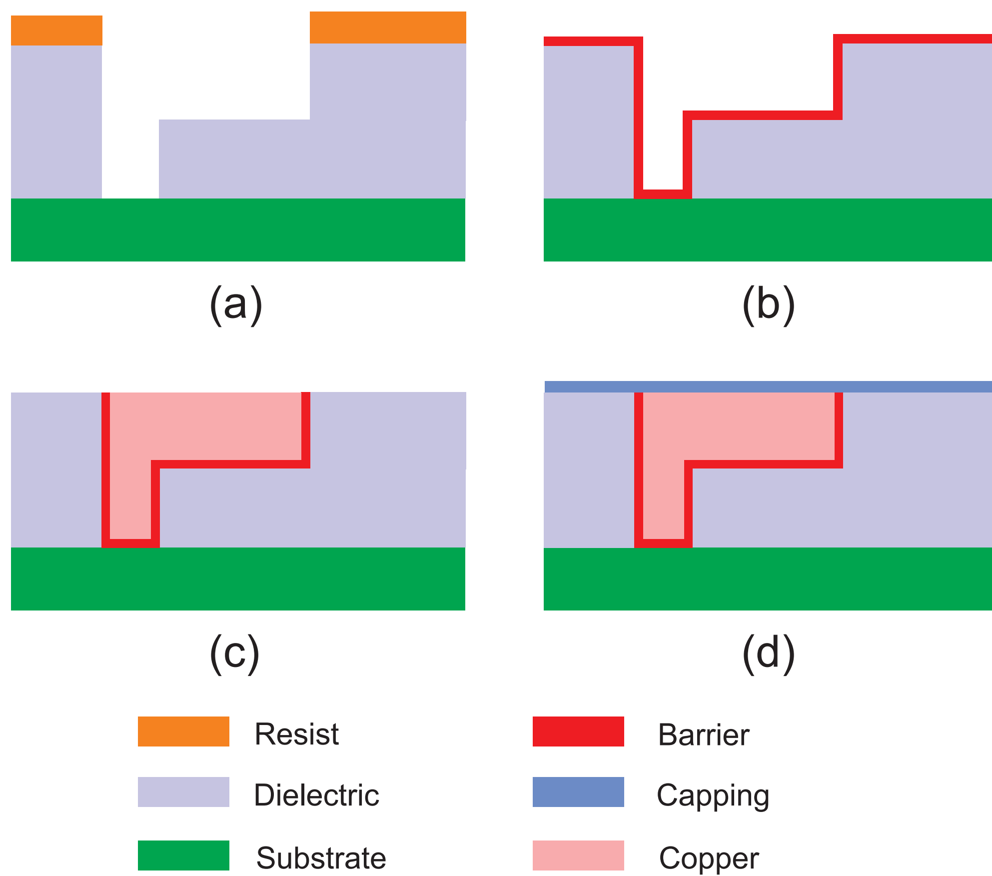

Figure E.1 – Cooper dual-damascene process: nucleation in (a) via and trench patterning, (b) barrier layer deposition, (c) Cu electroplating and excess removal by CMP, and (d) capping layer deposition.

APPENDIX F – η and β for ΔT_{PT}

The transistors' self-heating in the FEOL results in a non-uniform temperature distribution in the metallic layers of the BEOL. The temperature change in each metallic layer is given by [133]

$$\Delta T_{PT} = \frac{P_T}{2\pi k_{eff}^{beol}} ln\left(\frac{z}{2h_0 - z}\right), \quad \text{(F.1)}$$

where P_T is the power dissipated by transistors, z is the distance from heat source, h_0 is the BEOL thickness, and k_{eff}^{beol} is the effective thermal conductivity of the BEOL given by [133]

$$k_{eff}^{beol} = \left[\sum_{n=1}^{m}\left(\frac{L_n^{via}}{k_{eff_n}^{via}} + \frac{L_n^{int}}{k_{eff_n}^{int}}\right)\right]^{-1} \cdot h_0, \quad \text{(F.2)}$$

where m is the total number of interconnect layers, L_n^{via} and L_n^{int} are the height of the vias and interconnects for a particular layer, k_{eff}^{via} and k_{eff}^{int} are the thermal conductivities of the via and the metallic layers, respectively.

Eq. F.1 represents a one-dimensional (1D) model which considers the heat flow through the various parts of a chip, including the silicon substrate, the FEOL, and the BEOL. The model was validated by three-dimensional (3D) finite element simulations and also through comparison with experimental data [133]. The results show a reasonable agreement of the temperature in the metallic layers for regions which are not very close to the heat sources. Eq. F.1 has a lower accuracy in regions close to the heat sources [133], where the 3D nature of the heat flow problem becomes more evident. Here, 3D models are more accurate, but they are too time-consuming and cannot be easily integrated in the design flow, mainly for IC technologies below 45 nm with structures that involves more than 10 layers.

It should be pointed out that, although F.1 is essentially an 1D model, as previously mentioned, the effect of the substrate, the FEOL, and the BEOL have been considered. The heat flows mainly through the substrate, while a fraction considerably smaller flow through the BEOL [131, 241].

The thermal conductivities of the via and the interconnects layers depend on the fraction volume of vias (V_{via}) and lines (V_{int}), respectively, relative to the complete volume of the specific layer. The k_{eff}^{via}, given by F.3, varies with the thermal conductivity

of the metal (k_m) and insulating (k_i) materials as [242]

$$k_{eff}^{via} = k_m V_{via} + k_i(1 - V_{via}). \tag{F.3}$$

The thermal conductivity of the interconnects is given by

$$k_{eff}^{int} = \beta k_i \frac{1 + \eta V_{int}}{1 - V_{int}}, \tag{F.4}$$

where β and η are related to the thermal conductivities of the materials through [133]

$$\beta = \frac{L_{11}(k_m - k_i)}{k_i + L_{11}(k_m - k_i)}, \tag{F.5}$$

$$\eta = \beta \left(\frac{1}{L_{11}} - 1 \right), \tag{F.6}$$

with

$$L_{11} = \frac{{a_r}^2}{2({a_r}^2 - 1)} - \frac{a_r}{2({a_r}^2 - 1)^{3/2}} \cosh^{-1} a_r, \tag{F.7}$$

which depends on the average aspect ratio a_r of the wire, i.e. the ratio between the length and the height of the wire [133, 243].

Fig. F.1 shows η and β as a function of the a_r. Considering the Metal 1 layer from a 45 nm technology, a line with a height of 130 nm and a length of 10 μm has an a_r equal to 76.9. This value gives an η and β of 0.99. Short lines, with length smaller than 2.5 μm, exhibit a_r inferior to 20. Below this value, the η and β curves show a significant difference. In this work the dimensionless parameters η and β are approximated to 1 for interconnect lines with dimensions above 10 μm [133].

Fig. F.2 shows the effective thermal conductivity of the Metal 1 layer as a function of a_r with the metal volume fraction (V_{int}) as a parameter. As expected from the previous curves, the k_{eff}^{int} is constant for a_r values superior to 20. The thermal conductivity of the Metal 1 layer increases as the fraction volume of the lines change from 20% to 40%. With a V_{int} of 20% and a_r of 20, the k_{eff}^{int} is 2.08. The k_{eff}^{int} increases to 3.24, for a V_{int} of 40%, a variation of 55.7%. This demonstrates that the V_{int} has a more significant influence on the thermal conductivity than the a_r parameter.

Fig. F.3 shows the effective thermal conductivity of the BEOL (k_{eff}^{beol}) as a function of a_r and V_{int}. A k_{eff}^{beol} of 3.29 W/K.m is obtained for a V_{int} of 20%. The conductivity increases to 3.99 for V_{int} of 30%, a change of 21.3%. As before, increasing the fraction volume of the lines results in a larger thermal conductivity for the BEOL.

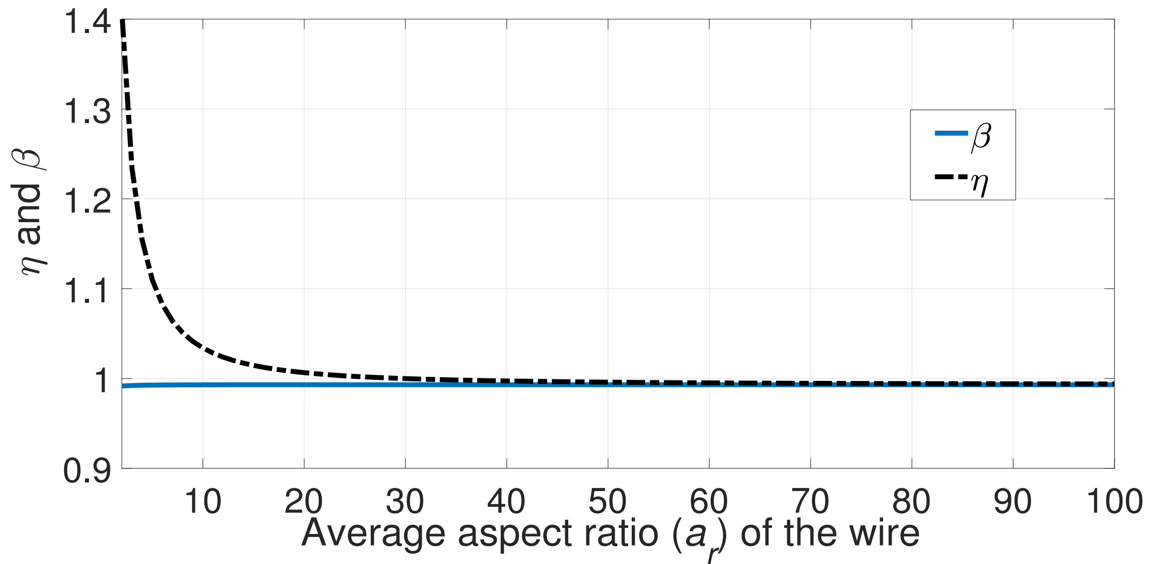

Figure F.1 – Parameters β and η as a function of the average aspect ratio a_r.

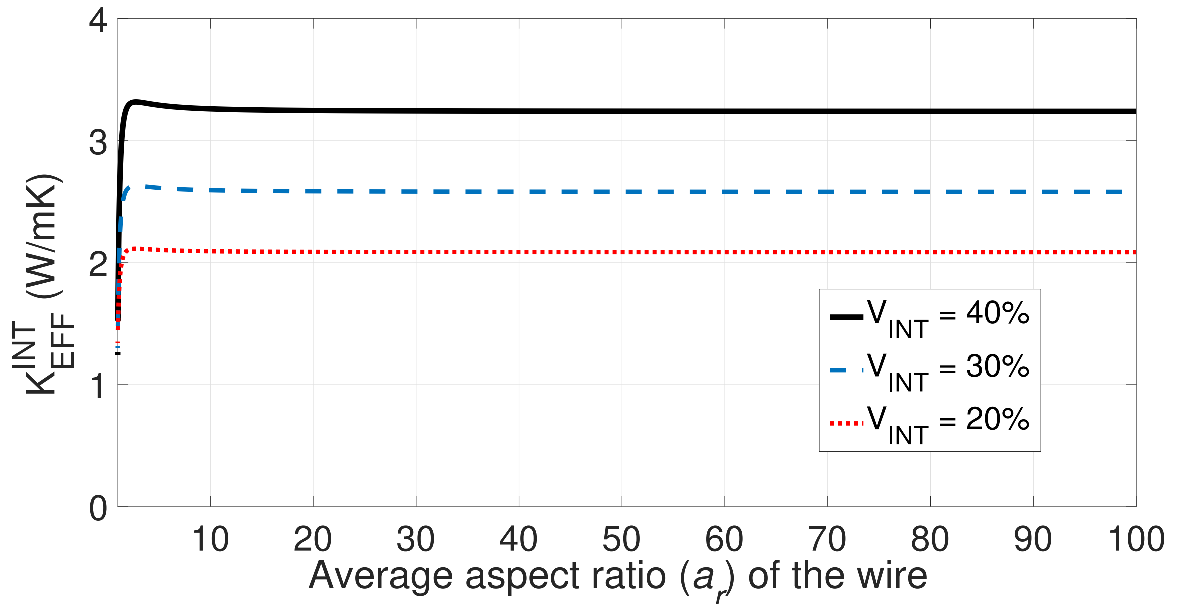

Figure F.2 – Effective thermal conductivity of the Metal 1 layer as a function of the average aspect ratio (a_r) for h_0 = 11720 nm and L_1^{int} = 130 nm.

Fig. F.4 shows the temperature variation (ΔT_{PT}) of the Metal 1, Metal 2, and Metal 3 layer as a function of k_{eff}^{int} for a power dissipation of 500 W/m. As expected, being closer to the FEOL, the power dissipations source, the Metal 1 layer exhibits the highest temperature. Observe that the k_{eff}^{int} can affect significantly the temperature of the layers. For a Metal 1 with k_{eff}^{int} of 40% its temperature is reduced by 34 K, a reduction of 33.3%. As the electromigration is more critical for lines under elevated temperatures and current densities, the lines with reduced k_{eff}^{int} and near the heat source are more susceptible to high temperatures and, thus potentially critical regarding EM failures.

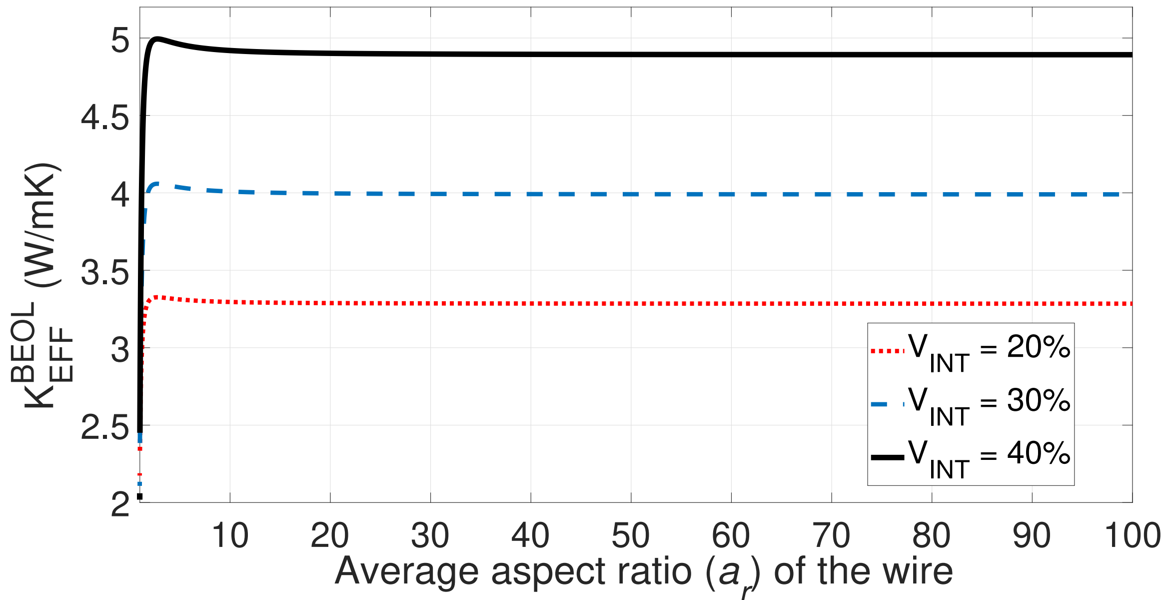

Figure F.3 – Effective thermal conductivity of the BEOL as a function of the average aspect ratio (a_r) with L_n^{int} and L_n^{via} dimensions from a 45 nm technology.

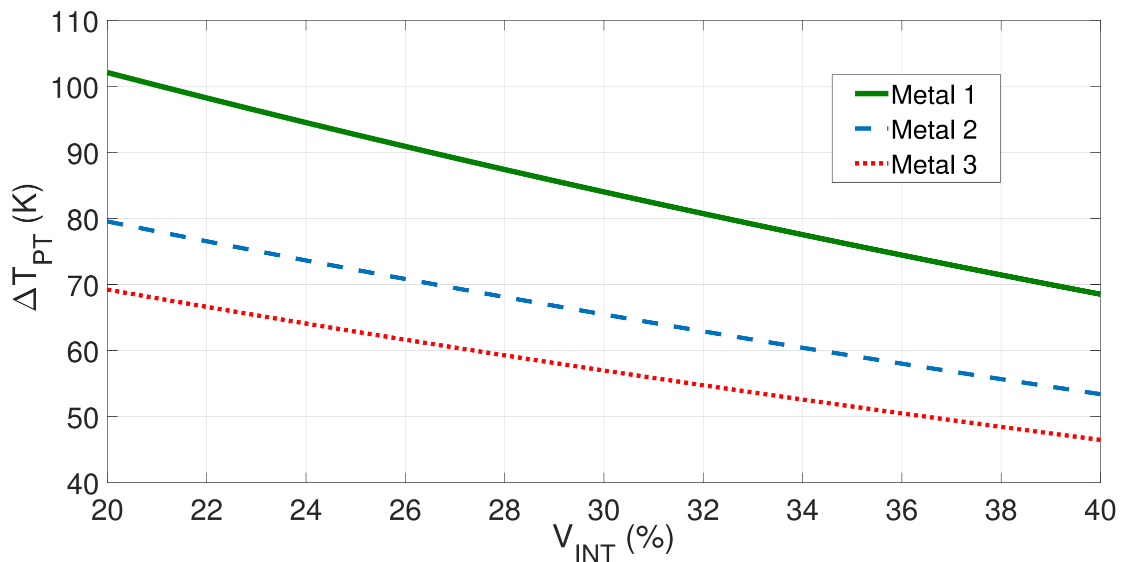

Figure F.4 – Temperature variation in the Metal1, Metal2 and Metal 3 layers, as a function of the fraction volume of lines (k_{eff}^{int}).

The importance of studying the temperature distribution on the BEOL becomes more evident for the newer technologies, for which the metallic layers have smaller thicknesses. For example, the 10 nm Intel technology has a Metal 1 layer thickness of 36 nm, 3.6 times smaller than the thickness of the Metal 1 from GPDK 45 nm. This indicates that new technologies have a reduced distance between the metal layers and the transistors. Consequently, the BEOL is more affected by temperature changes due the self-heating from the transistors.

APPENDIX G – Interconnects of the Opamp

The list of the interconnect paths for the operational amplifier of Section 5.3 is shown in Tables G.1 to G.4.

Table G.1 – EDA data of the Opamp paths.

Path	Layer	W (μm)	L (μm)	J/j_{max}	R (ohm)
'outm'	2	0.4	22.395	1.478	0.3296
'outm'	2	0.4	0.94	1.419	0.1419
'outm'	2	0.4	0.94	1.301	0.1419
'AVDD'	3	0.5	14.05	1.447	1.697
'outm'	2	0.4	0.94	1.182	0.1419
'AVDD'	2	1.7	4.825	1.232	0.3487
'AVDD'	2	1.7	4.075	1.232	0.1448
'AVDD'	2	1.7	3.988	1.12	0.135
'outm'	2	0.4	0.94	1.064	0.1419
'outm'	3	0.6	13.69	0.982	1.378
'outm'	3	0.6	14.24	0.982	1.433
'outm'	2	0.4	0.94	0.9459	0.1419
'net044'	1	0.25	7.425	0.3241	2.186
'net044'	1	0.25	9.605	0.3241	2.839
'net044'	1	0.25	4.835	0.3241	1.423
'outp'	3	0.5	14.24	1.18	1.72
'outp'	3	0.5	13.68	1.18	1.671
'AVSS'	2	1.6	0.9365	1.098	0.1084
'AVSS'	2	1.6	12.848	1.098	0.4849
'AVSS'	2	1.6	1.74	1.052	0.06568
'AVDD'	2	0.69	19.115	1.046	0.1668
'net044'	2	0.25	6.77	0.2971	1.634
'net044'	2	0.25	5.175	0.2971	1.249
'net044'	2	0.25	5.175	0.2971	1.314
'outm'	2	0.4	0.94	0.8277	0.1419
'AVSS'	2	1.6	1.74	0.9615	0.06568
'AVDD'	2	0.69	0.94	0.978	0.08228
'outp'	2	0.4	2.575	0.9771	0.3816
'outm'	2	0.4	2.585	0.9771	0.3829
'AVSS'	2	1.6	1.74	0.8706	0.06568
'AVDD'	2	0.69	0.94	0.9098	0.08228
'AVDD'	2	1.7	2.515	0.6965	0.08936
'AVDD'	1	0.18	0.8455	0.926	0.3218

Table G.2 – EDA data of the Opamp paths.

Path	Layer	W (μm)	L (μm)	J/j$_{max}$	R (ohm)
'AVDD'	1	0.18	6.395	0.926	2.529
'outm'	2	0.4	0.94	0.7094	0.1419
'AVDD'	3	0.5	14.14	0.913	1.708
'AVDD'	2	1.7	1.14	0.6911	0.0405
'outp'	2	0.665	2.269	0.8855	0.2057
'AVSS'	2	1.6	1.74	0.7797	0.06568
'AVDD'	2	0.69	0.94	0.8415	0.08228
'outp'	2	0.665	0.94	0.85	0.08538
'AVDD'	2	1.7	1.14	0.6804	0.0405
'net044'	2	0.25	1.14	0.2228	0.2754
'AVDD'	2	1.7	1.14	0.6696	0.0405
'net019'	2	0.25	1.1	0.3156	0.2658
'net019'	2	0.25	1.13	0.3156	0.273
'outp'	2	0.665	0.94	0.7792	0.08538
'AVSS'	2	1.6	1.74	0.718	0.06568
'net044'	1	0.06	0.375	0.08899	0.2879
'net044'	1	0.06	0.375	0.08899	0.2879
'net044'	1	0.06	0.375	0.08899	0.2879
'net044'	1	0.06	0.375	0.08899	0.2879
'AVDD'	2	0.08	1.54	0.332	0.954
'AVDD'	2	0.08	1.54	0.332	0.954
'AVDD'	2	0.08	1.54	0.332	0.954
'net22'	1	0.4	7.435	0.1762	1.367
'net22'	1	0.4	9.605	0.1762	1.767
'net22'	1	0.4	4.845	0.1762	0.8906
'net14'	2	0.08	1.54	0.3253	0.954
'net14'	2	0.08	1.54	0.3253	0.954
'net14'	2	0.08	1.54	0.3253	0.954
'AVSS'	2	1.6	1.74	0.3182	0.06568
'outm'	2	0.4	0.94	0.2365	0.1419
'net044'	1	0.25	1.145	0.08104	0.333
'net019'	1	0.12	0.835	0.1217	0.5167
'net019'	1	0.12	0.835	0.1217	0.5343
'AVDD'	2	1.7	1.14	0.2832	0.0405
'AVDD'	2	0.69	0.94	0.2955	0.08228
'AVDD'	2	0.65	0.94	0.2661	0.08735
'AVDD'	1	0.1	0.295	0.2848	0.1873
'outp'	2	0.665	0.94	0.2833	0.08538
'net044'	2	0.25	1.14	0.07428	0.2754
'net019'	2	0.25	0.94	0.1114	0.2271
'AVDD'	2	1.7	1.14	0.2724	0.0405
'net019'	2	0.25	0.94	0	0.2271
'AVDD'	2	1.7	3.136	0.267	0.1114
'net019'	2	0.25	0.94	0.1114	0.2271
'net019'	2	0.25	1.74	0.1052	0.4204
'AVDD'	1	0.18	8.82	0.2518	3.455

Table G.3 – EDA data of the Opamp paths.

Path	Layer	W (μm)	L (μm)	J/j_{max}	R (ohm)
'AVDD'	1	0.18	6.395	0.926	2.529
'AVDD'	1	0.18	17.605	0.2518	6.931
'AVDD'	1	0.18	17.605	0.2518	6.931
'AVDD'	1	0.18	7.275	0.2518	2.857
'AVDD'	1	0.18	5.995	0.2518	2.353
'AVDD'	2	0.65	0.94	0.1936	0.08735
'outp'	2	0.4	1.74	0.2443	0.2627
'outm'	2	0.4	1.74	0.2443	0.2627
'AVSS'	2	1.6	1.74	0.2273	0.06568
'AVDD'	2	0.69	0.94	0.2272	0.08228
'AVDD'	2	0.08	1.54	0.2236	0.954
'AVDD'	2	0.08	1.54	0.2236	0.954
'AVDD'	2	0.08	1.54	0.2236	0.954
'net14'	1	0.25	11.41	0.2193	3.359
'net14'	2	0.08	1.54	0.2169	0.954
'net14'	2	0.08	1.54	0.2169	0.954
'net14'	2	0.08	1.54	0.2169	0.9853
'net019'	2	0.25	0.94	0.2166	0.2271
'outp'	2	0.665	0.94	0.2125	0.08538
'net22'	2	0.25	1.14	0.1114	0.2754
'net019'	1	0.12	2.1	0.06085	1.236
'AVDD'	2	0.69	0.94	0.7733	0.08228
'outm'	2	0.4	0.94	0.5912	0.1419
'AVDD'	2	1.7	1.14	0.6588	0.0405
'outp'	2	0.4	17.405	0.7328	0.2627
'outm'	2	0.4	1.745	0.7328	0.2635
'AVDD'	2	1.7	1.14	0.648	0.0405
'outp'	2	0.665	0.94	0.7084	0.08538
'AVDD'	2	0.69	0.94	0.705	0.08228
'AVDD'	2	0.65	2.508	0.701	0.2328
'AVSS'	2	1.6	1.71	0.6856	0.06455
'AVDD'	2	1.7	1.14	0.6373	0.0405
'AVDD'	2	1.7	1.14	0.6258	0.0405
'AVDD'	2	1.7	1.14	0.6137	0.0405
'net14'	1	0.25	7.205	0.6579	2.121
'AVSS'	2	1.6	1.74	0.64	0.06568
'outp'	2	0.665	0.94	0.6375	0.08538
'AVDD'	2	0.69	0.94	0.6368	0.08228
'AVDD'	2	0.65	0.94	0.6285	0.08735
'AVDD'	2	1.7	1.14	0.5755	0.0405
'outm'	2	0.4	0.94	0.473	0.1419
'net14'	2	0.25	0.29	0.6031	0.07006
'net14'	2	0.25	3.735	0.6031	0.9024
'outm'	2	0.65	0.02	0.599	0.001858
'AVDD'	2	0.69	0.94	0.5685	0.08228

Table G.4 – EDA data of the Opamp paths.

Path	Layer	W (μm)	L (μm)	J/j_{max}	R (ohm)
'outp'	2	0.665	0.94	0.5667	0.08538
'AVDD'	2	1.7	1.14	0.5112	0.0405
'AVSS'	2	1.6	1.74	0.549	0.06568
'net044'	2	0.25	1.14	0.1486	0.2754
'AVDD'	2	0.65	0.94	0.556	0.08735
'AVDD'	1	0.18	6.395	0.926	2.529
'AVDD'	2	0.08	1.45	0.5556	0.8894
'AVDD'	2	0.08	1.45	0.5556	0.8894
'AVDD'	2	0.08	1.45	0.5556	0.9287
'AVDD'	1	0.18	11.41	0.5334	4.499
'net019'	2	0.25	1.74	0.2104	0.4204
'AVDD'	2	0.69	0.94	0.5003	0.08228
'AVDD'	2	1.7	1.14	0.4469	0.0405
'outp'	2	0.665	0.94	0.4959	0.08538
'outp'	2	0.4	17.405	0.4886	0.2627
'outm'	2	0.4	1.73	0.4886	0.2612
'net22'	2	0.25	6.77	0.26	1.636
'net22'	2	0.25	10.35	0.26	2.499
'AVDD'	2	0.65	0.94	0.4835	0.08735
'AVSS'	2	1.6	1.74	0.4579	0.06568
'outm'	2	0.4	0.94	0.3547	0.1419
'net019'	2	0.25	0.94	0.2166	0.2271
'net044'	1	0.06	0.225	0.1187	0.1804
'net044'	1	0.06	0.225	0.1187	0.1934
'net044'	1	0.06	0.1875	0.1187	0.1407
'AVDD'	2	0.08	1.54	0.4405	0.954
'AVDD'	2	0.08	1.54	0.4405	0.954
'AVDD'	2	0.08	1.54	0.4405	0.954
'net14'	1	0.25	11.41	0.4386	3.359
'net14'	2	0.08	2.525	0.4338	1.57
'net14'	2	0.08	2.525	0.4338	1.57
'net14'	2	0.08	2.525	0.4338	1.57
'AVDD'	2	1.7	1.14	0.3826	0.0405
'AVDD'	2	0.69	0.94	0.432	0.08228
'outp'	2	0.665	0.94	0.425	0.08538
'net14'	1	0.1	2.505	0.4215	1.602
'AVDD'	2	0.65	0.94	0.411	0.08735
'AVDD'	2	1.7	1.14	0.3444	0.0405
'AVDD'	2	1.7	1.14	0.3323	0.0405
'AVDD'	2	1.7	1.14	0.3263	0.0405
'Ibias'	1	0.08	11.41	0.3987	8.398
'AVSS'	2	1.6	1.74	0.3961	0.06568
'AVDD'	2	1.7	1.14	0.3155	0.0405
'net019'	1	0.13	2.105	0.05274	1.195
'Ibias'	2	0.08	1.65	0.3655	0.9966
'AVDD'	2	0.69	0.94	0.3637	0.08228
'AVSS'	2	1.6	1.71	0.3637	0.06455