TIAGO DAVI CURI BUSARELLO

STUDY AND DEVELOPMENT OF MULTILEVEL INVERTERS FOR APPLICATIONS IN INTELLIGENT DISTRIBUTION SYSTEMS

ESTUDO E DESENVOLVIMENTO DE INVERSORES MULTINÍVEIS PARA APLICAÇÕES EM REDES INTELIGENTES DE DISTRIBUIÇÃO DE ENERGIA ELÉTRICA

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Faculdade de Engenharia Elétrica e de Computação

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Thesis presented to the School of Electrical and Computer Engineering of the University of Campinas in partial fulfillment of the requirements for the degree of Doctor in Electrical Engineering, in the area of Electrical Energy

Tese apresentada à Faculdade de Engenharia Elétrica e de Computação da Universidade Estadual de Campinas como parte dos requisitos exigidos para a obtenção do título de Doutor em Engenharia Elétrica, na Área de Energia Elétrica.

Orientador: JOSÉ ANTENOR POMILIO
Coorientador: HELMO KELIS MORALES PAREDES

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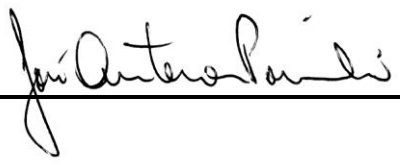

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"O homem é do tamanho do seu sonho"

Fernando Pessoa

Aos meus pais Honorato Busarello (in memoriam) e Judite Jalile Curi Busarello.

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ABSTRACT

Distributed generation systems have become common along the last years due to the development of renewable energy sources. Additionally, storage technologies and their respect power converters have been added into the system in order to store and to supply energy in suited moments. By aiming the reliability, uninterrupted supplying, efficiency and stability, centralized controllers were implemented in distributed system, making them to be entitled smart-grids. Such controllers manage the operation modes of the system generators and converters. This thesis presents a research project covering the study and development of multilevel converters for applications in intelligent distribution systems. The study approaches the cascaded symmetrical and asymmetrical topologies, indicating the main concepts about the structure, the modulation, the power distribution across the modules, the output filter and the current and voltage controllers, among others. Afterwards, the thesis proposes an Interactive Battery-Based Storage system. The interaction makes the storage to be able to perform ancillary functions and to operate coordinately with centralized and local controllers. Decisions on the operation mode are taken based on specific rules. Additionally, a synergistic operation is achieved when the Interactive Battery-Based Storage works with another intelligent power device. Concepts about micro and smart-grids are also presented in order to clarify how the proposed intelligence contributes to the smart-grid realization. The efficacy of the study and the proposed IBBS were verified through simulation and experimental results.

RESUMO

Sistemas com geração distribuída têm se tornado comum ao longo dos últimos anos devido ao crescente aproveitamento de fontes renováveis de energia. Nesse contexto, acumuladores de energia e seus conversores de potência têm sido adicionados ao sistema com a finalidade de armazenar e fornecer energia em momentos oportunos. Com a finalidade de garantir confiabilidade, fornecimento interrupto, eficiência e estabilidade, sistemas de supervisão e de controle devem ser implementados em tais redes, caracterizando-as como sistemas inteligentes. Tais sistemas devem coordenar os modos de operações dos geradores e conversores. Esta tese apresenta um projeto de pesquisa que abrange o estudo e desenvolvimento de inversores multiníveis para aplicações em sistemas inteligentes de distribuição. O estudo aborda as topologias cascatas simétrica e assimétrica, indicando os principais conceitos sobre a estrutura, a modulação, a distribuição de potência nos módulos, o filtro de saída e os controladores de corrente e tensão, além de outros. Além disso, a tese propõe um sistema armazenador à baterias interativo. A interação faz com que o armazenamento seja capaz de realizar funções auxiliares e de operar em redes com controle local e centralizado. As decisões sobre o modo de operação são tomadas com base em regras específicas. Uma operação sinérgica é atingida quando o armazenador opera em conjunto com outro dispositivo inteligente. Conceitos sobre rede inteligentes são apresentados a fim de esclarecer como a inteligência proposta contribui para a realização das smart-grids. A eficácia do estudo e da inteligência proposta é verificada através de simulação e de resultados experimentais.

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LIST OF ABBREVATIONS

AD	Analog to Digital
ACMI	Asymmetrical Cascaded Multilevel Inverter
APOD	Alternative Phase Opposition Disposition
BBS	Battery-Based Storage
BMS	Battery Monitoring System
CPT	Conservative Power Theory
DAC	Digital to Analog Converter
DER	Distributed Energy Resource
DG	Distributed Generator
GTO	Gate turn-off thyristor
IBBS	Interactive Battery-Based Storage
IGCT	Integrated gate-commutated thyristor
MMT	Modular Multilevel Topology
PCC	Point of Common Point
PD	Phase Disposition
PLL	Phase-Locked Loop
PI	Proportional-Integrator
POD	Phase Opposition Disposition
PR	Proportional Resonant
PV	Photo Voltaic
PWM	Pulse Width Modulation
SCMI	Symmetrical Cascaded Multilevel Inverter
SO	System Operator
SOC	State-of-Charge
SOH	State-of-Health
SPI	Serial Peripheral Interface
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Compensator
THD	Total Harmonic Distortion
UPS	Uninterrupted Power Source
WG	Wind Generator

CONTENT

1 INTRODUCTION

The usage of multilevel converters proliferated in the last years, motivated mainly by the possibility of handling great amount of power directly in the medium voltage without the need of using bulky transformers. Additionally, high quality signals with low commutation frequency can be achieved. As result, the filtering requirements are reduced and the production of electromagnetic radiation. Multilevel converters have also niche of application in low voltage systems. The feature of modularity increases the reliability of the device, making them attractive choices for new applications [1], [2].

At the same time, issues about smart-grids have taken the spotlight of the industrial and academia sectors involved with electrical energy. The United States Department of Energy defines that "a smart grid is self healing, enables active participation of consumers, operate resiliently against attacks and natural disasters, accommodate all generation and storage options, enable introduction of new products, services and markets, optimize asset utilization and operate efficiently, provide power quality for the digital economy" [3], while the European Technology Platform Smart Grid states that "a smart grid is an electricity network that can intelligently integrate the actions of all users connected to it –generators, consumers and those that do both – in order to efficiently deliver sustainable, economic and secure electricity supply" [4].

Independently of definitions, smart grid brought new challenges to electrical sector. Phenomena which were once unworried must be thoroughly considered in smart-grid implementation. Some examples are reverse power flux in classical unidirectional grids, grid parameter variation caused by the high penetration of distributed generators, the necessity of a centralized controller as a decision-taker and so on. Little-by-little, accurate solutions are presented in the literature in order to overcome such issues. Consequently, the smart-grid scenario starts to be a reality.

Two indispensable elements for smart-grid realization are Distributed Generators (DG) and storages. DG systems become common along the last years due to the development of renewable energy sources while storage technologies were added into the system in order to store and to supply energy in suited moments.

Reports have demonstrated that generators based on renewables will represent a meaningful percentage of the total world energy production, with a prediction of around 80% by 2050 in United States [5]. Certainly, such scenario will be achieved with a high penetration

of storage. Storage play an important role to support the temporal mismatch between generation and consumption and to compensate the intermittent behavior of renewable sources. Batteries are a promising technology for storages. Several hurdles found in batteries are being broken. One of them is the possibility to recycle 99% of total weight of sodium-sulphur batteries [6].

By aiming the reliability, uninterrupted supplying, stability and mainly a coordinated performance of the DGs and storages, centralized and local controllers must be implemented. Such controllers manage the operation of the system by defining the set-points of the DGs. But in order to make a conventional grid to be smart, the power electronic converters used in DG, storage and other power devices must be capable to perform ancillary services. For example, functions like harmonic compensation may be performed by a converter in a PV system when there is no available energy to be injected into the electrical system. For that purpose, the converter must be equipped with ability to communicate to local and central controllers and to take decision depending on the exchanged information.

Given the current strength of multilevel converters and the claim for smart-grids realization, this thesis presents the study and development of multilevel inverters for applications in intelligent distribution systems. The study covers the cascaded symmetrical and asymmetrical topologies, detailing the main concepts about the structure, the modulation, the power distribution across the modules, the output filter and the current and voltage controllers. The study is for general applications. Later, the thesis proposes an Interactive Battery-Based Storages (IBBS). The interaction makes a BBS (Battery-Based Storage) capable to operate in grids with centralized and local controllers. The IBBS exchanges information with the central controller, such as the current battery state-of-charge (SOC) and the power delivered by a DG. Moreover, the IBBS combined to another interactive power electronic device makes a synergistic operation of whole system, contributing to the smart-grid realization.

The thesis is divided as follow:

Chapter 2 presents the objectives and justification of the research project, showing the advantage of using multilevel converters, in the symmetrical and asymmetrical topologies, over the classical H-bridge in a storage application. Four figures of merit are used: power losses, semiconductor sizing, output filtering and operation under occurrence of fault. Additionally, the need of aggregating intelligence in power electronic devices is explained through the presentation of small scale smart-grid projects.

Chapter 3 and 4 presents the study and implementation of a Symmetrical Cascaded Multilevel Inverter (SCMI) and Asymmetrical Cascaded Multilevel Inverter (ACMI), respectively. Initially, the structure and the modulation are presented. Afterwards, the power distribution and the DC-link currents are analyzed. The chapters continue by presenting how to design the output filter and how to implement closed-loop current control. The procedure for tuning the controller parameters is described. Chapter 3 presents the closed-loop control system to control the DC-link voltage in SCMI while Chapter 4 just presents the challenges to control such voltage in ACMI. Chapter 4 also presents the possibility of employing the ACMI in BBS without the need of changing the physical structure. The procedure to control the AC voltage is presented in Chapter 4. These chapters are intended to contribute to applications with ACMI and SCMI topologies.

Chapter 5 summarizes the features found in SCMI and ACMI topologies. A brief comparison followed by comments is presented. The comparison is restricted to the topologies with three modules.

Chapter 6 presents a proposal of an Interactive Battery-based System (IBBS). Additionally, concepts about smart-grids are presented in order to clarify how the interaction contributes to the smart-grid realization. The chapter begins presenting the Phase-Locked Loop (PLL) and technical impacts caused by the connection of DG in electrical grids. Further, methods for estimating the battery State-of-Charge (SOC) and State-of-Health (SOH) are presented. Descriptions about how the IBBS is able to perform ancillary functions and to operate in smart micro-grid with centralized and local controllers are presented. The IBBS exchanges information with these controllers and decisions are taken based on specific rules. Additionally, a synergistic operation is achieved when the proposed IBBS works coordinately with another intelligent power electronic device.

Chapter 7 presents general conclusions and suggestions for future work. The potential of extension of the research project is described.

Appendix A presents other multilevel topologies. The diode-clamped, the pyramidal diode-clamped, the flying capacitor, the modular and hybrid topologies are presented. The presentation is conditioned to the power structure, describing advantages and disadvantages.

Appendix B presents brief details about storage technologies, such as those based on pumped hydro, compressed air, battery, flywheel, capacitor and supercapacitor. The battery storage receives special attention. Some chemistry technologies are described. At the end, some battery storage systems installed worldwide are presented.

Appendix C shows details about the simulation of the SCMI. All the circuits used in the simulation are presented.

Appendix D presents how the effect of a disturbance can be minimized in a closed-loop system. A disturbance appears in Chapter 3 and 4 during the procedure of modeling the systems.

Appendix E shows details about the simulation of the ACMI.

Appendix F shows details about the simulation of the smart micro-grid.

Appendix G presents details about the smart micro-grid prototype. A general schematic as well as the circuits are presented.

Appendix H presents the publications along the doctorate course. Partial and final results of the research project were published in international periodicals and conferences.

All simulations were done in PowersimTech PSIM software with code generation. Code generation means the software generates the C-code based on the elements used in the simulation. The microcontroller used in the prototypes is the floating-point TMS320F28335, from Texas Instruments. The simulation and experimental results are presented side-by-side for better visualization. When limitations appeared to either simulation or experimentally, the results are presented alone. All current and voltage measured experimentally were collected by probes in 0.1V/A and 1mV/V, respectively, except differently specified.

The simulation files used in this thesis are freely available on https://sites.google.com/site/busarellosmartgrid/home

2 OBJECTIVES AND JUSTIFICATION

The objectives and justifications of the research project are described by evaluating a typical application scenario. The first objective is to study and to implement cascaded multilevel inverters in symmetrical and asymmetrical structures.

Uninterrupted Power Supply (UPS) usually use batteries as storage element and CC-AC converter as device to handle the energy [7]. The batteries are connected in series in order to guarantee the full power flux control. Figure 2:1 presents a simplified diagram of a storage system connected to an electrical grid. The storage system is composed by batteries, a H-bridge converter and an output filter. The batteries are considered a bank of battery. The inductor *L* belongs to the electrical grid.

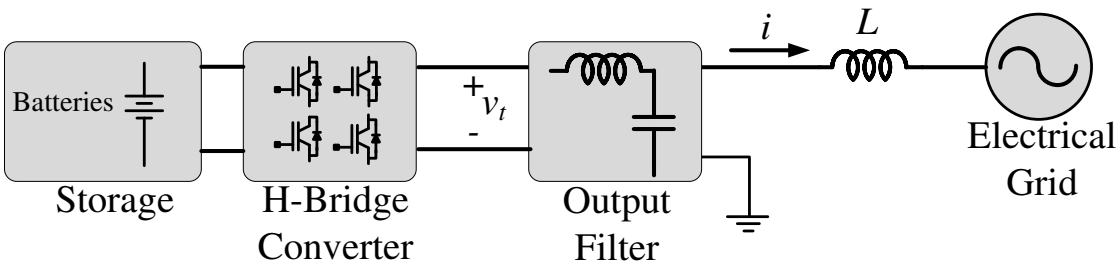


Figure 2:1 - Simplified diagram of a classical storage system connected to the electrical grid.

Four figures of merit can be highlighted in a storage system: (i) power losses, because reducing them may enlarge the discharging capacity; (ii) semiconductor sizing, since its cost tends to rise as the blocking voltage increases; (iii) output filtering, because the delivered power should fit power quality levels and (iv) operation under fault, since full interruption is undesirable.

The power losses are the conduction and switching losses [8], [9]. The switching losses occur when a transistor turns on and off. Such transitions are not instantaneous, resulting in a non-null product of the voltage and current. Figure 2:2 presents the switching characteristics in a transistor. The signal applied to the transistor collector-emitter (drain-source is presented in Figure 2:2a, with T_{sw} being the switching time period. Figure 2:2b presents the voltage and collector (drain) current. When the transistor is on, the current *I* flows for an inductive load, that is the general case. When the transistor is off, the voltage *V* appears between collector and emitter (drain and source). During the turn-on transition, the current buildup consists of a short delay time ($t_{d(on)}$) followed by the current rise time (t_{ri}). Only after the current *I* flows entirely through the transistor the voltage falls to a small on-state value of V_{on}, with a voltage fall time of (t_{vf}).

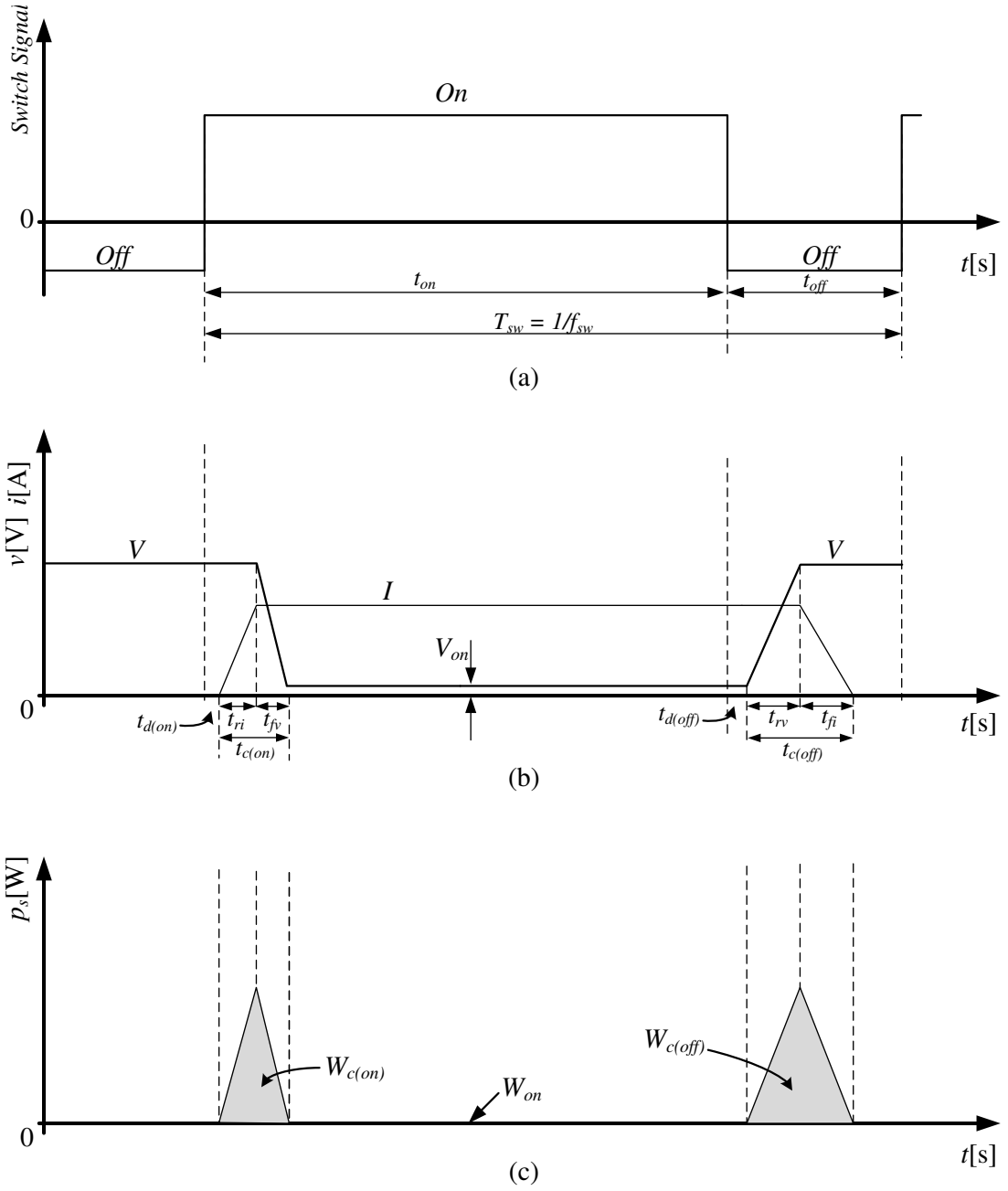


Figure 2:2 - Switching characteristics in a transistor. (a) switch gate signal, (b) voltage and current across the transistor, (c) instantaneous switching losses.

A large values of transistor voltage and current are present simultaneously during the turn-on interval ($t_{c(on)}$), where

$$t_{c(on)} = t_{ri} + t_{fv} \tag{2.1}$$

The energy dissipated during the turn-on transition can be approximated as given in (2.2).

$$W_{c(on)} = \tfrac{1}{2} V I t_{c(on)} \tag{2.2}$$

Once the transistor is fully on, the on-state voltage V_{on} will be on the order of a volt depending on the device, and the transistor conducts the current I. The transistor remains

in conduction during the interval t_{on}, which in general is much larger than the turn-on and turn-off transition times. The energy dissipated W_{on} during the this on-state interval is given by (2.3).

$$W_{on} = V_{on} I t_{on} \tag{2.3}$$

In order to turn the transistor off, the command signal is removed. During the turn-off interval, the voltage buildup consists of the turn-off delay time $t_{d(off)}$ and a voltage rise time t_{rv}. Once the voltage reaches its final value V, the current I falls to zero with a current fall time t_{fi}. Again, large values of voltage and current occur simultaneously during the crossover interval $t_{c(off)}$, where

$$t_{c(off)} = t_{rv} + t_{fi} \tag{2.4}$$

The energy dissipated in the switch during this turn-off interval is given by (2.5).

$$W_{c(off)} = \frac{1}{2} V I t_{c(off)} \tag{2.5}$$

The instantaneous power makes clear that a large power dissipation occurs in the transistor during the turn-on an turn-off intervals. Hence, the average switching power loss in the transistor due to these transitions can be approximately given by (2.6).

$$P_{sw} = \frac{1}{2} V I f_{sw} \left(t_{c(on} + t_{c(off)} \right) \tag{2.6}$$

where f_{sw} is the switching frequency.

Equation (2.6) shows that the switching power losses in a transistor increases as the switching frequency increases.

The other major contribution to the losses in the power dissipated during the on-state, which varies in proportion to the on-state voltage. The conduction power losses is given by (2.7).

$$P_{on} = V_{on} I \frac{t_{on}}{T_{sw}} \tag{2.7}$$

One of the criteria to size a transistor is to know its drain to source blocking voltage (or collector to emitter) in the cut-off region [10], [11]. In Figure 2:1, such voltage is equal to the total voltage from the series connected batteries. Figure 2:3 presents a simplified diagram for the visualization of the drain to source voltage in a transistor. The transistors were replaced by simplified switches for better visualization.

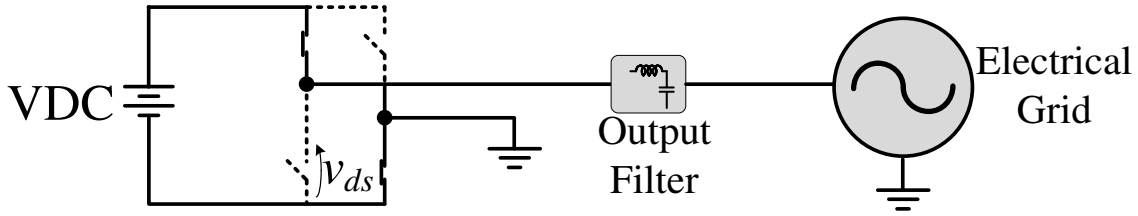


Figure 2:3 - Simplified diagram for visualization of the drain to source voltage in a transistor.

When the upper-left transistor is ON, the bottom-left transistor is in parallel to the batteries. Therefore, the voltage across the transistor is given by (2.8).

$$v_{ds} = VDC \tag{2.8}$$

Such feature also dictates the technology of the transistors. High VDC voltage requires devices with bulk-power capability, like IGBTs, GTOs or IGCTs. On the other hand, low VDC voltages allow the use of MOSFETs.

The parameters of the output filter can be considered as figure of merit mainly because its volume. Bulky filters make the system heavier and more expansive. The volume of a passive filter is proportional to its developed effort. Strictly, a passive filter makes relatively high effort when the desired output waveform is far from the input waveform [12], [13]. In Figure 2:1, the input signal of the output filter is a square or quasi-square waveform, depending on the modulation, and the desired output signal is a sinusoidal waveform. In this case, the developed effort is to attenuate all frequencies higher than the fundamental. One manner to reduce the filter volume, while maintaining the required attenuation, is to increase the switching frequency. However, such action increases the switching losses.

In terms of reliability, still in Figure 2:1, if a transistor fails, the H-bridge converter becomes unable to keep working. Consequently, the storage system operation is fully interrupted.

As the DC source is composed by batteries, the use of cascaded multilevel inverters seems to be an attractive option by many reasons: the need of isolated DC sources is easily implemented; the improvement of the inverter output waveform allows the reduction of output filter effort and, in some cases, the modularity structure allows redundancies that improve the overall system reliability. Figure 2:4 presents the concept of dividing the batteries into three equal banks.

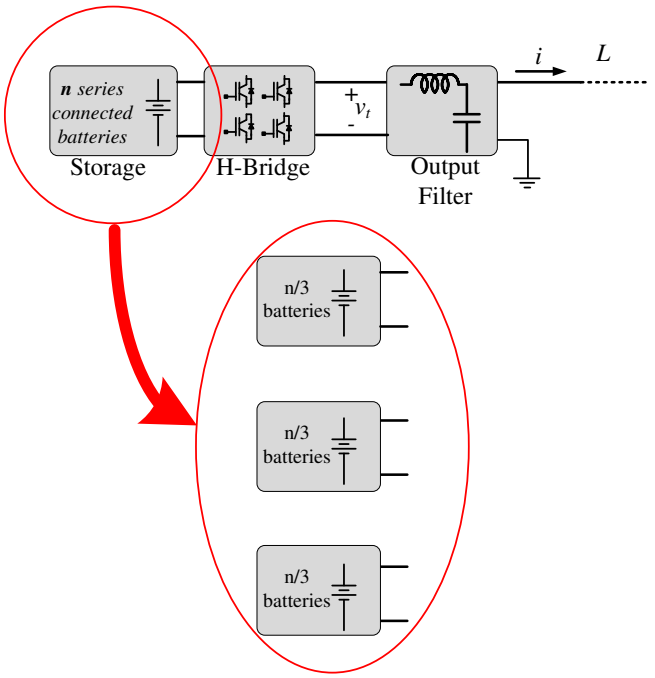


Figure 2:4 - The concept of dividing the batteries into three equal banks.

An H-bridge converter is connected to each battery bank. Later, their output terminals are series connected, resulting the Symmetrical Cascaded Multilevel Inverter (SCMI). Figure 2:5 presents the SCMI topology with three banks of battery. Each bank of battery plus the H-bridge converter is defined as a module. Therefore, the SCMI has three modules.

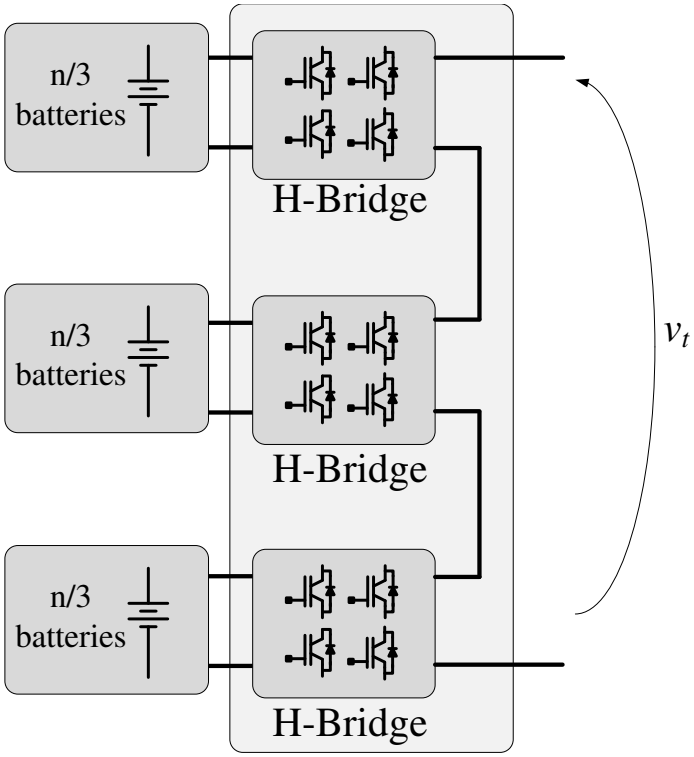
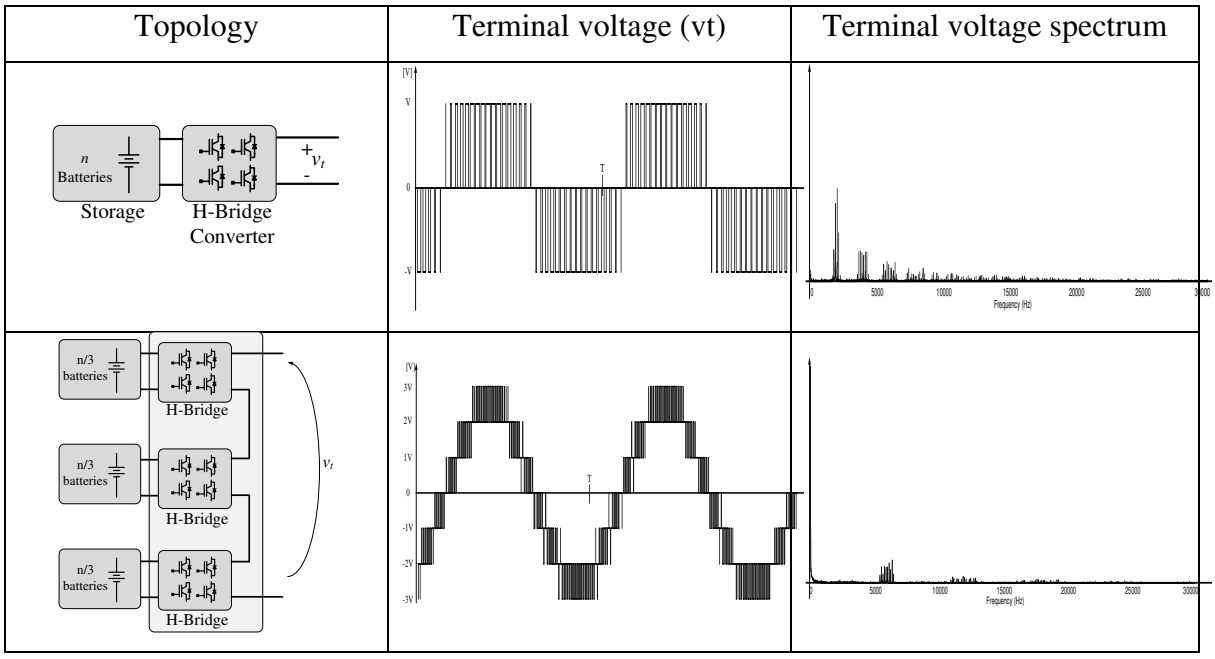


Figure 2:5 - The SCMI topology with three banks of battery.

Evaluating the same figures of merit and comparing them to the classical storage system, the drain to source voltage is lower. In this case, it is one third of the bank of battery. The transistors are sized with lower blocking voltage. Therefore, the cost is expected to be lower. The switching losses are lower not only due to the lower reverse voltage, but also due to a SCMI feature of applying low switching frequency. By a suited modulation technique, the SCMI terminal voltage presents spectral components two times higher than the product of number of module by the switching frequency of each module [1]. Board 2:1 presents a comparison of the terminal voltage and their spectrum between the SCMI and the classical topology. Each H-Bridge has PWM technique with switching frequency equals to 1 kHz. The SCMI terminal voltage has spectral components around 6 kHz and its multiples.

Board 2:1 – Comparison of the terminal voltages and their spectra between the SCMI and the classical PWM topology.



The terminal voltage is the signal applied to the input of the output filter. In the SCMI, the waveform is closer to a sinusoidal than the classical topology. As result, the required attenuation is lower and the output filter tends to have lower volume.

The use of several modules allows, in some cases, the uninterrupted operation under fault. In order to guarantee the continuity of the operation, the fault is limited to one of the modules. The remaining modules must have a total DC voltage higher than the peak voltage of the electrical grid. In occurrence of fault, the SCMI keeps working by-passing the module under failure. Figure 2:6 presents the continuity of operation when one module fails. The fail can be in the battery bank or in the H-bridge converter. A by-pass is applied through

the converter terminal. One of the possibilities to bypass a module is simply keeping turned on the upper transistors (or the lower) in the corresponded H-bridge converter.

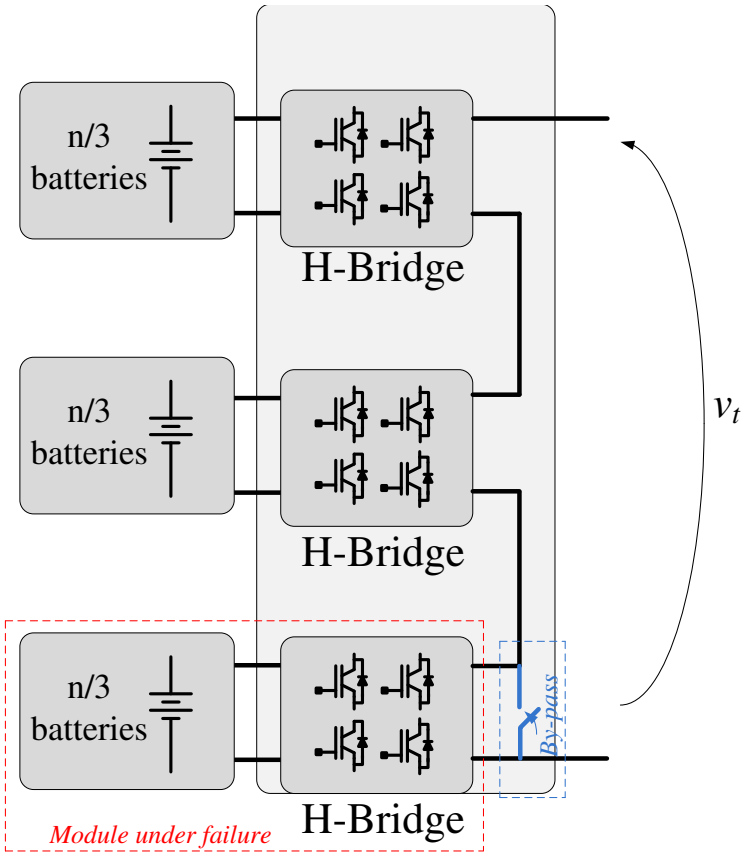


Figure 2:6 - Continuity of the operation when one module is under failure.

The batteries were divided into equal banks. Nevertheless, the division could occur in different banks. The banks could be divided in the ratio {1:2:6:…} and {1:3:9,…}, among others, related to total available batteries. Figure 2:7 presents the division of the batteries into three different banks. The ratio among the batteries is {1:2:6}.

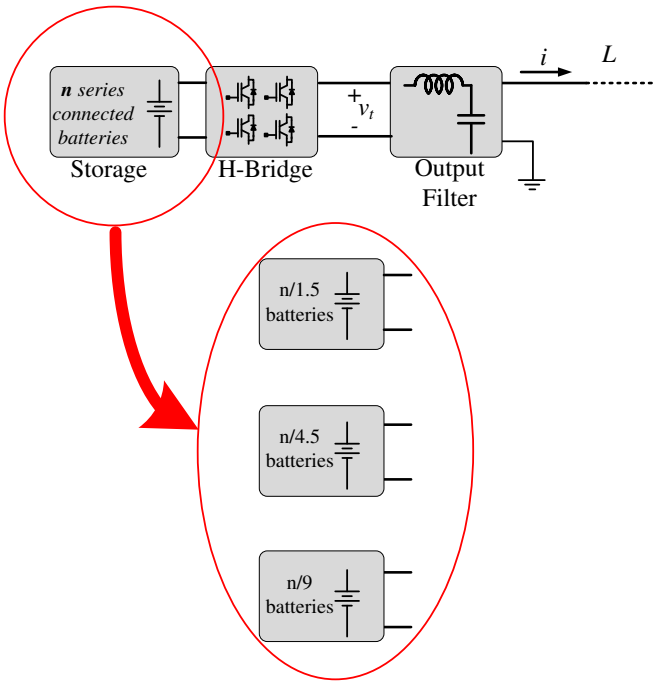


Figure 2:7 - Division of the batteries into three different banks.

Similarly, by connecting one H-bridge converter to each battery bank and series connecting their outputs, the SCMI is obtained. Figure 2:8 presents the Asymmetrical Cascaded Multilevel Inverter (ACMI) topology with three different banks.

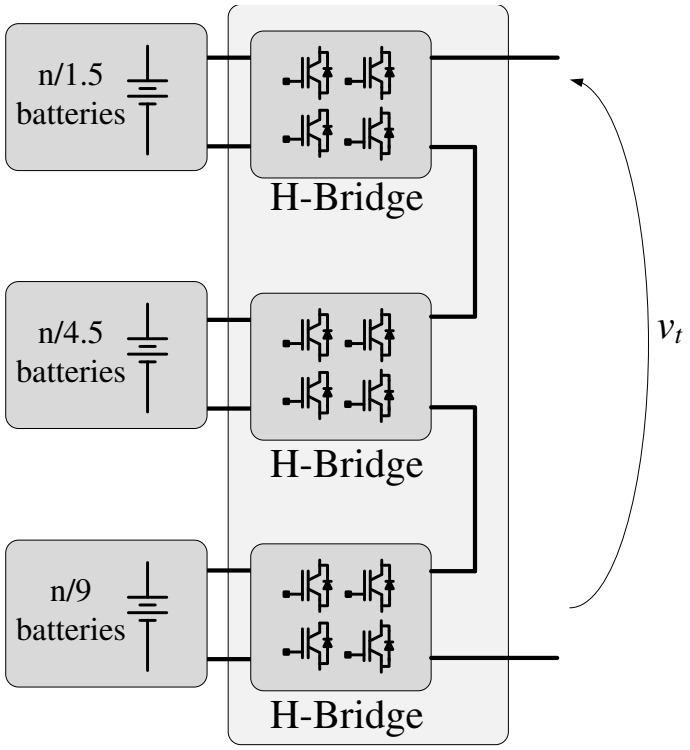


Figure 2:8 - ACMI topology with three different banks.

The evaluation of the figures of merit is similar to those for SCMI. However, the ACMI has some specific features. The upper module has the great part of the batteries.

Consequently, the most part of the total power is processed on it. The operation under fault is restricted to the lower modules.

The SCMI and ACMI are attractive topologies. The switching losses are reduced compared to a classical PWM inverter, semiconductors with lower power rate may be used, the output filter can have relative low volume and the system can keep working even under occurrence of fault [14]–[17]. Therefore, the first objective of the research project is justified. Presenting the study and implementation of SCMI and ACMI contributes to the applications based on these topologies. Relevant features are presented in the next chapters, as modulation strategy, power distribution, current and voltage control, among others.

But currently, the main stream in the electrical sector is the smart-grids. A possible smart-grid consist of the main generation, usually provided by the connection with the distribution grid, distributed generators, storage devices, electrical vehicle, linear and nonlinear load, agents behaving as producer and consumer, the so-called prosumers, etc., and all of them equipped with Information and Communication Technology (ICT). Central and local controllers should manage the local grid in order to guarantee stability, reliability, uninterrupted supply and coordinated operation among the devices. Figure 2:9 presents a typical concept of a smart grid [18].

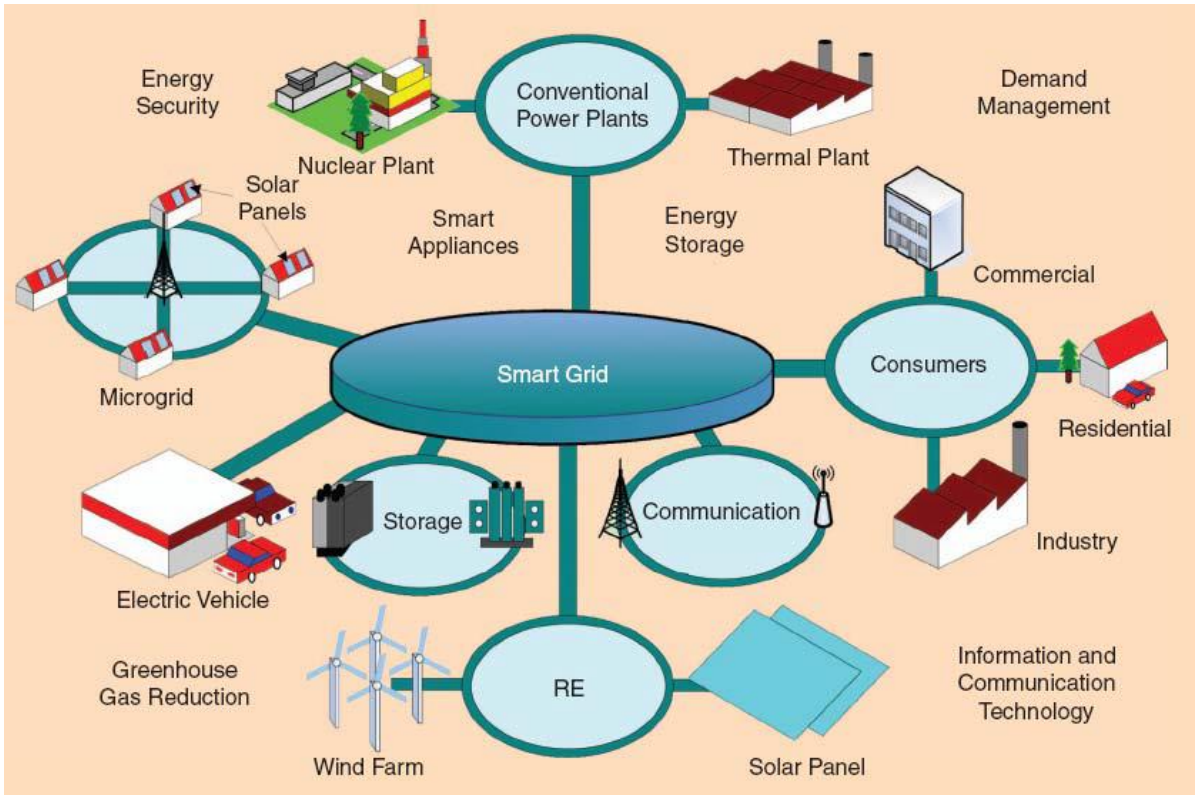


Figure 2:9 – Typical concept of a smart grid [18].

A number of real smart-grids are already in operation worldwide as off-grid application, pilot cases and full-scale demonstration. In European Union, the forces to develop smart-grids were motivated mainly by "Strategic Research Agenda for Europe's Electricity Networks of the Future" [19] and the project "More Microgrids" [20]. In United States, two major R&D and demonstration programs going on currently are Smart Power Infrastructure Demonstration for Energy, Reliability and Security (SPIDERS) [21], run by the Department of Defense, and Renewable and Distributed Systems Integration (RDSI) [22], run by the Department of Energy. Similar agendas and project are running in Asia and Latin America. Some of the smart-grids worldwide are presented in Table 2.1.

Table 2:1 - Some of the smart-grids worldwide.

Site (responsible partner)	**Location**	**Technologies/Feature**
Santa Rita Jail, Chevron Energy Solutions – CERTS microgrid demonstration [23]	USA	large-scale energy storage, PV, fuel cell
University of Nevada Las Vegas – "Hybrid" Homes: dramatic residential demand reduction in the desert southwest [24]	USA	PV, advanced meters, in-home dashboard, automated DR, storage
Promontory, ATK Space Systems – powering a defense company with renewables	USA	hydro-turbines, compressed air storage, solar thermal, wind turbines, waste heat recovery system
Gaidouromantra on Kythnos Island [25]	Greece	residential/island
Bornholm Island [26]	Denmark	multi-microgrid/island
Condor Sustainable Electrification Project	Chile	Off-grid
Demonstrative Project of Regional Power Grids with Various New Energies – NEDO [27]	Japan	Demonstrative grid-tied microgrid

From the smart-grid point of view, conceiving a storage system based on SCMI or ACMI makes no difference from the classical storage structure. The storage system is just another device in the smart-grid. The advantages within the structure and how the inner power

is processed do not matter for the grid. It does not matter to the smart-grid if the inner structure of a storage has four or twelve transistor and how big is the output filter. The grid would rather to count on the storage to contribute and to support in the operation of the smart-grid. Therefore, one of the objectives of the research project is to propose an Interactive Battery-Based Storage (IBBS). The interaction means the capability of the BBS to operate coordinately with local and centralized controllers and to perform ancillary functions. Moreover, the BBS in conjunction to other interactive elements may result in a synergist operation of the grid. Concepts about smart-grids are also presented in order to clarify how the interaction contributes to the smart-grid realization.

The last objective is to build an experimental setup in order to verify the efficacy of the study and the proposal presented in this thesis.

Table 2:2 summarizes the objectives and a brief justification of the research covered this thesis.

Table 2:2 - Objectives and a brief justification of the research covered in this thesis.

Objective	**Brief Justification**
Study and implementation of cascaded multilevel inverter in symmetrical and asymmetrical structures for general applications	The current strength of multilevel converters and their advantages over classical H-Bridge inverters
Propose an Interactive Battery-Based Storage	The claim for smart-grids realization
Build an experimental setup	Experimental verification of the study and the proposal

3 STUDY AND IMPLEMENTATION OF SYMMECTRICAL CASCADED MULTIVEL INVERTER

This chapter presents the study and implementation of a SCMI [15], [28]. Initially, the study is conducted through the analysis of a SCMI with *n* series connected modules. Later, a SCMI with three modules is implemented and the studies are directed to such configuration. The goal is to contribute to the design of SCMI. Some issues are the single- and three-phase structures, modulation, power distribution, output filter and closed-loop control. The studies apply for storage applications, but are not limited to. The concepts are verified through simulation and experimental results. Details about the simulation are given in Appendix A.

3.1 The symmetrical cascaded multilevel inverter

Figure 3:1 presents a single-phase *l*-level SCMI with *n* modules. Each module has an isolated DC source and their output voltages can present three possible values. The SCMI terminal voltage is called v_t while the module terminal voltages are called v_{t1}, v_{t2} and v_{tn}, respectively.

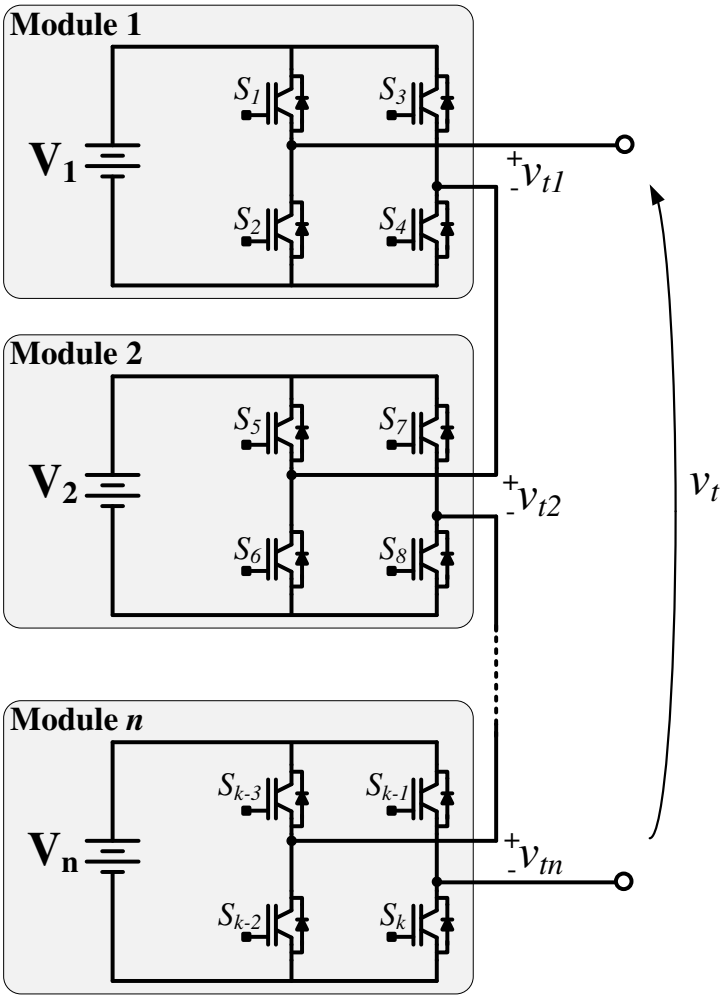


Figure 3:1 – Single-phase *n*-level SCMI.

The number of levels (l) in the terminal voltage (v_t) is given by (3.1).

$$l = 2n + 1 \tag{3.1}$$

Once the DC sources have the same value, they will be called as (3.2).

$$V_{dc} = V_1 = V_2 = ... = V_n \tag{3.2}$$

The SCMI terminal voltage is composed by the sum the terminal voltages of all modules. Figure 3:2 presents diagram of the SCMI at the fundamental frequency. Each module is represented by a sinusoidal voltage source with respective amplitude and phase. The SCMI terminal voltage is sinusoidal with amplitude V_t and angle δ.

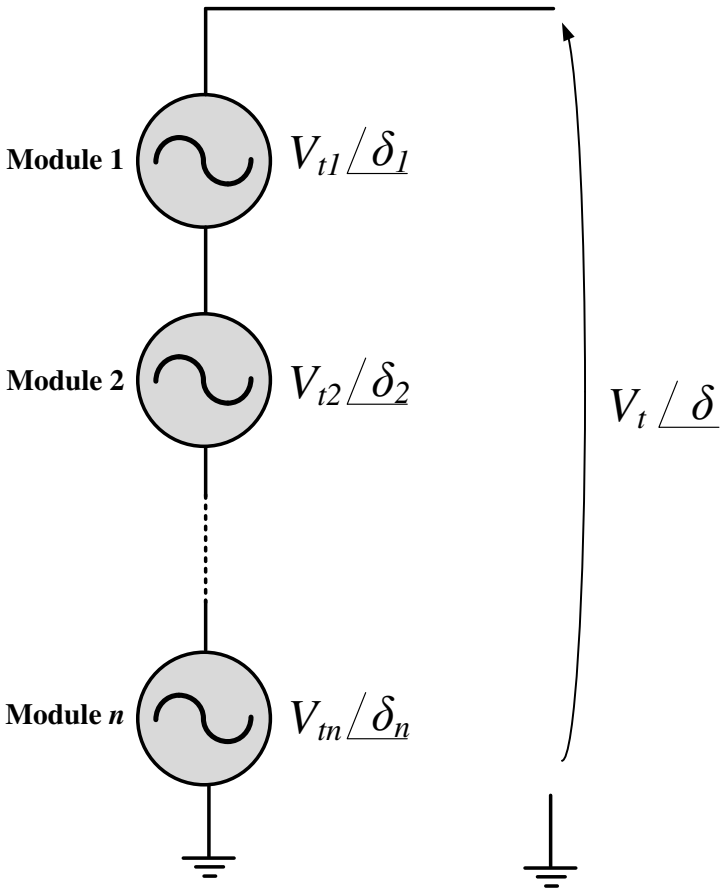


Figure 3:2 – Fundamental frequency diagram of the SCMI.

The angle of fundamental components of each module terminal voltage is equal to the SCMI terminal voltage angle. The reason is the symmetry of the waveforms related to the time-axis, as will be evident later. Therefore, the angles will be written as (3.3).

$$\delta = \delta_1 = \delta_2 = ... = \delta_n \tag{3.3}$$

Therefore, it is enough to modulate a sinusoidal waveform with equal amplitude in each module in order to obtain the SCMI terminal voltage.

3.2 Modulation strategy

In order to compose the terminal voltage with all possible *l* levels, a suited modulation strategy must be applied. There are several modulation strategies for SCMI, being the most common those based on Sinusoidal Pulse Width Modulation (SPWM). They are distinguishable in Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and Phase Shift (PS) [29]–[33]. In APOD, each carrier is phase shifted by 180° from its adjacent carrier. In POD, the carriers above the sinusoidal reference zero point are 180° out of phase with those below zero point while in PD the carriers are in phase. In PS modulation, the carriers are phased-shifted related to each other.

The advantage of using a SPWM technique in SCMI falls in the fact that the terminal voltage presents switching spectra *n*-times higher than the switching frequency spectra for each module. For example, a SCMI composed by three modules, each one with unipolar SPWM switching at 1 kHz, the terminal voltage presents 6 kHz as switching behavior. The factor two is due to the unipolar PWM modulation [34].

$$f_{sw\_vt} = 1kHz \cdot 2 \cdot 3 = 6\ kHz \tag{3.4}$$

The amount of carriers (γ) for each SPWM modulation is proportional to the number of level at the output voltage and it is given by (3.5).

$$\gamma = l - 1 \tag{3.5}$$

3.3 Symmetrical cascaded multilevel inverter with Phase Shift SPWM

This section presents a SCMI, composed by three modules, and using the PS SPWM. Figure 3:3 presents the SCMI with three modules. Therefore, the SCMI terminal voltage will present seven levels.

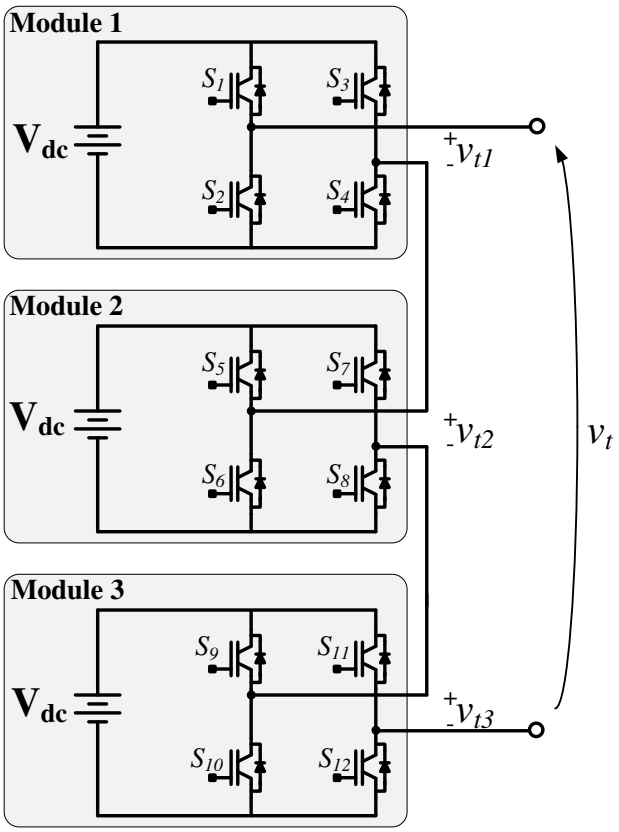


Figure 3:3 – Symmetrical cascaded multilevel inverter with three modules.

According to (3.5), six carriers must be employed. The angle between each other is given by (3.6).

$$\sigma = \frac{360°}{\gamma} \tag{3.6}$$

Figure 3:4 presents a schematic diagram used to obtain each transistor gate signal in a SCMI with three modules and modulated by PD SPWM. The PWM signals are obtained through the comparators. The frequency of each carrier (triangular generators) is 1 kHz. Once the PWM is unipolar, the switching frequency spectrum has components in 2 kHz and their multiples.

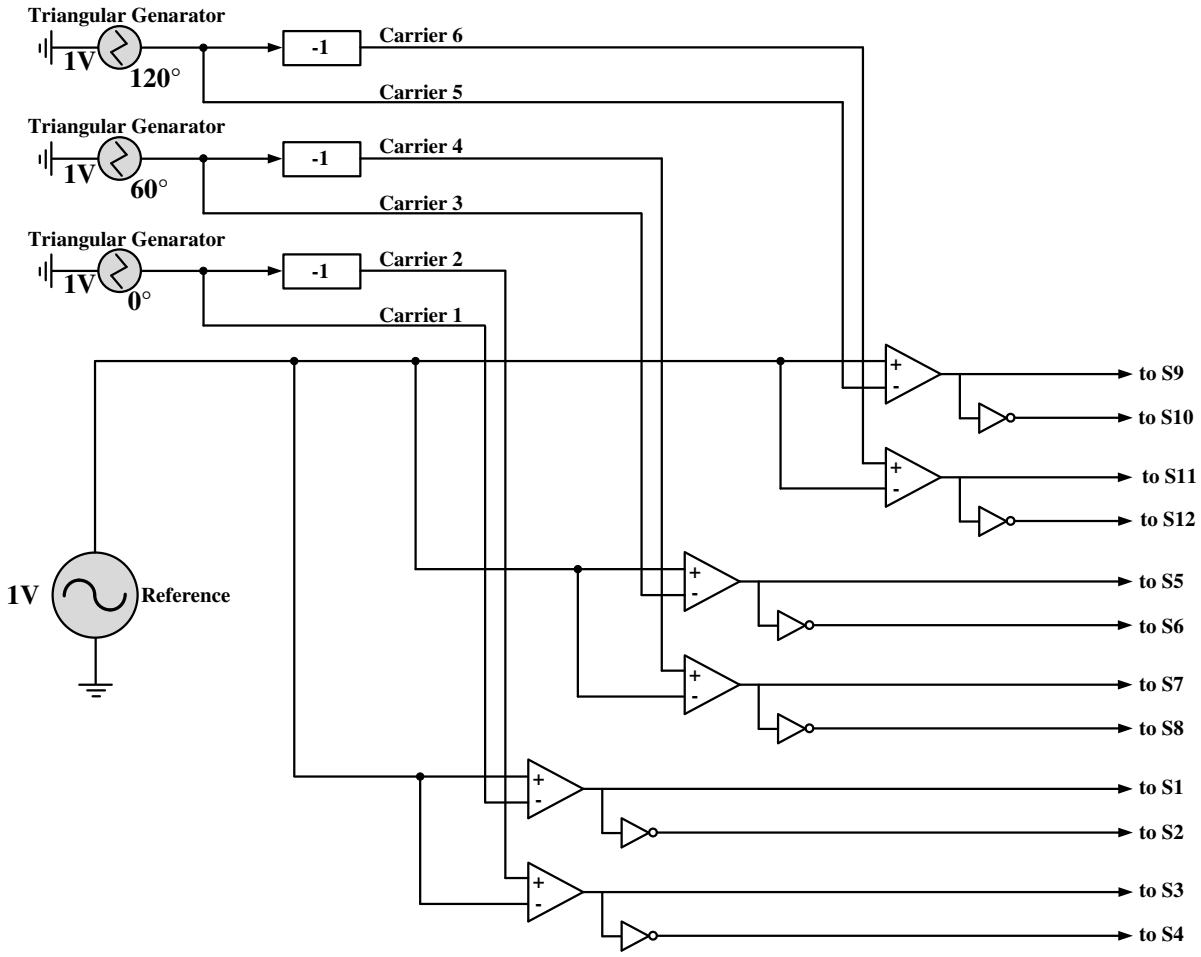
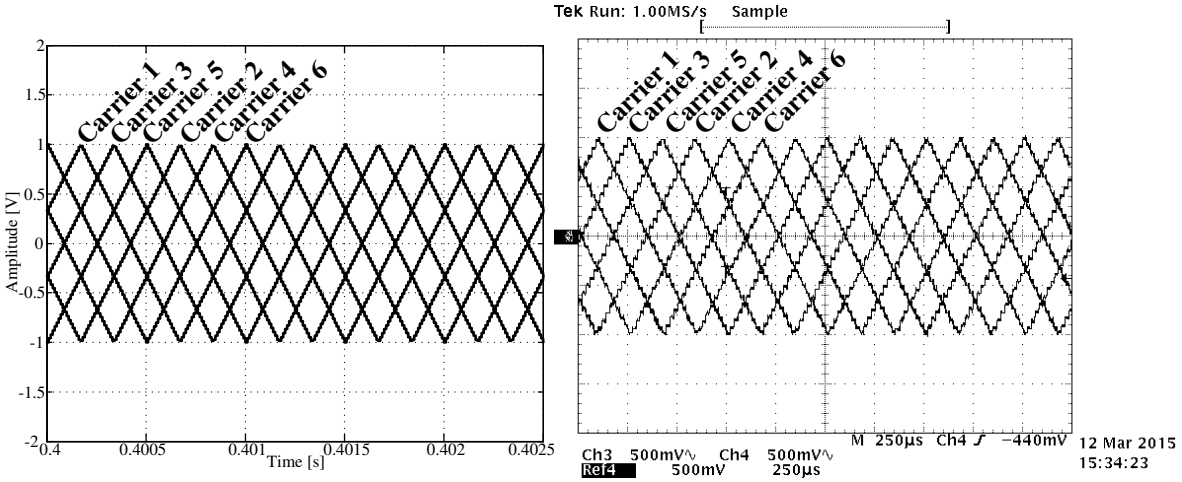


Figure 3:4 - Schematic diagram used to obtain each transistor gate signal in a SCMI with three modules and modulated by PD SPWM.

Figure 3:5 presents the six carriers obtained by the schematic presented in Figure 3:4. The carriers were measured on the oscilloscope by means of the Digital-to-Analog (DAC) 4922 with 12 bits.



(a) (b)

Figure 3:5 - The six carriers obtained by the schematic presented in Figure 3:4. (a) Simulation and (b) Experimental.

According to [34], The terminal voltage for the SCMI is given by (3.7), valid for double-edge carrier modulation.

$$v_t(t) = 3V_{dc}M\cos(\omega_0 t) + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{k=-\infty}^{\infty}\frac{1}{2m}J_{2k-1}(mkM)\cos\left[(m+k-1)\pi\right] \\ p\cos\left[2m\omega_c t + (2k-1)\omega_0 t\right] \quad (3.7)$$

where ω_c is the carrier angular frequency, m and k are the harmonic index variables and $J_k(x)$ is the Bessel function of order k and argument p.

The fundamental terminal voltage for each module of the SCMI is given by (3.8).

$$v_{t1,2,\ldots,n}(t) = V_{dc}M\cos(\omega_o t) \quad (3.8)$$

where M is the modulation index and ω_o is the reference signal angular frequency.

Figure 3:6 presents the module 1 terminal voltage and its spectrum. The modules 2 and 3 have the same voltage waveform and spectrum. The fundamental angle is equal in each module and equal to the SCMI terminal voltage.

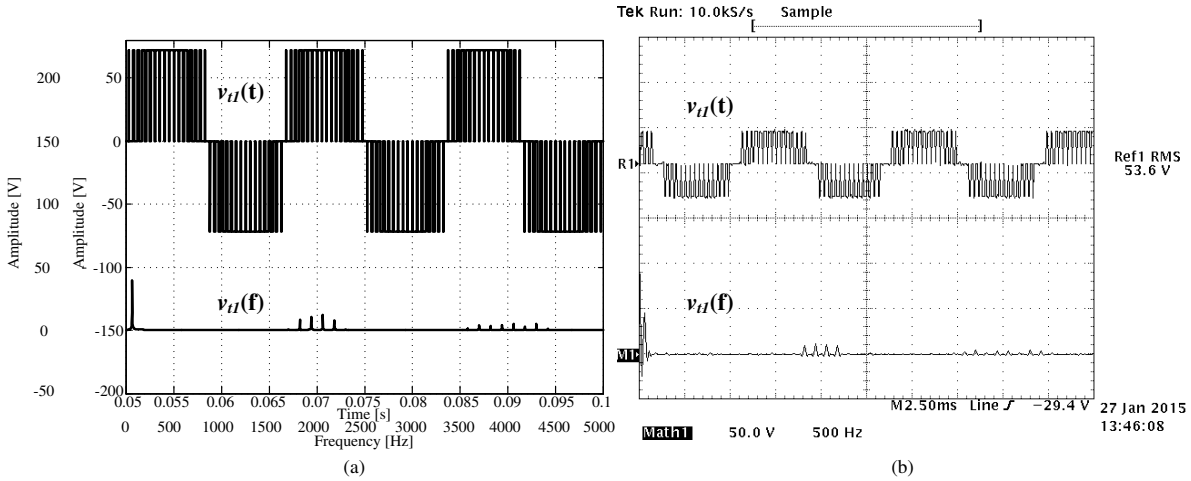


Figure 3:6 - Module 1 terminal voltage and its spectrum. (a) Simulation and (b) Experimental.

Figure 3:7 presents the SCMI terminal voltage and its spectrum. The waveform presents seven levels and the switching spectrum is around 6 kHz and their multiples. Its shape is close to a sinusoidal waveform, which results in reduction in the output filter volume.

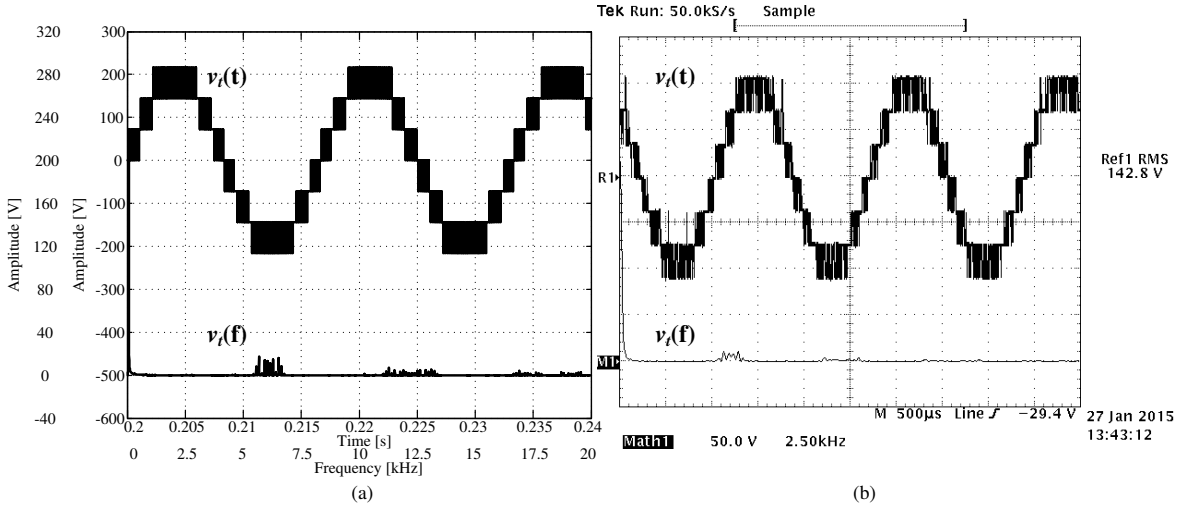


Figure 3:7 - SCMI terminal voltage and its spectrum. (a) Simulation and (b) Experimental.

3.4 Redundant commutations

SCMI presents redundant commutations. A redundant commutation occurs when two or more modules change their output voltage while the SCMI terminal voltage keeps unchanged. They contribute to the switching losses and can be removed without compromising the whole SCMI performance. Some methodologies to remove redundant commutations are presented in the literature [35]–[38]. However, such remotion has impact in the power of each module and its effect should be taken account in project specifications. In this thesis, no one methodology for removing the redundant commutation is applied.

3.5 Power distribution

When a load is connected to the SCMI output, or even when the SCMI is injecting power into the grid, the DC sources supply the power. Once there are several equal series connected modules, it is expected to verify an equal power distribution among the modules.

In order to certify that, a RL load with two values, one-by-one, is connected to the SCMI output. Figure 3:8 presents a RL load connected to the SCMI.

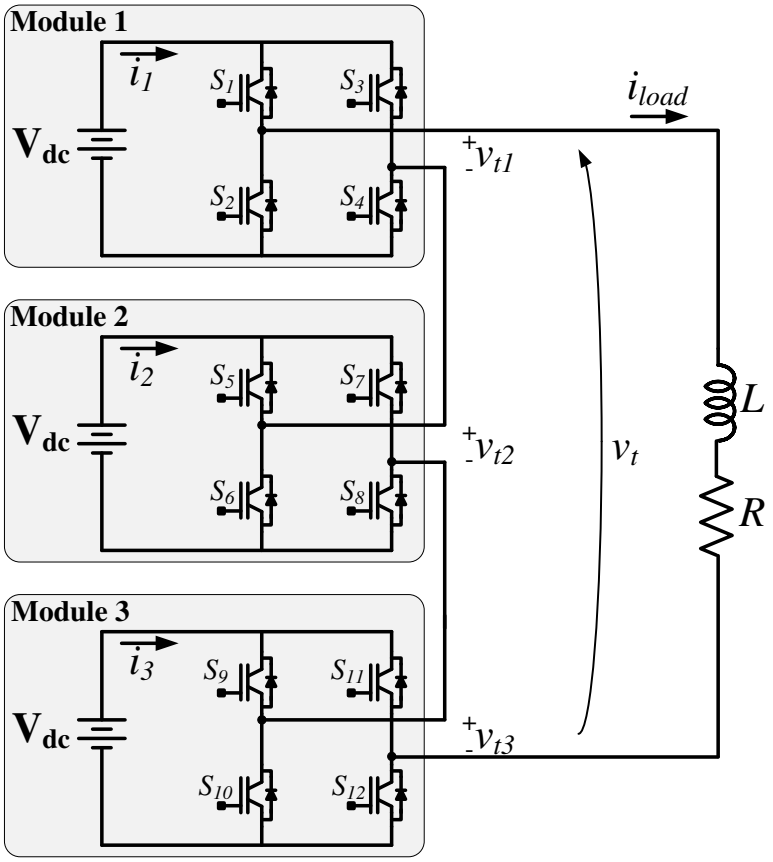
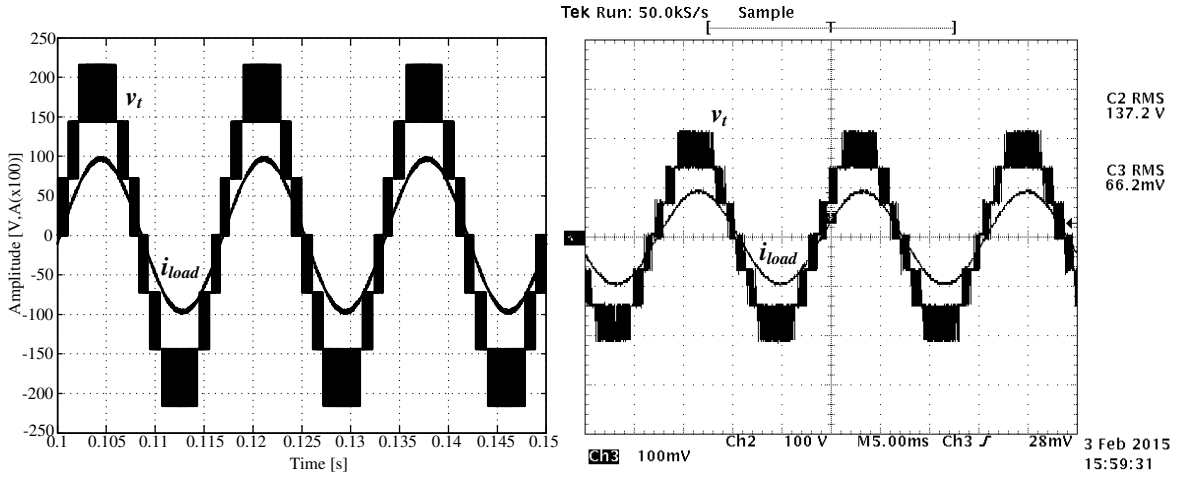


Figure 3:8 - A RL load connected to the SCMI.

Figure 3:9 presents the SCMI terminal voltage and the load current for R = 200 Ω and L = 57 mH. The current is sinusoidal and in out-of-phase related to the voltage due to the inductive behavior of the load.



(a) (b)

Figure 3:9 - SCMI terminal voltage and the load current for R = 200 Ω and L = 57 mH. (a) Simulation and (b) Experimental (Ch3: 0.1V/A).

Assuming that the load current is given by (3.9).

$$i_{load}(t) = I_{load}\sin(\omega t + \theta_{load}) \tag{3.9}$$

where I_{load} is the amplitude and θ_{load} is the angle between the current and the SCMI terminal voltage.

The module 1 terminal voltage at fundamental frequency is given by (3.10).

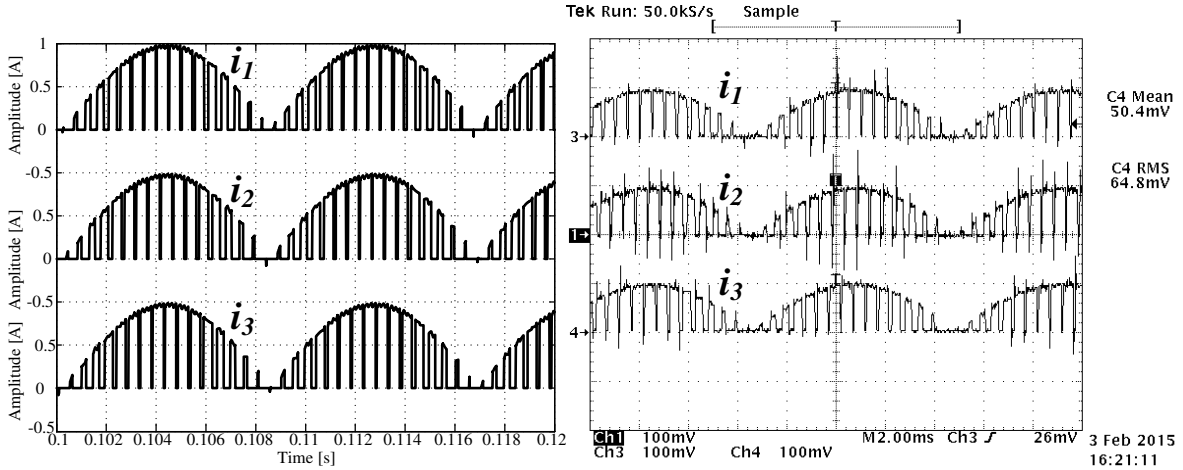
$$v_{t1}(t) = V_{dc}M\cos(\omega_o t) \tag{3.10}$$

The power processed in the module 1 is given by (3.11).

$$p_{m1}(t) = i_{load}(t)v_{t1}(t) = I_{load}\sin(\omega t + \theta_{load})V_{dc}M\cos(\omega_o t) \tag{3.11}$$

Once the load current passes through all modules and their terminal voltages are the same, the power processed by each module is the same.

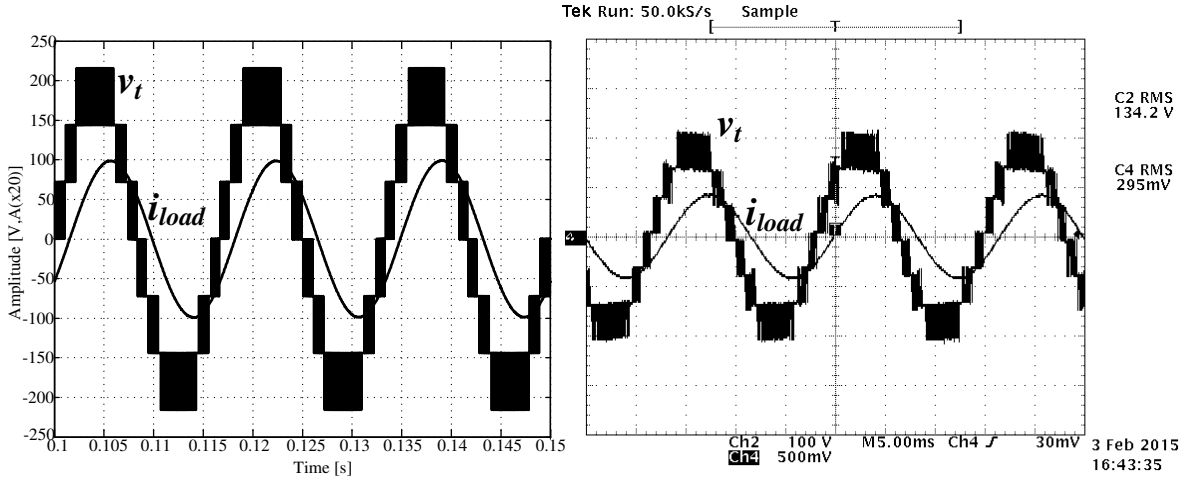
Figure 3:10 presents DC-link current for the three modules. They have the same shape. Each module process one third of the delivered power.



(a) (b)

Figure 3:10 - DC-link currents. (a) Simulation and (b) Experimental (Ch1, Ch3, Ch4: 0.1V/A).

Figure 3:11 presents the SCMI terminal voltage and the load current for R = 33 Ω and L = 57 mH. Similar behavior is observed in the current waveform.



(a) (b)

Figure 3:11 - SCMI terminal voltage and the load current for R = 33 Ω and L = 57 mH. (a) Simulation and (b) Experimental (Ch4: 0.1V/A).

Figure 3:12 presents DC-link current for the three modules. Similarly, each module processes one third of the processed power

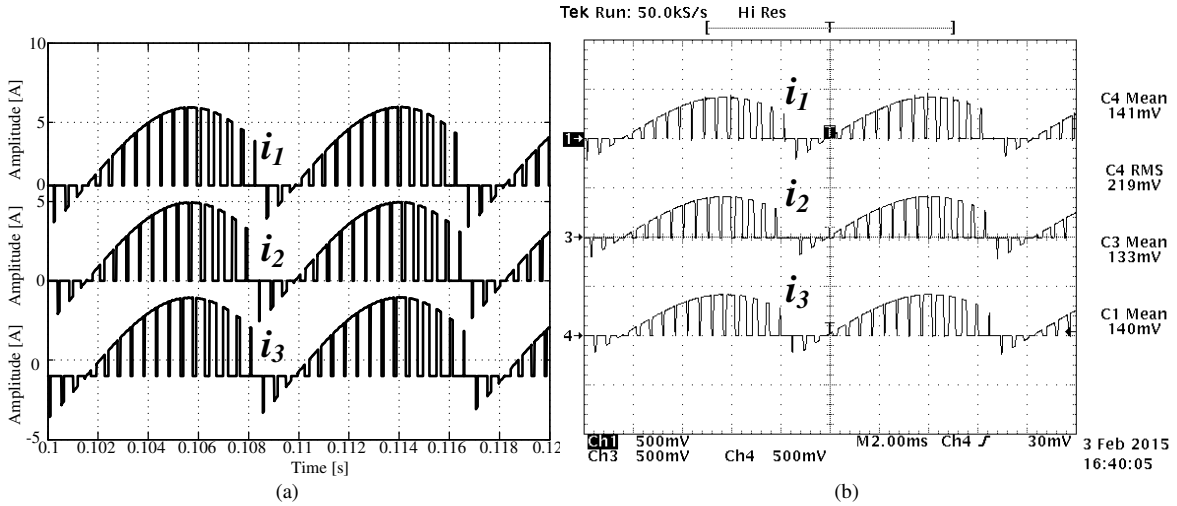


Figure 3:12 - DC-link currents. (a) Simulation and (b) Experimental (Ch1, Ch3, Ch4: 0.1V/A).

Figure 3:13 presents the simulated average power in the three modules. As expected, they have approximately the same value.

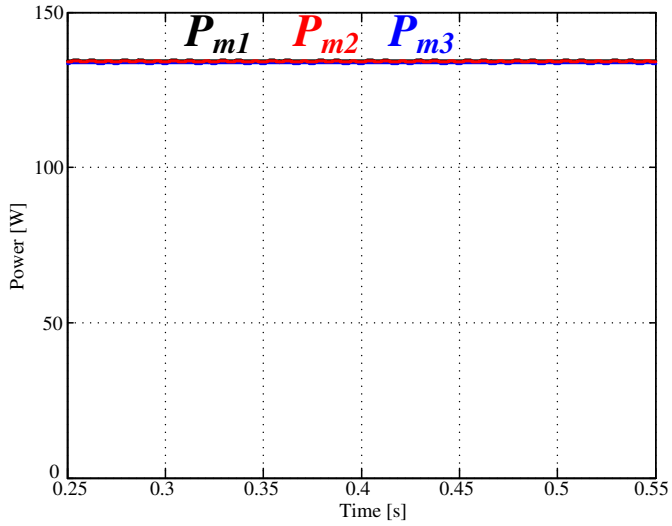


Figure 3:13 - Simulated average power in the three modules.

3.6 Concerning the DC-link currents

As observed in the above DC-link currents, there are moments where the currents reach negative values. These moments happen at the same time for all modules, simplifying the application of a solution to overcome that. Storage applications are prepared for bidirectional power flux. However, such behavior may reduce the life-cycle of the storage element [6].

The current is pulsating and its frequency depends on the switching frequency. A high frequency pulsating current is not desirable for the most kind of storage technologies [39]. In order to overcome this inconvenience, a current controlled DC-DC converter may be

applied between the storage and the inverter. Figure 3:14 presents a SCMI with a current controlled DC-DC converter in each module.

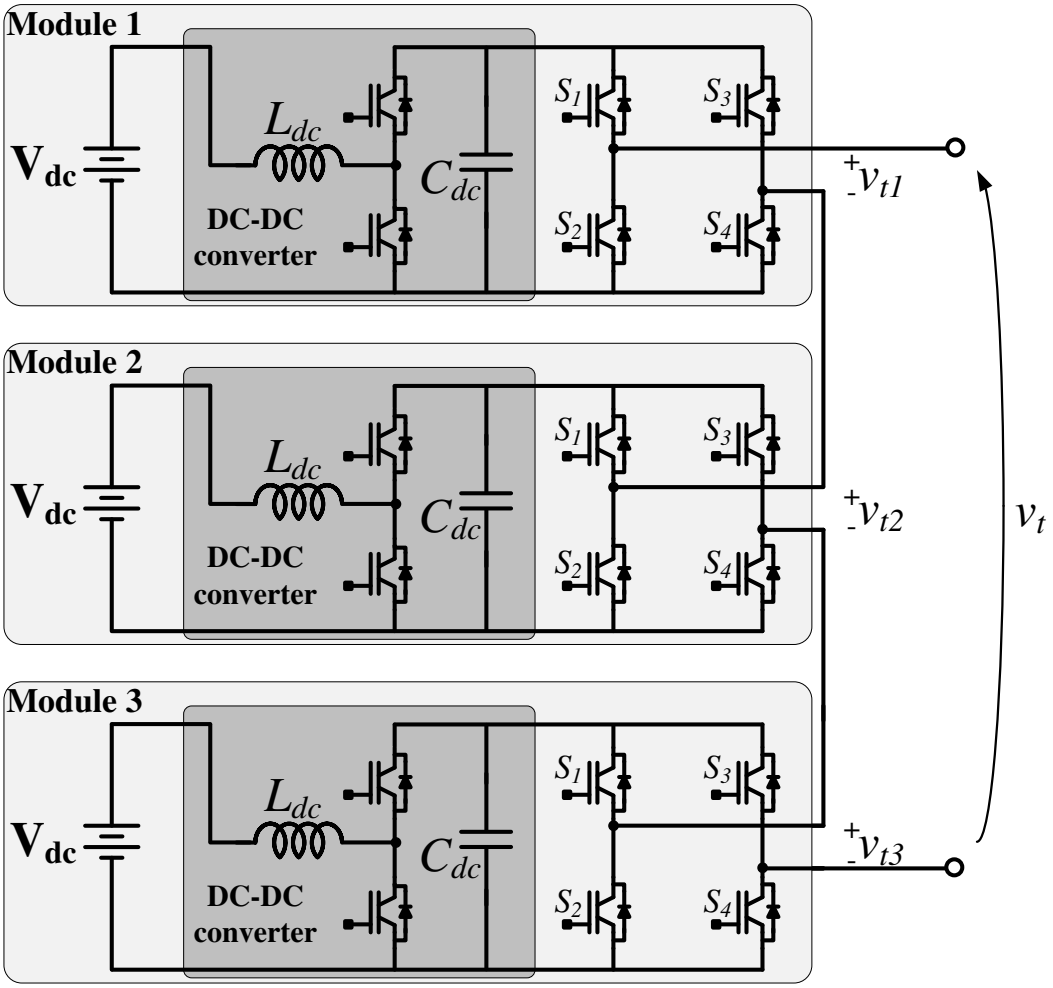


Figure 3:14 - SCMI with a current controlled DC-DC converter in each module.

The DC-DC converter makes the storage current to be continuous, with low ripple, by controlling the inductor current. This solution increases the number of components, the complexity and the power losses. However, it is technically feasible mainly because the possibility of employing transistors in the DC-DC converter similar to that found in the H-bridge inverter. In other words, the DC-DC converter needs to be switched at a relative high frequency, feature found in the H-bridge inverter. The H-bridge inverter and DC-DC converter transistors are equal-sized in voltage, current and frequency.

If the storage element is battery-based, a simpler alternative to make the storage current be continuous is to connect a capacitor in parallel to storage element. The capacitor plus the internal battery resistance work as low-pass filter for the current. Additionally, the capacitor also support on fast response usually required in load steps events. Figure 3:15 presents the SCMI with a capacitor placed in parallel to each voltage source.

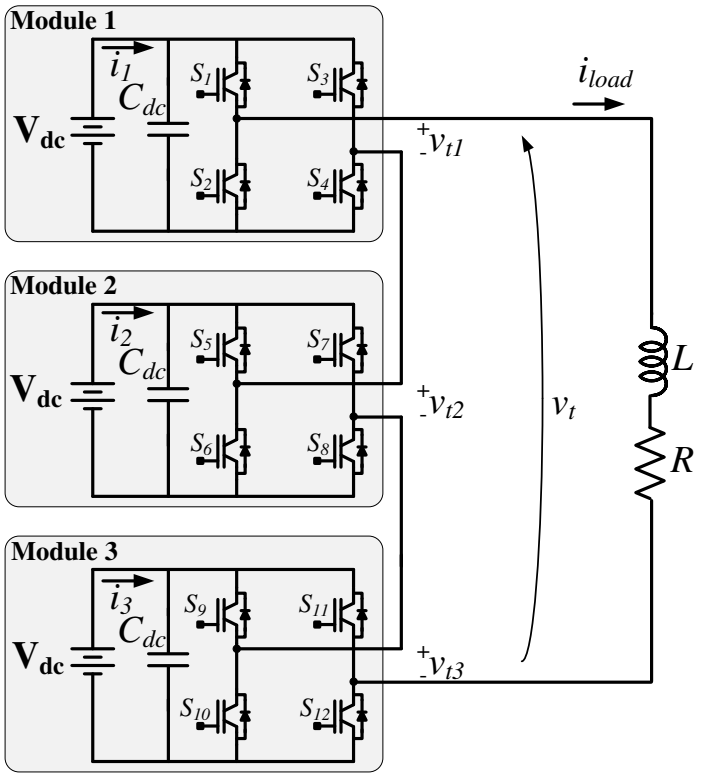


Figure 3:15 - The SCMI with a capacitor placed in parallel to each voltage source.

Figure 3:16 presents the simulated DC-link currents for the three modules when the capacitors are placed. This resulted was simulated with a 150 mΩ series resistance in the voltage source and 2800 μF. The current now is continuous. Throughout this thesis, these capacitors are kept connected.

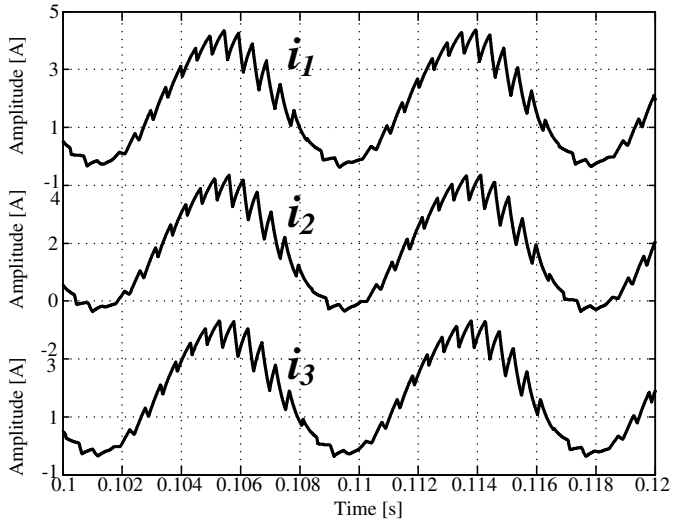


Figure 3:16 – Simulated DC-link currents for the three modules when the capacitors are placed.

3.7 The SCMI connected to an electrical grid.

Figure 3:17 presents the SCMI connected to an electrical grid through a passive filter. The passive filter is still unknown and it will be presented later. The grid is composed by a stiff generator with an output inductance (L_G), it has amplitude V_p and angular frequency ω rad/s. The Point of Common Coupling (PCC) is the delimitations between the grid and the SCMI.

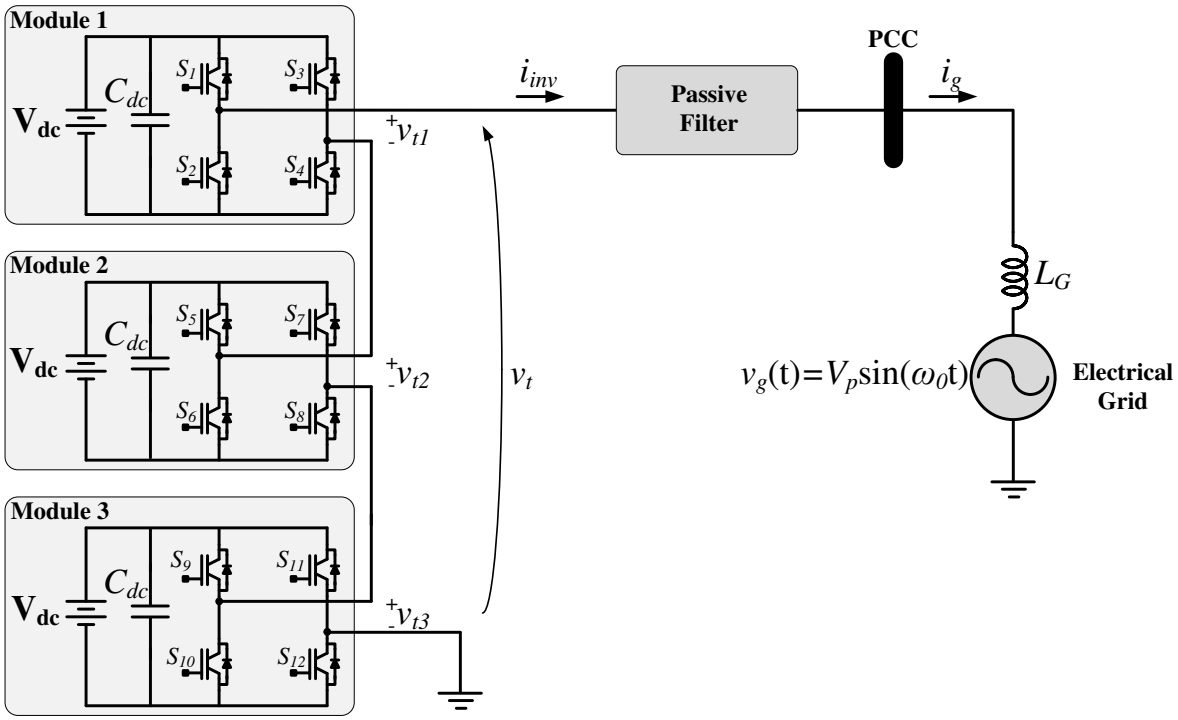


Figure 3:17 - The SCMI connected to an electrical grid through a passive filter.

3.8 SCMI output filter

The feature of multilevel inverters to have their terminal voltage close to sinusoidal waveform allows the applications of an output filter with reduced order. Therefore, LC and LCL filters are not attractive in grid-tied applications for these inverters.

A simplified method for designing the output inductor is to compute the inductance by taking a small percentage of the base impedance [40]. This method is applied in this thesis and its procedure is presented as follow. The SCMI output inductor is called throughout this chapter as L_{SCMI}.

The base impedance is given by (3.12).

$$Z_b = \frac{\left(\frac{V_p}{\sqrt{2}}\right)^2}{P_{SCMI}} \tag{3.12}$$

where P_{SCMI} is the SCMI nominal power.

The output filter reactance is given by (3.13).

$$X_{LSCMI} = L_{SCMI}\omega_0 = Z_b \frac{x_{(\%)}}{100} \tag{3.13}$$

where $x_{\%}$ is the chosen percentage of the base impedance. The choice must be lower than 10% in order to limit AC voltage drop across the reactance [41][40].

Replacing (3.12) in (3.13), the SCMI output inductor is given by (3.14)

$$L_{SCMI} = \frac{V_P{}^2 x_{(\%)}}{2P_{SCMI}\omega_0} \frac{1}{100} \tag{3.14}$$

3.9 Closed-loop current control

Since the SCMI is connected to the grid, it is desirable to control its output current in order to guarantee an acceptable level of energy quality. Moreover, controlling the output current makes easier the implementation of protection schemes.

Figure 3:18 presents the SCMI connected to the grid with closed-loop current control. The influence of the grid inductance is considered in the control design. The SCMI output current is sensed by means of a current sensor and the measured signal is sent to the control strategy block. The PCC voltage is measured in order to be used in a feedforward action. A signal conditioning circuit (not shown) is used to fit the current and voltage values within the microcontroller range. The conditioned signal cannot suffer changes neither in amplitude nor in phase.

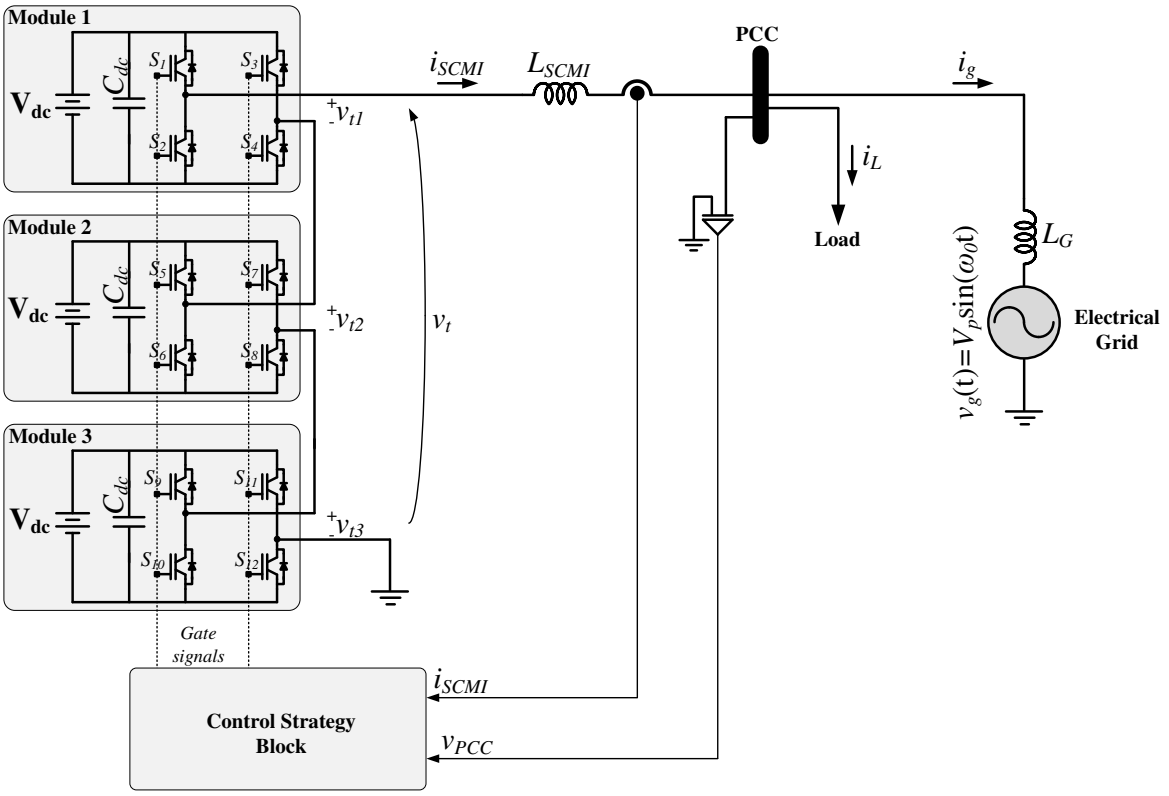


Figure 3:18 – The SCMI connected to the grid with closed-loop current control.

According to the control theory, a PI controller is unable, in stationary frame, to make the controlled variable to follow a sinusoidal reference without amplitude and phase errors [42]. An exception arises when the system plant has relative low bandwidth [43]. In this chapter, a PI with feedforward action is applied to control the SCMI output current in stationary frame.

Figure 3:19 presents the control strategy block diagram. The measured current (i_{SCMI}) is subtracted from the current reference (i_{SCMI}*) and the resulted error signal (e) is sent to the controller, which, in turn, acts in the SCMI through the modulated signal (u). A voltage feedforward (v_{PCC}) is added to the current controller output signal. The SCMI plus the output filter is represented by a current plant ($I_{SCMI}(s)$). The current sensor gain is assumed to be unitary and its compensation is made right after the measured signal have passed through the micronctroller AD converter. The PWM has unitary triangular and will be omitted.

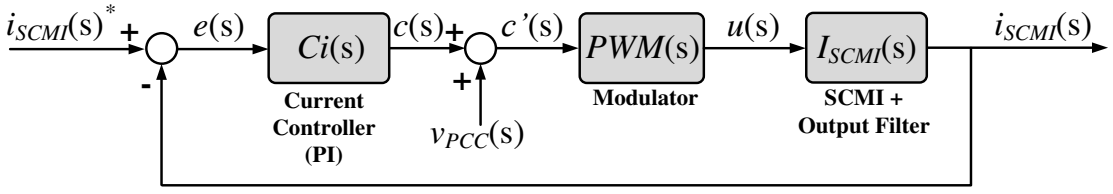


Figure 3:19 - The control strategy block diagram.

The PI is tuned aiming null steady-state error. Therefore, the control objective can be expressed in mathematical form as presented in (3.15).

$$i_{SCMI}(t) \rightarrow i_{SCMI}{}^{*}(t) \quad \text{as} \quad t \rightarrow \infty \tag{3.15}$$

In order to guarantee (3.15), the system must be mathematically modeled. The model can be obtained by simple application of Kirchhoff's laws. This yields the following model that describes the system dynamics.

$$L_G \frac{di_g(t)}{dt} = v_{PCC}(t) - v_g(t) \tag{3.16}$$

$$L_{SCMI} \frac{di_{SCMI}(t)}{dt} = v_{t1}(t) + v_{t2}(t) + v_{t3}(t) - v_{PCC}(t) \tag{3.17}$$

$$i_{SCMI}(t) = i_g(t) + i_L(t) \tag{3.18}$$

where i_L is a current from a possible load connected to the PCC.

The module terminal voltages can be written as (3.19).

$$\begin{bmatrix} v_{t1}(t) \\ v_{t2}(t) \\ v_{t3}(t) \end{bmatrix} = \begin{bmatrix} u_1(t)V_{dc} \\ u_2(t)V_{dc} \\ u_3(t)V_{dc} \end{bmatrix} \tag{3.19}$$

where $u_{1,2,3}$ denote the modulation signals for each H-bridge. Their signals are continuous and their values are in the range [-1 1].

In order to facilitate the controller design and to reduce the model expressions, it is convenient to transform (3.19) by the definition given in (3.20) [44].

$$\lambda(t) = u_1(t) = u_2(t) = u_3(t) \tag{3.20}$$

Therefore, (3.17) can be rewritten as (3.21).

$$L_{SCMI} \frac{di_{SCMI}(t)}{dt} = 3V_{dc}\lambda(t) - v_{PCC}(t) \tag{3.21}$$

Isolating $v_{PCC}(t)$ in (3.21) and replacing it in (3.16), it reaches (3.22).

$$L_G \frac{di_g(t)}{dt} = 3V_{dc}\lambda(t) - L_{SCMI} \frac{di_{SCMI}(t)}{dt} - v_g(t) \tag{3.22}$$

Similarly, isolating $i_g(t)$ in (3.18) and replacing it in (3.22), it reaches (3.23).

$$L_G \frac{d\left[i_{SCMI}(t) - i_L(t)\right]}{dt} = 3V_{dc}\lambda(t) - L_{SCMI} \frac{di_{SCMI}(t)}{dt} - v_g(t) \tag{3.23}$$

Rearranging (3.23), it results (3.24).

$$\left(L_G + L_{SCMI}\right) \frac{di_{SCMI}(t)}{dt} = 3V_{dc}\lambda(t) - v_g(t) + L_G \frac{di_L(t)}{dt} \tag{3.24}$$

The last terms can be considered as disturbances and may be neglected while the $v_g(t)$ term will be compensated by the feedforward action. These statements are shown in (3.25). Appendix D presents how the effect of a disturbance can be minimized

$$\left(L_G + L_{SCMI}\right)\frac{di_{SCMI}(t)}{dt} = 3V_{dc}\lambda(t) - \underbrace{v_g(t)}_{\text{Compensated by feedforward}} + \underbrace{L_G\frac{di_L(t)}{dt}}_{\text{Disturbance}} \tag{3.25}$$

By applying the perturbation and linearization technique [11] and taking the Laplace transformation, the SCMI plus output filter transfer function is given by (3.26).

$$\frac{I_{SCMI}(\mathrm{s})}{\lambda(s)} = \frac{3V_{dc}}{s\left(L_G + L_{SCMI}\right)} \tag{3.26}$$

The PÌ controller transfer function is given by (3.27).

$$Ci(s) = \frac{\lambda(s)}{e(s)} = \frac{k_p\left(sT_{PI}+1\right)}{sT_{PI}} \tag{3.27}$$

The closed-loop transfer function that relates the SCMI output filter and its reference is given by (3.28).

$$\frac{I_{SCMI}(s)}{I_{SCMI}{}^*(s)} = \frac{3V_{dc}k_p\left(sT_{PI}+1\right)}{s^2T_{PI}\left(L_G + L_{SCMI}\right) + s3V_{dc}k_pT_{PI} + 3V_{dc}k_p} \tag{3.28}$$

Neglecting the one-sampling delay [45], the damping factor is given by (3.29).

$$\xi = \frac{1}{2}\sqrt{\frac{3V_{dc}k_pT_{PI}}{L_G + L_{SCMI}}} \tag{3.29}$$

ξ =1 leads to a critically damping response and it is a good choice. Moreover, the time constant T_{PI} must be assigned to be much longer than the control delay from the view point of control stability [42]. By setting a value to the T_{PI}, the k_p is found.

3.10 Discretizing the controller

The procedure for tuning the PI controller was presented in *s*-domain. Once the control strategy implementation in this thesis is digital, it is necessary to discretize the PI controller. Discretizing a *s*-domain controller without discretizing the whole system is valid because the fictitious *w*-plane, mapped from the *z*-plane, is close to *s*-plane except for frequencies higher than hundreds of kilohertz [46].

In order to discretize the PI controller, the Backward-Difference approximation is applied, given by (3.30).

$$s = \frac{1 - z^{-1}}{T_s} \tag{3.30}$$

where T_s is the sampling period.

Therefore, the PI controller transfer function in z-domain is given by (3.31).

$$C_{PI}(z) = k_p \frac{\left(1 + \frac{T_s}{T_{PI}} - z^{-1}\right)}{1 - z^{-1}} \tag{3.31}$$

3.11 Verifying the current controller

In order to verify the efficacy of the designed current controller, the SCMI was set to be operated as active filter. Figure 3:20 presents the system used to verify the efficacy of the current controller. A nonlinear load made by a diode rectifier with LC filter at the DC-side was used as a source of harmonic currents.

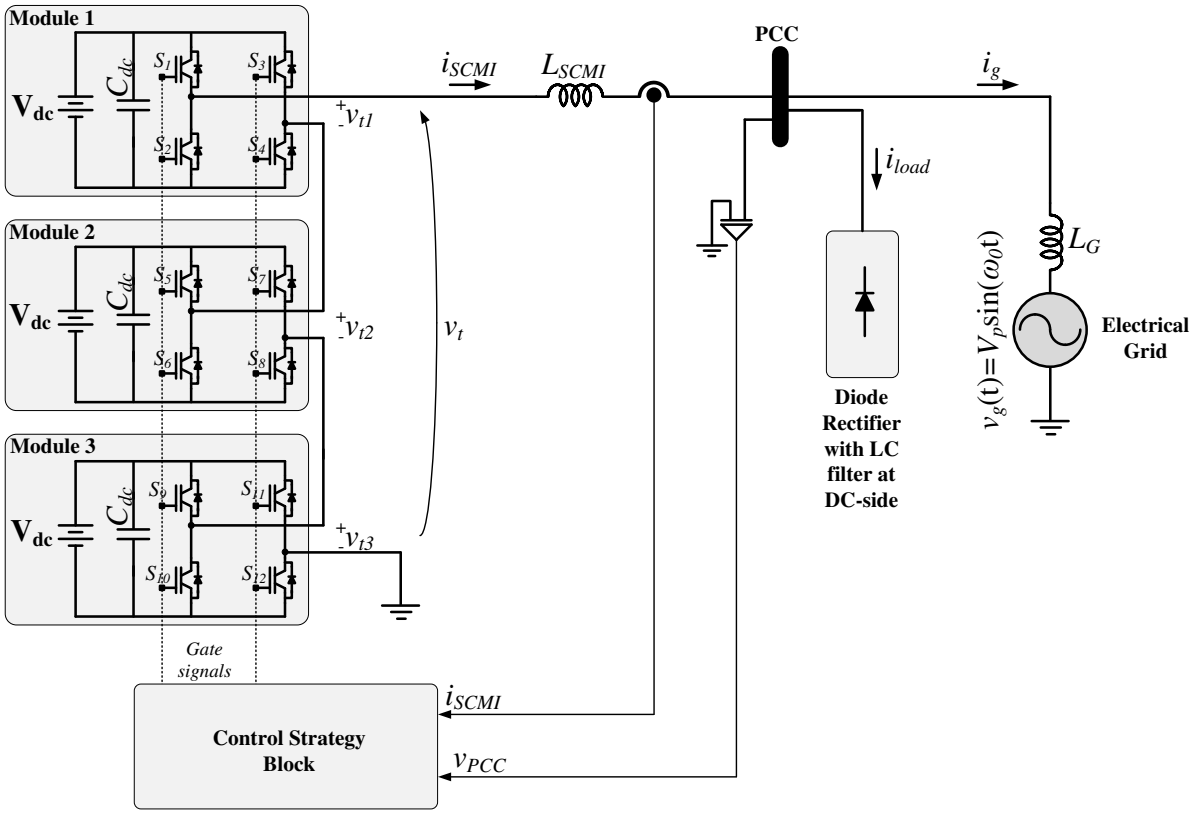


Figure 3:20 - System diagram used to verify the efficacy of the current controller.

The parameters used in the simulation and in the prototype are presented in Table 3:1.

Table 3:1 - Parameters used in the simulation and in the prototype.

Parameter	**Value**
Grid peak voltage	V_p = 180 V
Grid frequency	f_g = 60 Hz
Grid inductance	L_G = 0.3 mH

Inductance of the rectifier DC-side filter	L_{rect} = 35 mH
Capacitance of the rectifier DC-side filter	C_{rect} = 470 µF
Rectifier load	R_{rect} = 95 Ω
SCMI nominal power	P_{SCMI} = 500 W
Percentage of the base impedance	x% = 5%
SCMI output inductance (according to (3.14)	L_{SCMI} = 4.25 mH
DC voltage source	V_{dc} = 72 V
DC-link capacitor	C_{dc} = 2800 µF
Sampling frequency	F_s = 30 kHz
Switching frequency	F_{sw} = 2 kHz
Damping factor	ξ = 1
PI time constant (adopted)	T_{PI} = 20 ms
PI proportional gain (according to (3.29)	k_p = 0.004212962

Figure 3:21 presents the PCC voltage, the grid current, the SCMI output current and its current reference signal. The SCMI output current follows its reference signal with negligible steady-state error. Consequently, the grid current is sinusoidal and in-phase with the PCC voltage. The manner how the current reference signal was obtained is not relevant at this point. Later, the Conservative Power Theory (CPT) will be introduced and the reference signal is explained.

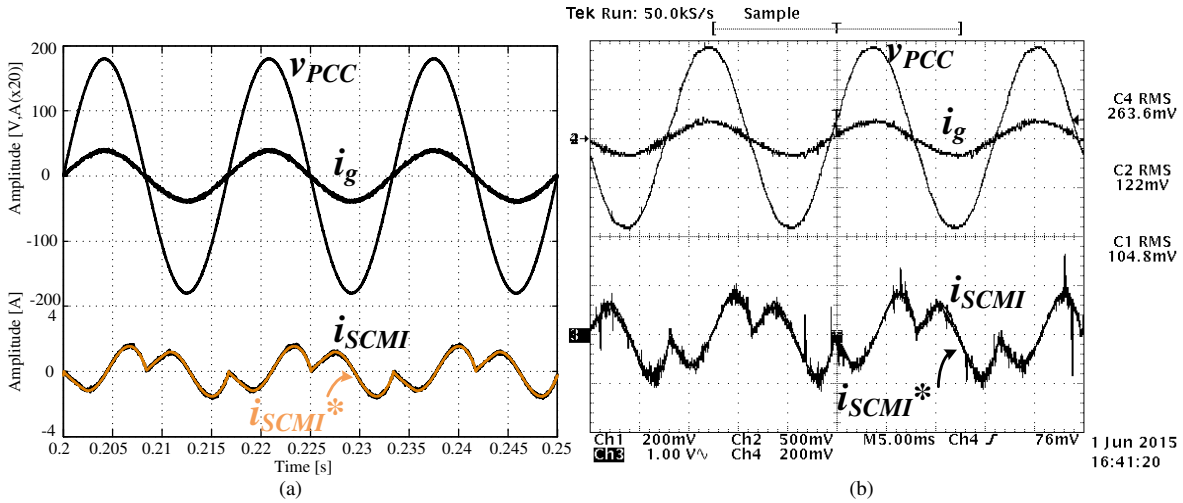


Figure 3:21 - PCC voltage (v_{PCC}), the grid current (i_g), the SCMI output current (i_{SCMI}) and its current reference signal (i_{SCMI}*). (a) Simulation and (b) Experimental (Ch1, Ch2: 0.1V/A; Ch4: 0.5V/V).

Figure 3:22 presents the simulated signal error between the SCMI output current and its reference signal.

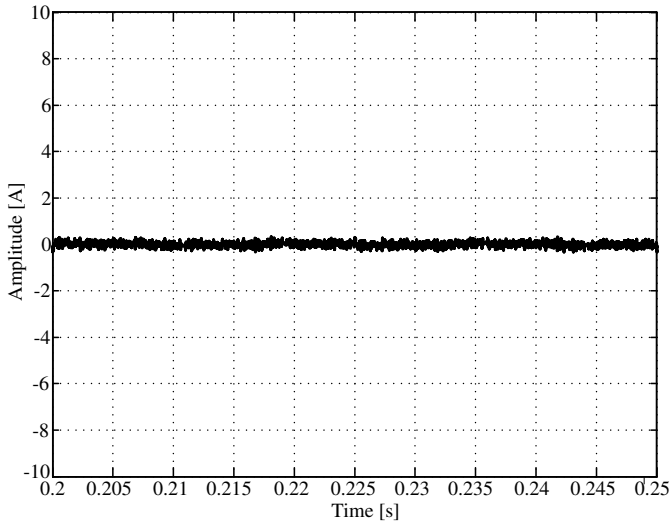
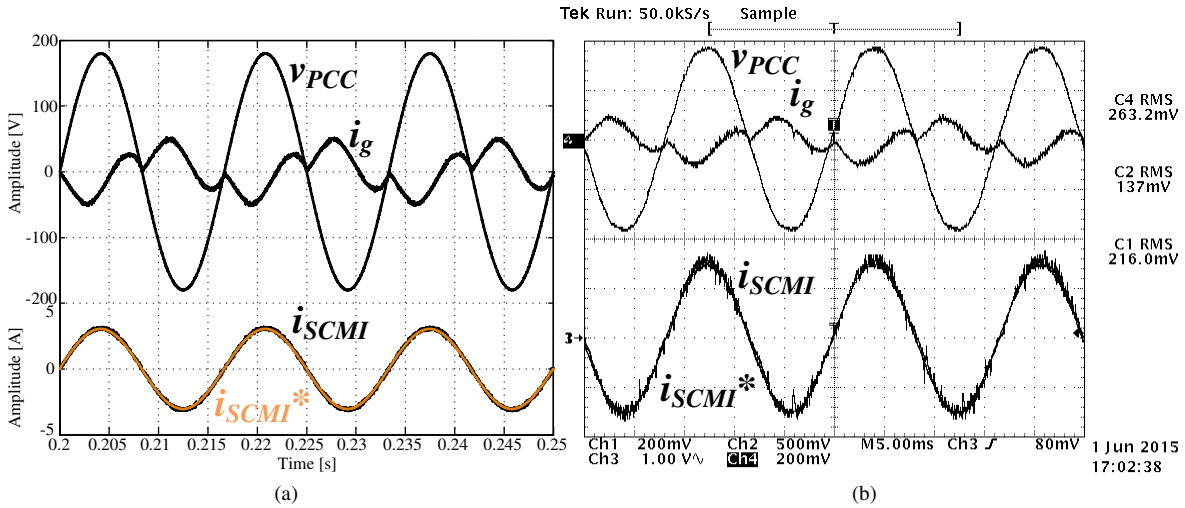


Figure 3:22 - Simulated signal error between the SCMI output current and its reference signal.

Figure 3:23 presents the SCMI output current following a sinusoidal reference. The SCMI current is in-phase to the PCC voltage. Therefore, the designed PI controller and the obtained SCMI model are effective and truthful.



(a) (b)

Figure 3:23 - SCMI output current following a sinusoidal reference. (a) Simulation and (b) Experimental (Ch1, Ch2: 0.1V/A; Ch4: 0.5V/V).

3.12 Closed-loop DC-link voltage control

Although the SCMI study presented is this thesis is mainly directed to storage applications, it is convenient to describe how the SCMI DC-link voltages are controlled. The description applies when capacitors are used instead of DC sources. Some applications which may be done by using only capacitors at the SCMI DC-link are those that do not handle active power, except the losses, such as active filters and STATCOMs. A variety of SCMI DC-link

voltage control strategy is reported in the literature [44], [47]–[50]. In this thesis, a classical strategy is presented and its validation is made though simulation. Figure 3:24 presents the SCMI where the DC sources were replaced by capacitors. Each DC-link is measured and the signals are sent to the control strategy block.

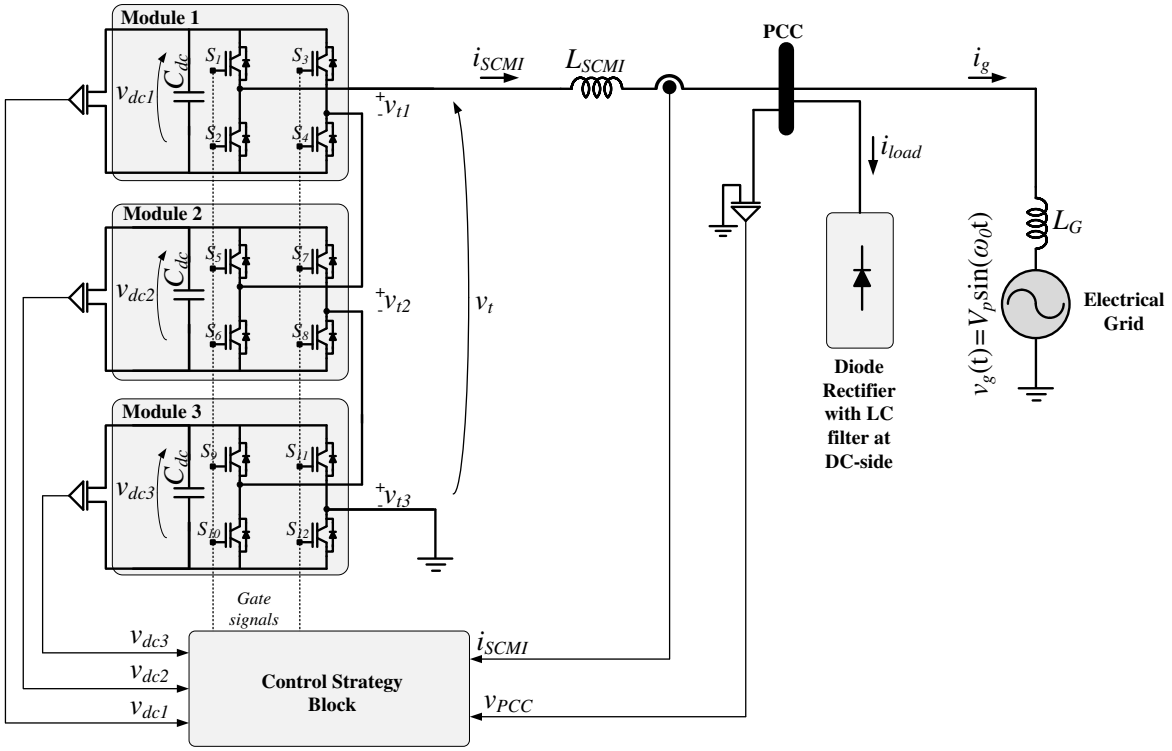


Figure 3:24 - The SCMI where the DC sources were replaced by capacitors.

The DC-link voltage must be controlled in order to guarantee the total operation of the SCMI and also to overcome the power losses. The DC-links absorbs active power from the module terminal point. The active power across each module terminal point is given by (3.32).

$$p_{act(1,2,3)} = \frac{1}{T}\int_{t_0}^{t_0+T}\sum_{h=1}^{\infty} v_{t(1,2,3)h}(t)\, i_{SCMIh}(t)\, dt \tag{3.32}$$

where h is the harmonic order.

Analyzing the integral in (3.32), the module terminal voltage is multiplied by the SCMI current in each harmonic. The voltage is shaped through the PWM and its harmonic content has the switching components plus the frequencies found in the synthetized current. In active filter, the SCMI current is the harmonic content from a nonlinear load. Figure 3:25 presents the harmonic content for the module 1 terminal voltage and for the SCMI output current. The SCMI was set to operate as active filter. The fundamental component of the SCMI output current is due to the reactive power compensation.

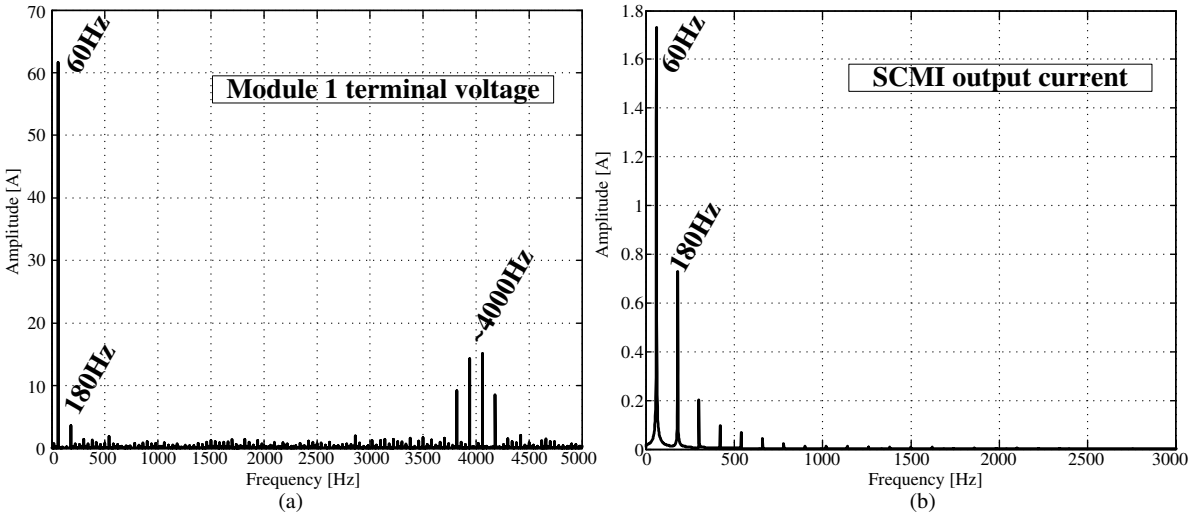


Figure 3:25 - Harmonic content for the module 1 terminal voltage and for the SCMI output current.

By applying the presented voltage and current into (3.32), the non-null products are at the low frequencies. The product at the fundamental is much higher than those found in 180Hz, 300Hz, etc. The active power in theses frequencies can be neglected. Therefore, it is expected that the strategy used to control the DC-link voltage in a classical H-Bridge inverter may be applied to the SCMI [51]–[54], taking into account the existence of three modules.

Figure 3:26 presents the block diagram of the DC-link voltage control strategy. The current control loop presented in section 3.9 is an inner loop of the DC-link voltage control. Therefore, the voltage controller must be slower than the current controller [43].

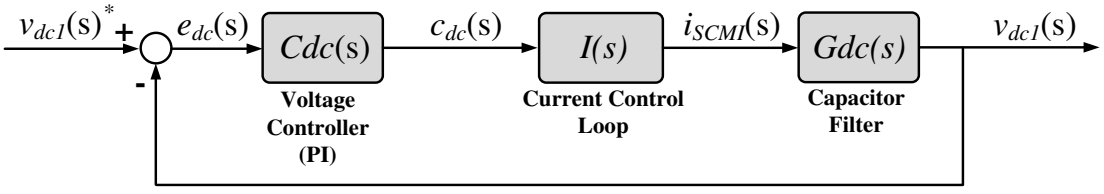


Figure 3:26 - Block diagram of the DC-link voltage control strategy.

Figure 3:27 presents the diagram showing how the DC-link controller should be employed. Each module is compared to the voltage reference. The resulted signal is summed up and it is divided by the number of modules. Then, the signal passes through a PI controller, which in turn, is subtracted from the SCMI current reference signal. The PCC voltage is used to synchronize to the fundamental frequency of the voltage.

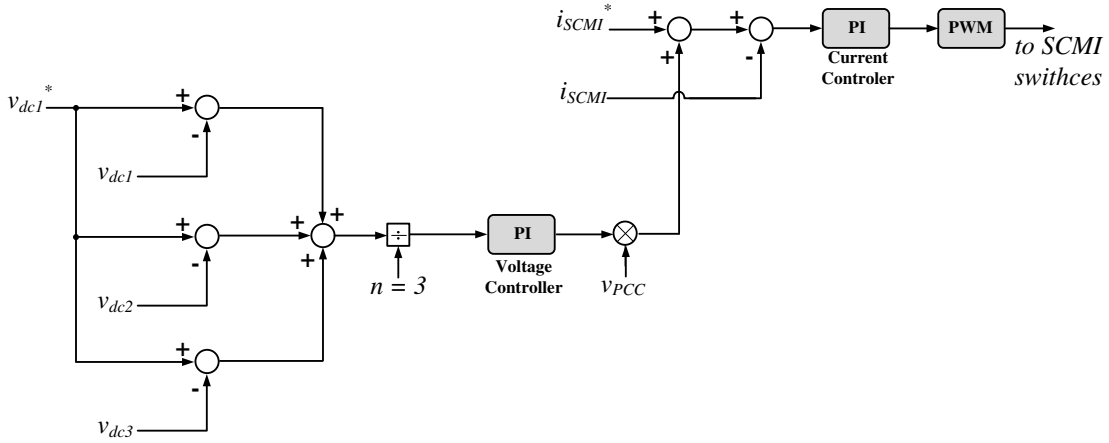


Figure 3:27 - Diagram indicating how the DC-link controller must be employed.

The procedure to tune the PI controller in the DC-link control is similar to that for classical H-Bridge inverter [55], [56] and it is omitted here. A detailed analysis for SCMI is presented in [57]. An unbalance control mesh should be included in order to compensate the parameter variation. Otherwise, the DC-link voltages may diverge.

3.13 Verifying the DC-link voltage controllers

The system showed in Figure 3:24 was simulated. The parameters presented in Table 3:1 are applied in this section. Moreover, Table 3:2 presents the parameters used in the DC-link voltage control. The discretizing of the PI controller was done by means of the Backward transformation.

Table 3:2 - Parameters used in the DC-link voltage control.

Parameter	**Value**
PI proportional gain	k_{dc} = 0.001154
PI time constant	T_{dc} = 120 ms
DC-link voltage reference	V_{dc}* = 72 V

Figure 3:28 presents the simulated DC-link voltage for each module. A pre-charge exists in order to avoid overcurrent during initial transition. The initial overvoltage is mainly caused by the SCMI output inductor. The three module DC-link voltages are controlled at the reference value. At = 2s, a load step occurred. The voltages reach the steady-state condition after approximately 100ms.

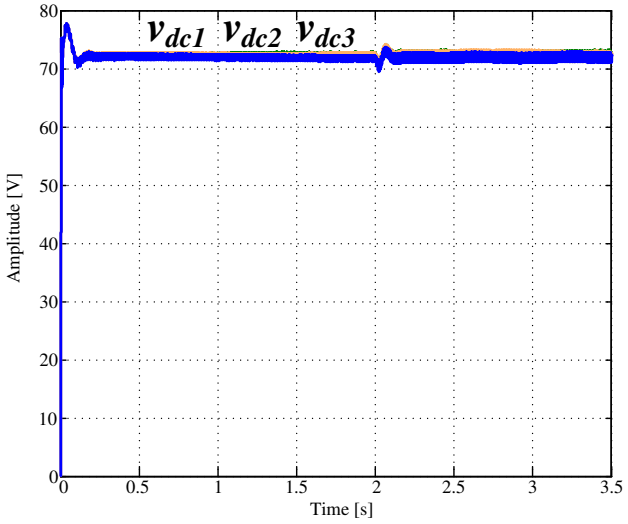


Figure 3:28 – Simulated DC-link voltage for each module.

Figure 3:29 presents the simulated PCC voltage, the grid current, the load current, the SCMI output current and its signal reference for the same load step. The SCMI output current still follows its reference, indicating that the voltage and current controller can be considered independent.

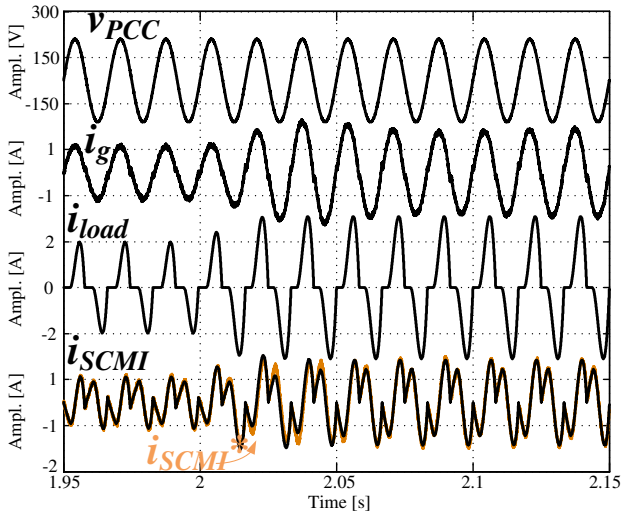


Figure 3:29 – Simulated PCC voltage, the grid current, the load current, the SCMI output current and its signal reference for the same load step.

3.14 SCMI prototype

Figure 3:30 presents the prototype of the SCMI used in this chapter.

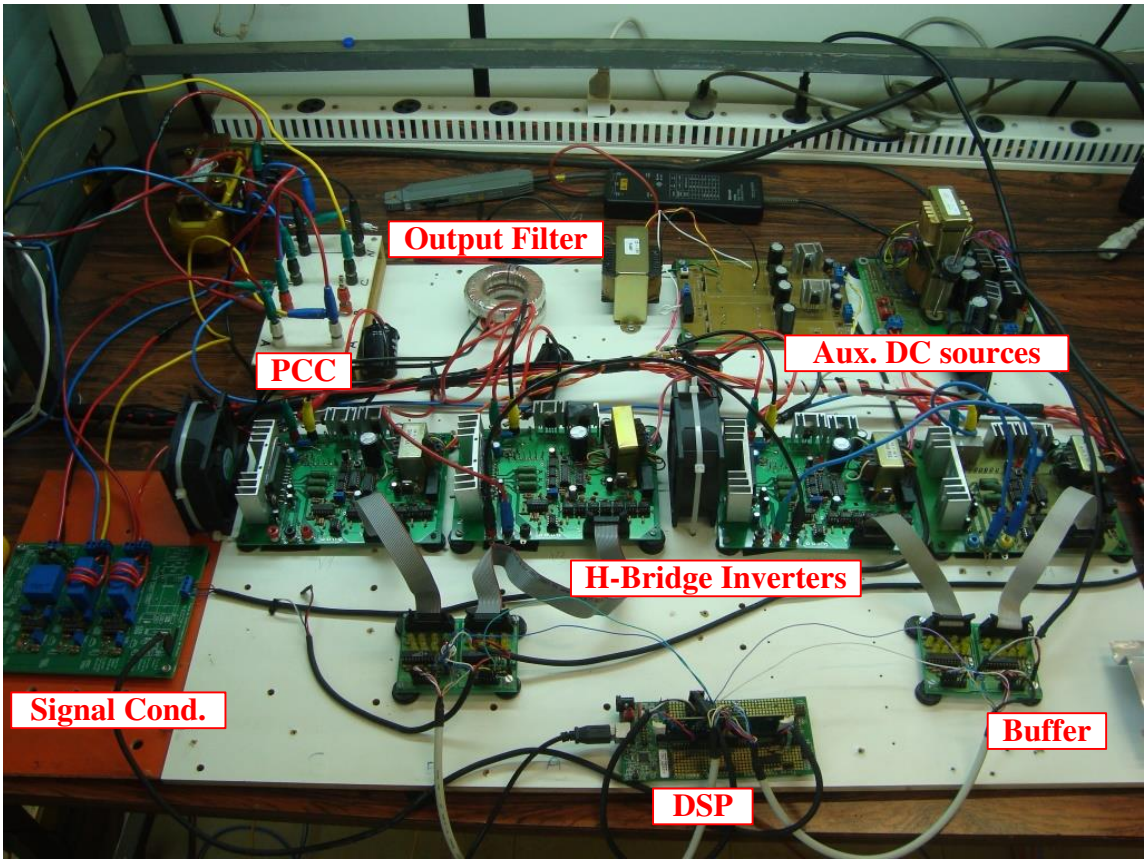


Figure 3:30 - Prototype of the SCMI used in this chapter.

3.15 Three-phase SCMI

This section presents the three-phase SCMI and its features. The studies previously described are extended to three-phase.

The use of a three-phase SCMI is recommended for high-power application. A drawback is on the number of isolated DC sources, which is relatively high. The amount of levels is increased when the line-to-line voltage is taken. An increase in the number of levels reduces the voltage distortion.

Figure 3:31 presents the three-phase SCMI with three modules each one. Each phase is composed by three-modules with equal DC sources. The voltages v_a, v_b and v_c are referred to the ground.

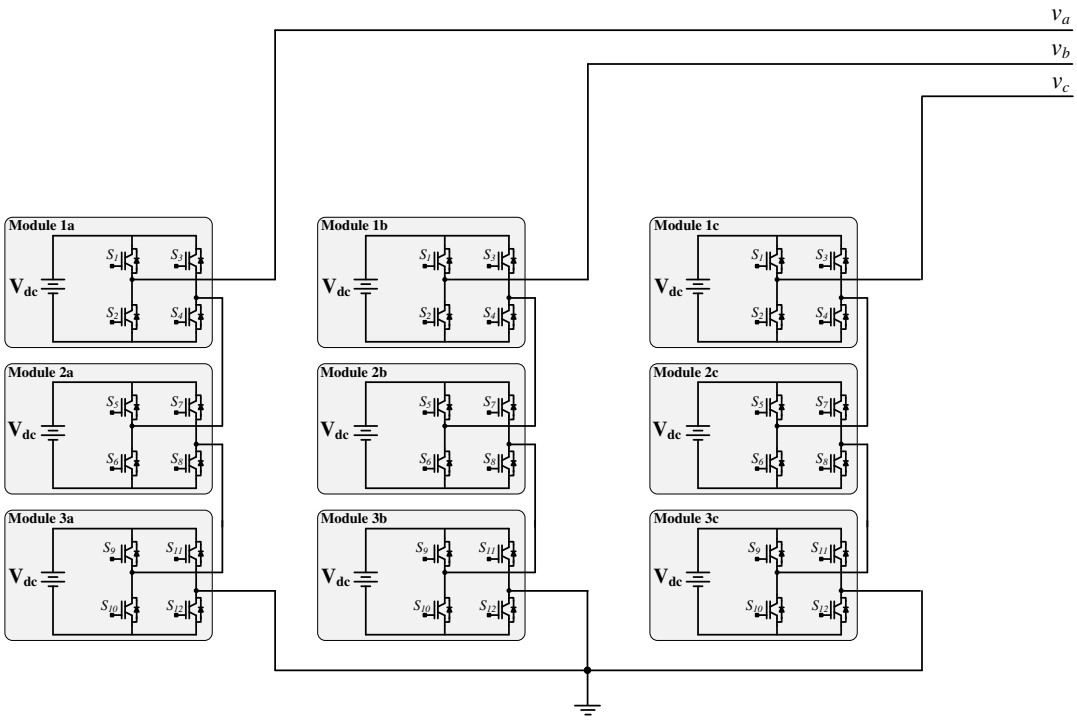


Figure 3:31 - Three-phase SCMI with three modules each one.

Figure 3:32 presents the simulated three-phase voltage related to the ground. Each phase-to-ground voltage is equal to that presented in the single-phase SCMI study.

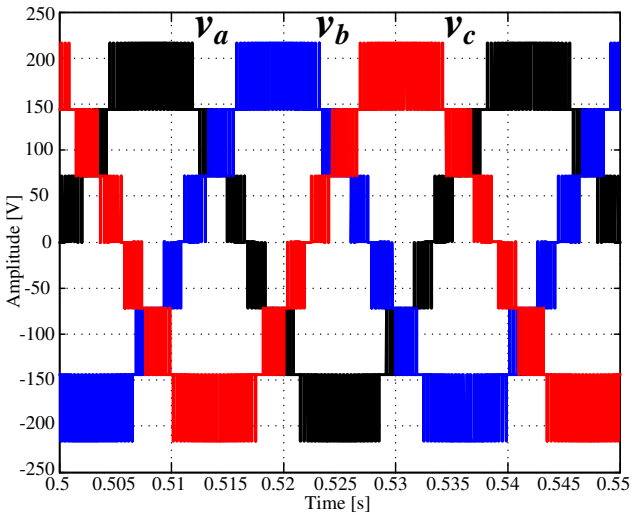


Figure 3:32 – Simulated three-phase voltage related to the ground.

Figure 3:33 presents the simulated SCMI line-to-line voltage for modulation index equals to 0.9. The number of level is now 13.

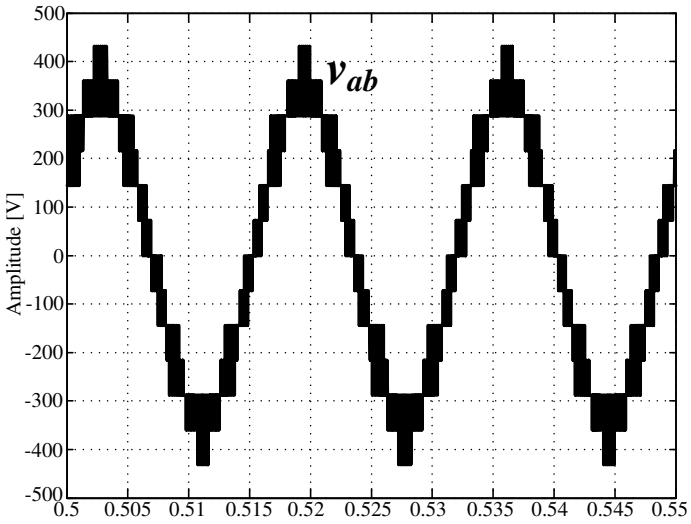


Figure 3:33 – Simulated SCMI line-to-line voltage for m = 0.9.

3.16 Storage system in medium industrial voltage

Applications in medium industrial voltages are more prone to be made by the cascaded symmetric topology mainly because the modularity. The amount of modules tends to be high [45]. High number of modules is an advantage due to the possibility of operation even under some failure in one or more modules. Each modules must be equipped with a mechanism to by-pass its terminals. This section presents a study where a BBS system is applied to a 4.16 kV grid through a SCMI with eight modules. The output voltage can present up to 17 levels. Then, a failure is emulated in one of the modules. Figure 3:34 presents the BBS connected to a medium industrial voltage grid.

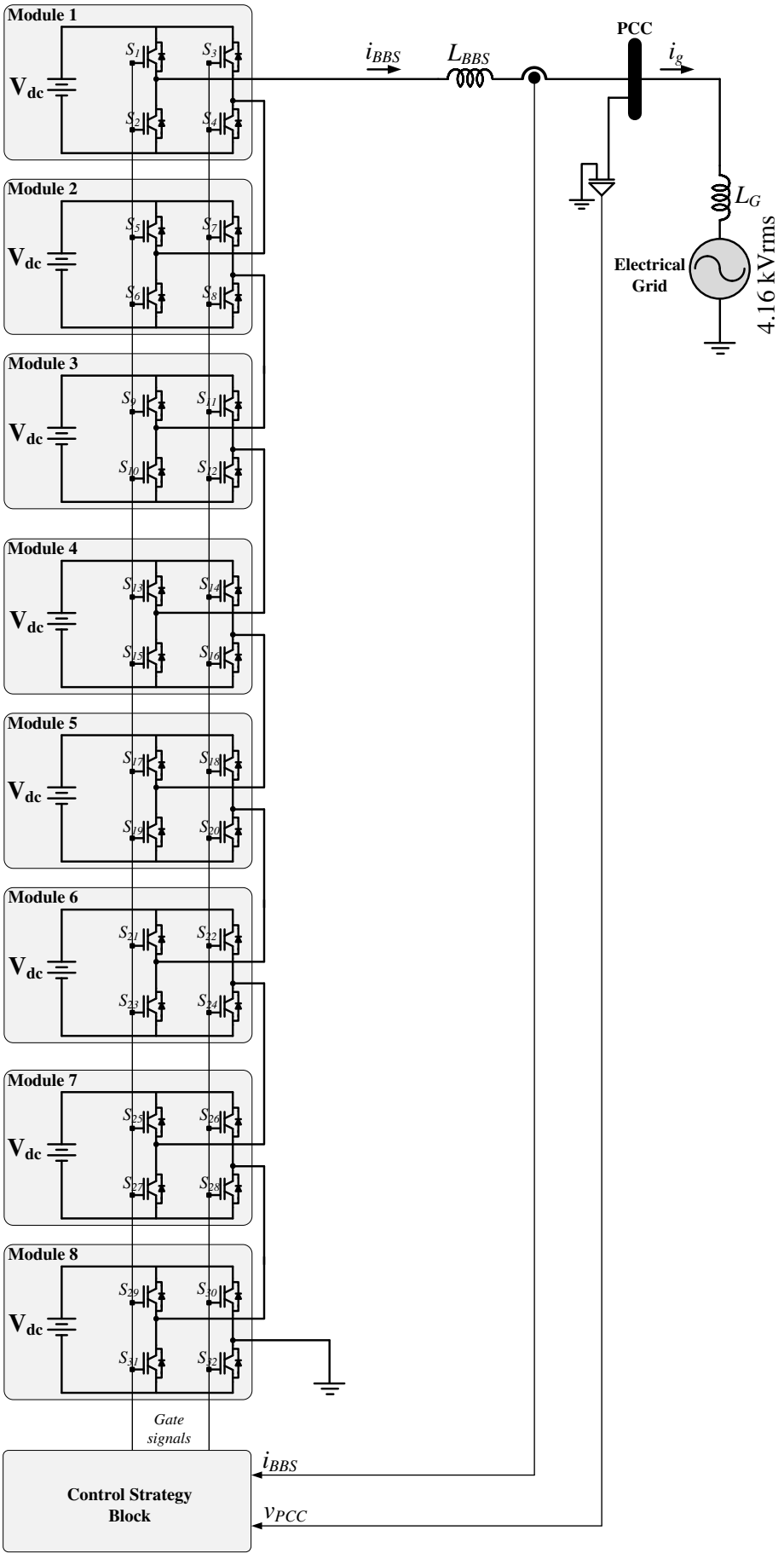


Figure 3:34 - BBS connected to a 4.16 kV grid.

Table 3:3 presents the parameters used in the simulation.

Table 3:3 – Parameters used in the simulation.

Parameter	**Value**
BBS Nominal Power	P_{BSS} = 2.5 MW
BBS Nominal Energy	E_{BBS} = 2.5 MWh
VDC Voltage for each module	V_{dc} = 900 V
BBS output inductance (3.14)	L_{BBS} = 900 uH
PI time constant	T_{P_BBS} = 15 ms
PI proportional gain (3.29)	k_{p_BBS} = 0.020325

A failure in one of the modules is emulated. The module under fault is removed through by-passing its terminal point. It is assumed that there is a system to detect and to set the by-pass mechanism. After the failure, the BBS passes to operate with seven modules. No changes are made in the control structure. The condition to make the BBS to continue operating in the same way before and after the failure is that the terminal voltage in steady-state condition must be made by 15 levels. In other words, before the failure, the control imposes a terminal voltage with 15 levels.

Figure 3:35 presents the simulated PCC voltage and the BBS current when one module is by-passed. Initially, the current is sinusoidal and in-phase with the PCC voltage. At narrow position, the module 8 is by-passed. The BBS current is kept unchanged, except for the appearance of a small distortion.

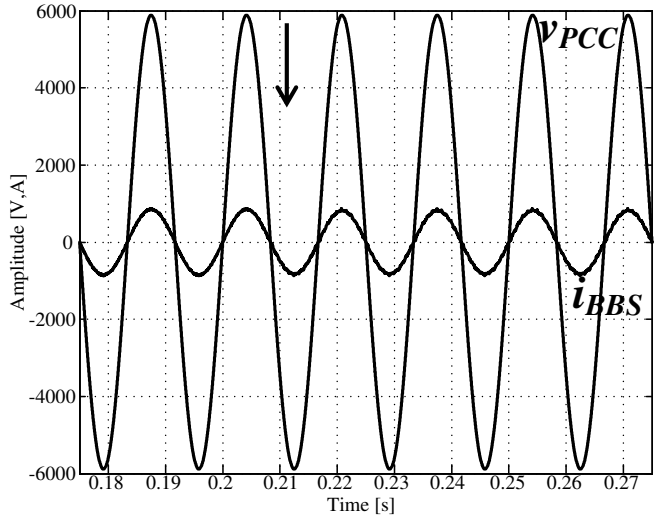


Figure 3:35 – Simulated PCC voltage and the BBS current when one module is by-passed.

Figure 3:36 presents the BBS terminal voltage when the module is by-passed. The terminal voltage is composed by 15 levels before and after the failure. Afterwards, the terminal voltage presents minimal distortions.

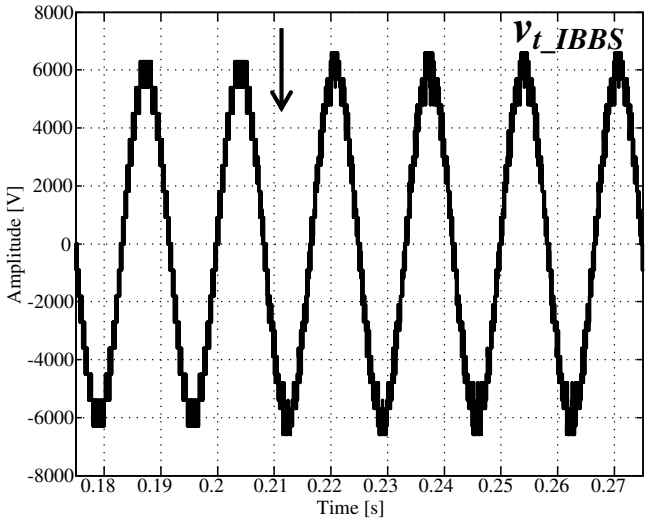


Figure 3:36 – Simulated BBS terminal voltage when one module is by-passed.

The BBS should signalize that its operation has one module bypassed. Then, an operator may provide the maintenance. The modularity of the BBS can guarantee the replacement of the module under fault without interrupting the operation. Therefore, a BBS made by SCMI is an attractive choice for applications in medium industrial voltage.

4 STUDY AND IMPLEMENTATION OF ASYMMETRICAL CASCADED MULTILEVEL INVERTER

This chapter presents the study and implementation of an ACMI. Initially, the study approaches the {1:2:6} and {1:3:9} topologies. Later, an ACMI with three modules in {1:2:6} is deeply studied and verified through simulations and experimental results. The features found in the {1:2:6} ratio are extended to {1:3:9} with minimal changes. Details about the simulation are given in Appendix C.

4.1 The asymmetrical cascaded multilevel inverter

The module DC-link voltages are commonly scaled in {1:2:6:…} and {1:3:9,…} ratios. However, some applications has been reported in the literature covering different ratios [58], [59]. Figure 4:1 presents a single-phase *k*-level ACMI with *n* modules. Each module has an isolated DC source. The ACMI terminal voltage is called v_{ta} while the module terminal voltages are called v_{ta1}, v_{ta2} and v_{tan}, respectively. The subscript *a* means "asymmetrical" and it should not be misunderstood with phase *A*.

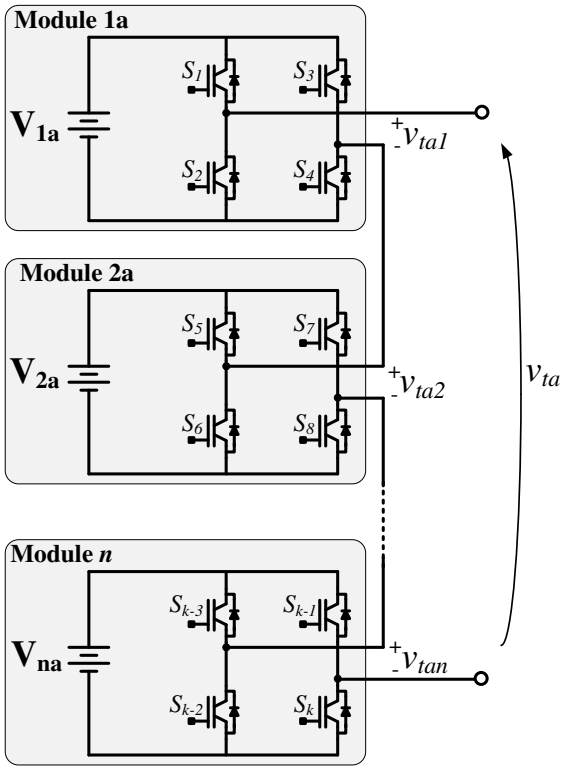


Figure 4:1 - Single-phase *k*-level symmetrical cascaded multilevel inverter with *n* modules.

The number of levels (k_r) in the terminal voltage (v_{ta}) for the {1:2:6:…} ratio is given by (4.1).

$$k_{r126..} = 2 \cdot 3^{n-1} + 1 \tag{4.1}$$

The number of levels in the terminal voltage (v_{ta}) for the {1:3:9:…} ratio is given by (4.2).

$$k_{r139...} = 3^{n} \tag{4.2}$$

The terminal voltage is composed by the algebraic sum of each module terminal voltage. Figure 4:2 presents the fundamental frequency diagram of the ACMI.

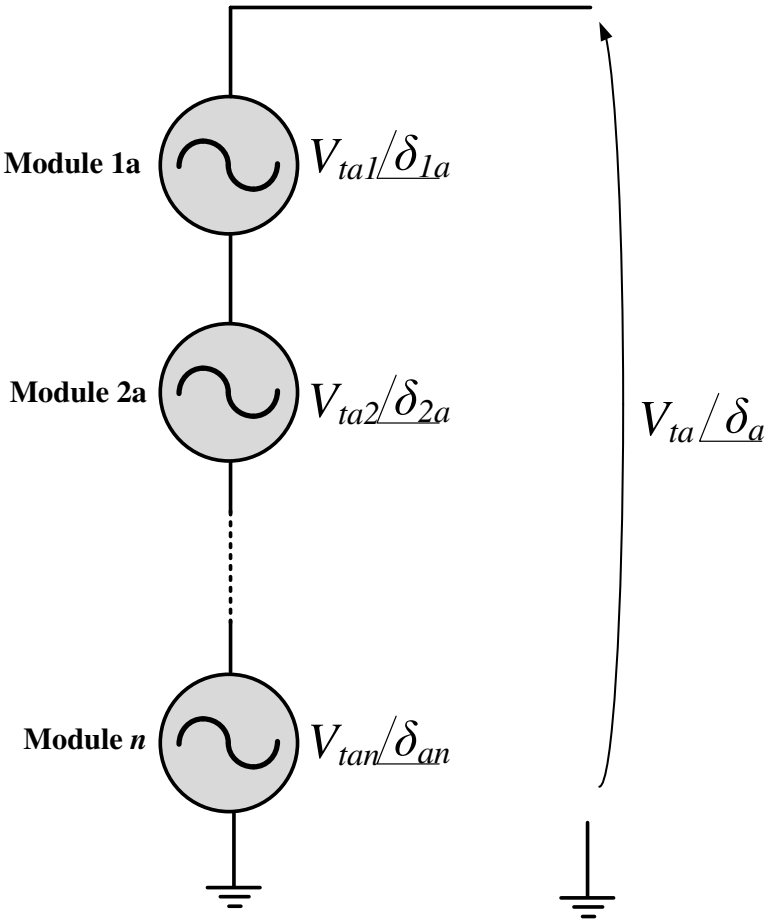


Figure 4:2 - Fundamental frequency diagram of the ACMI.

Similarly to the SCMI, the angles at the fundamental frequency of the module terminal voltage are equal to that found at the ACMI terminal voltage due to the waveform symmetry. The angles are written as (4.3).

$$\delta_a = \delta_{1a} = \delta_{2a} = ... = \delta_{na} \tag{4.3}$$

4.2 Modulation strategy

The ACMI needs a suited modulation in order not to lose its main advantage, which is the low switching frequency at the module with higher voltage. The application of PWM in the ACMI is not feasible due to its inherent high switching frequency. If the PWM is

applied, all modules operate in high switching frequency and the ACMI is better replace to a single H-bridge inverter.

The most common modulation applied in ACMI is the Staircase [60]–[63], also known sometimes as Nearest-Level Modulation [64], [65]. Figure 4:3 presents the principle of operation of the staircase modulation for an ACMI with three modules. This principle is valid for any ratio among the DC-link voltages. For the module with higher voltage, the reference signal (a sinusoidal in this case) is compared to a positive and a negative DC value. The DC values correspond to a direct relation to the values found in the DC sources. For example, for {1:2:6} case and for a reference with amplitude equals to one, the DC positive and negative values in the comparators for the module 1, 2 and 3 are 1/18, 1/9 and 1/3, respectively.

If the reference is higher than the DC value, in the positive semi cycle, the comparator output is positive. Otherwise, it is null. Similar procedure is applied to the negative semi cycle. The output signal of the comparator is the switch pattern to be applied to transistor of the referred module. Moreover, the output signal is subtracted from the reference and the resulting signal is the reference for the next module. Then, this reference is compared to another positive and negative DC values. The process is repeated until the last module has its switch pattern. The DC values used in the comparators are the half of the corresponded module DC-link voltage.

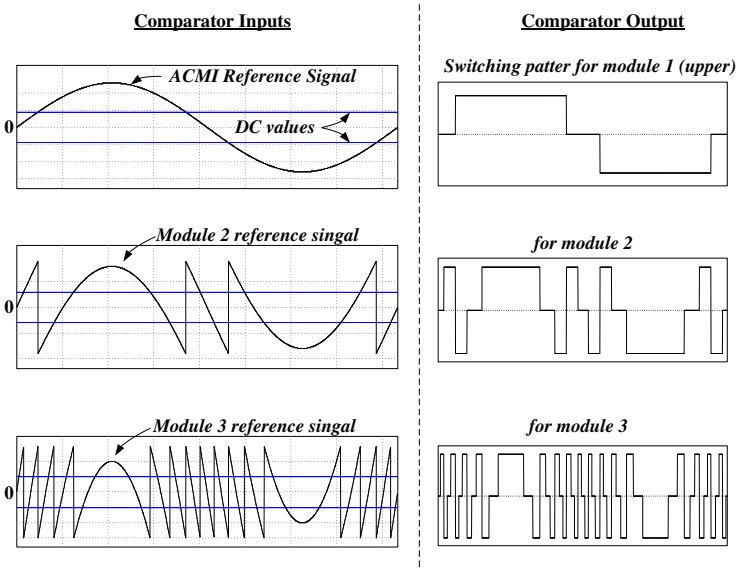


Figure 4:3 - Principle of operation of the staircase modulation for an ACMI with three modules.

4.3 Asymmetrical cascaded multilevel inverter with staircase modulation

This section presents an ACMI, composed by three modules voltage scaled in {1:2:6}, and equipped with staircase modulation. Figure 4:4 presents the ACMI with three

modules. The DC voltages are named as VDCa, 2VDCa and 6VDCa. The module 1a, 2a and 3a are called throughout this thesis as Upper, Middle and Lower Module, respectively.

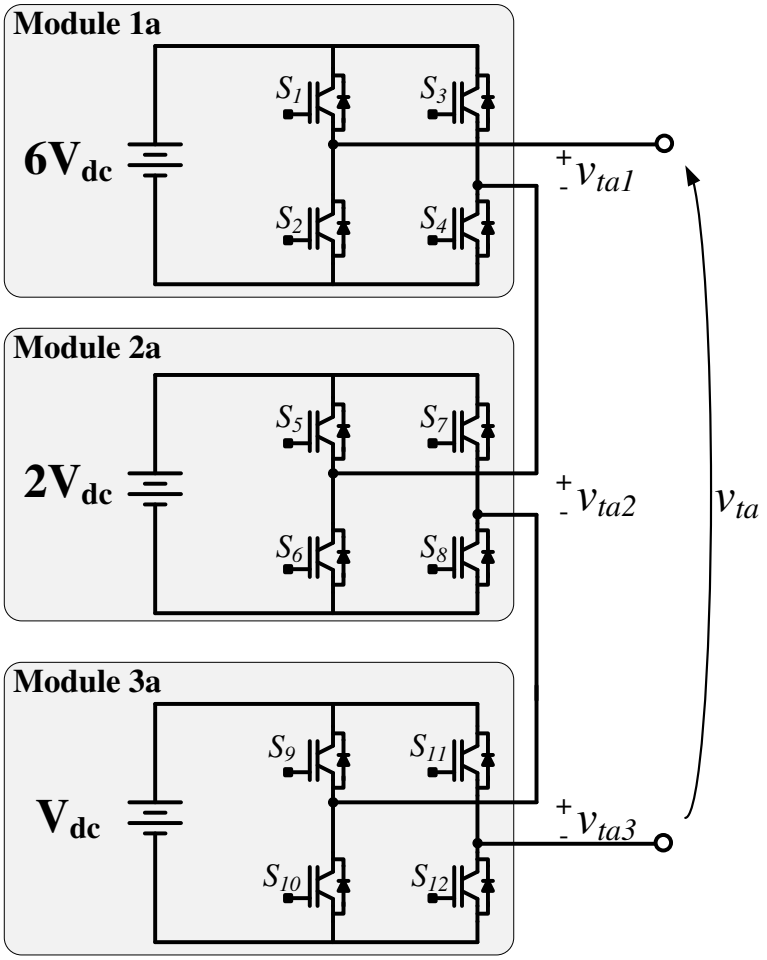


Figure 4:4 – ACMI with three modules.

Figure 4:5 presents how to obtain each transistor gate signal in an ACMI with three modules and staircase modulation. Notice that the values used in the comparators of the staircase modulation are evident. If the {1:3:9} ratio is desired, it is enough to change the constants used in the comparator input.

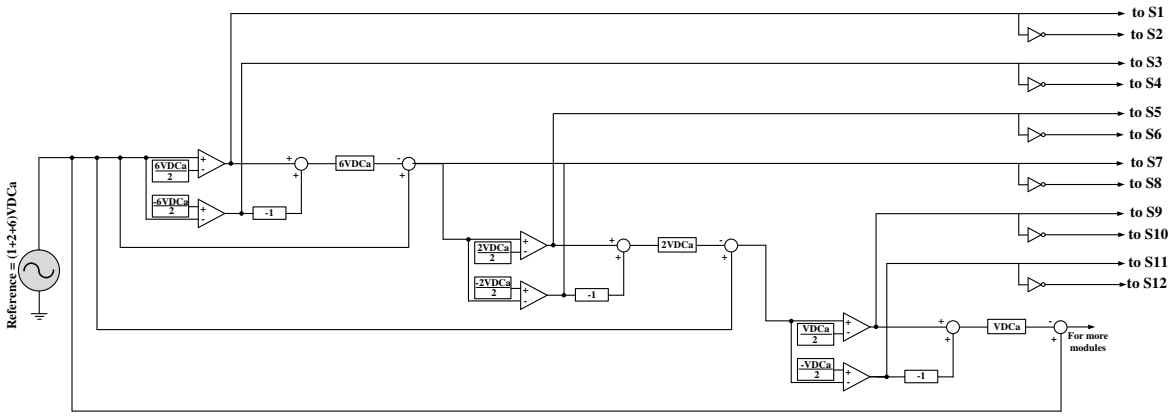


Figure 4:5 - How to obtain each transistor gate signal in an ACMI with three modules and staircase modulation.

Figure 4:6 presents the input signals of the comparators.

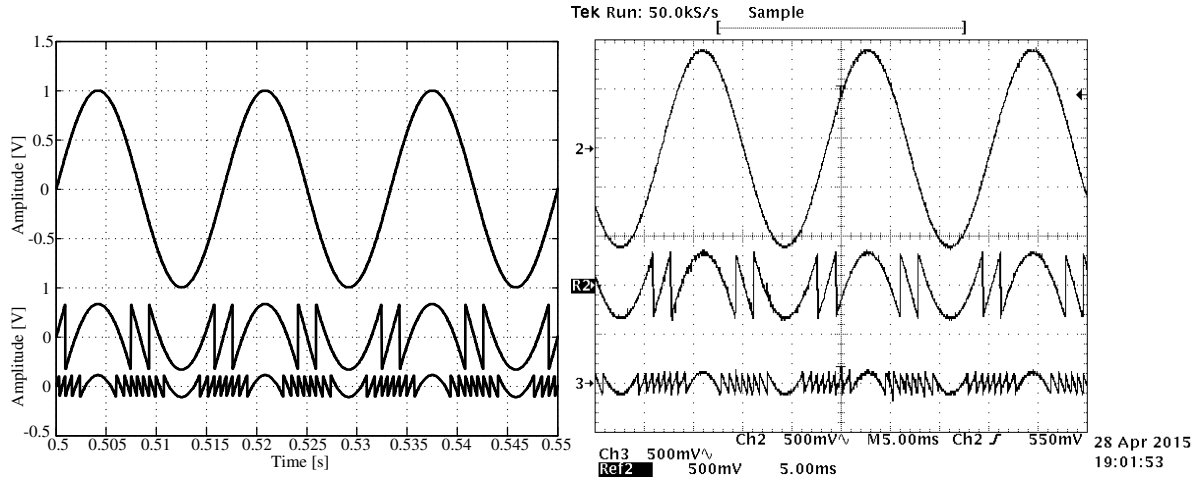


Figure 4:6 – Input signals of the comparators. (a) Simulation and (b) Experimental.

The terminal voltage of the upper module is given by [34] (4.4).

$$v_{ta1}(t)=\frac{4V_{dc}}{\pi}\sum_{m_a=0}^{\infty}\frac{1}{2p+1}\sin\left\{\left[2m_a+1\right]\cos^{-1}\left(\frac{1}{3M}\right)\right\}\cos\left(\left[2m_a+1\right]\omega_0 t\right) \quad (4.4)$$

Where M is the modulation index and ω_0 is the reference signal angular frequency.

The terminal voltage of the middle module is given by (4.5).

$$\begin{aligned} v_{ta2}(t)=&\frac{3}{2}MV_{dc}\cos(\omega_0 t)-\frac{8V_{dc}}{\pi}\sum_{m_a=0}^{\infty}\frac{1}{\left[2m_a+1\right]}\sin\left\{\left[2m_a+1\right]\cos^{-1}\left(\frac{1}{3M}\right)\right\}\cos\left(\left[2m_a+1\right]\omega_0 t\right)\\ &+\frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{\substack{p=\infty\\ p\neq 0}}^{\infty}\frac{1}{m_a}J_{2p+1}(3\pi m_a M)\cos\left(\left[m_a+x\right]\pi\right)\cos\left(\left[2m_a+1\right]\omega_0 t+2m_a\omega_c t\right) \end{aligned} \quad (4.5)$$

Figure 4:7 presents the terminal voltage of the upper module and its spectrum. As expected, the upper module terminal voltage has low switching frequency and low frequency spectrum components. At this point, the reduction in the power losses is evident. The upper module terminal voltage has four commutations in 60 Hz cycle, valid for sinusoidal reference. This means that each transistor in the upper module turns-on and off once in such cycle. Consequentially, the formation of the area which represents the switching losses, as depicted previously in Figure 2:2c, happens just once for each transistor in 60Hz cycle. Therefore, the ACMI has lower switching losses compared to a classical PWM based inverter. Similar feature is found in the central and lower module, as observed in the next figures.

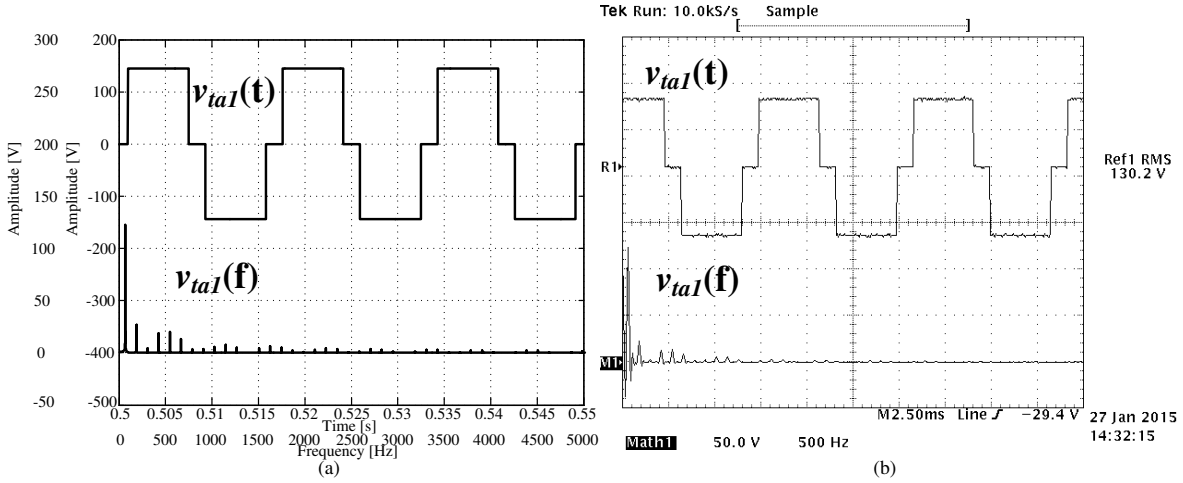


Figure 4:7 - Terminal voltage of the upper module and its spectrum. (a) Simulation and (b) Experimental.

Figure 4:8 presents the terminal voltage of the middle module its spectrum. There are also low frequency components.

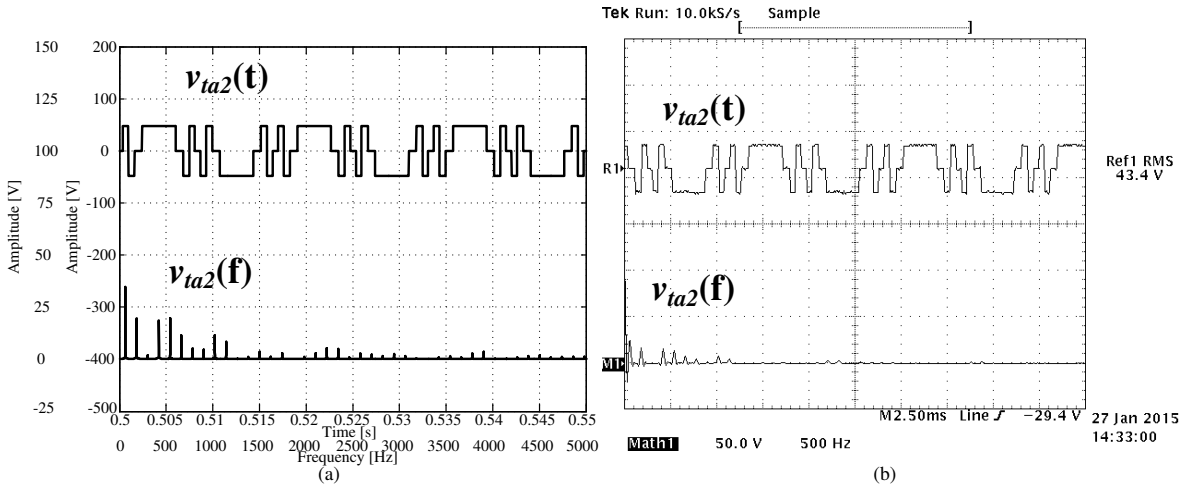


Figure 4:8 - Terminal voltage of the middle module its spectrum. (a) Simulation and (b) Experimental.

Figure 4:9 presents the terminal voltage of the lower module and its spectrum. The spectrum decreases as the frequency increases.

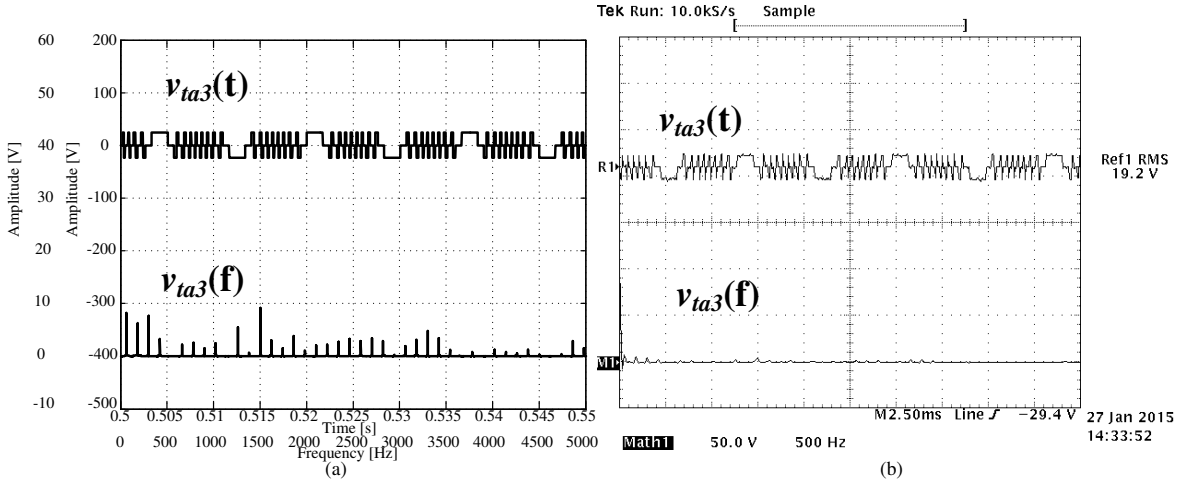


Figure 4:9 - Terminal voltage of the lower module and its spectrum. (a) Simulation and (b) Experimental.

Figure 4:10 presents the ACMI terminal voltage and its spectrum. The voltage has nineteen levels and it is close to a sinusoidal waveform. The low frequencies components are cancelled with each other. Since the terminal voltage has no significant harmonic components, the output filter is minimzed.

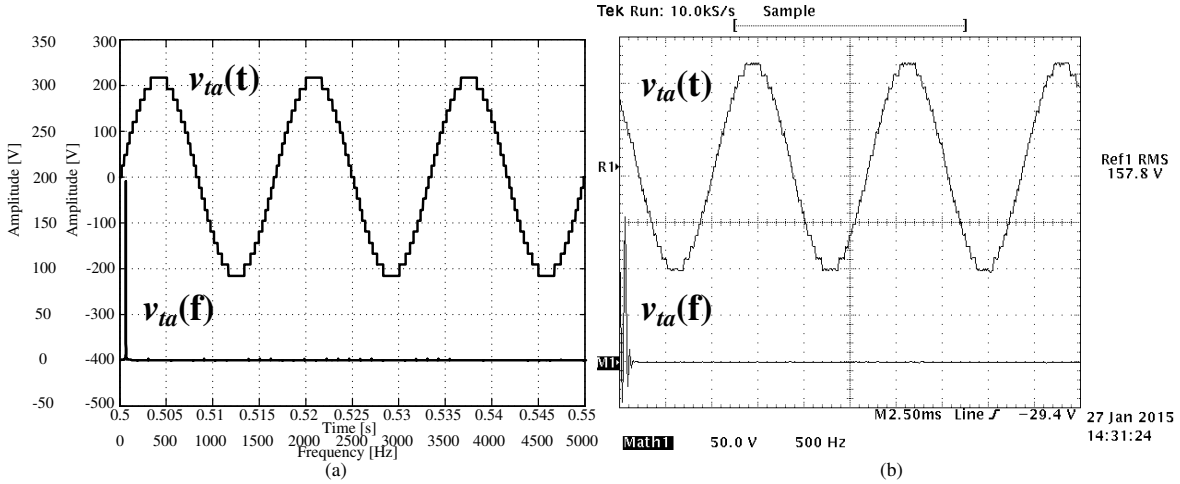


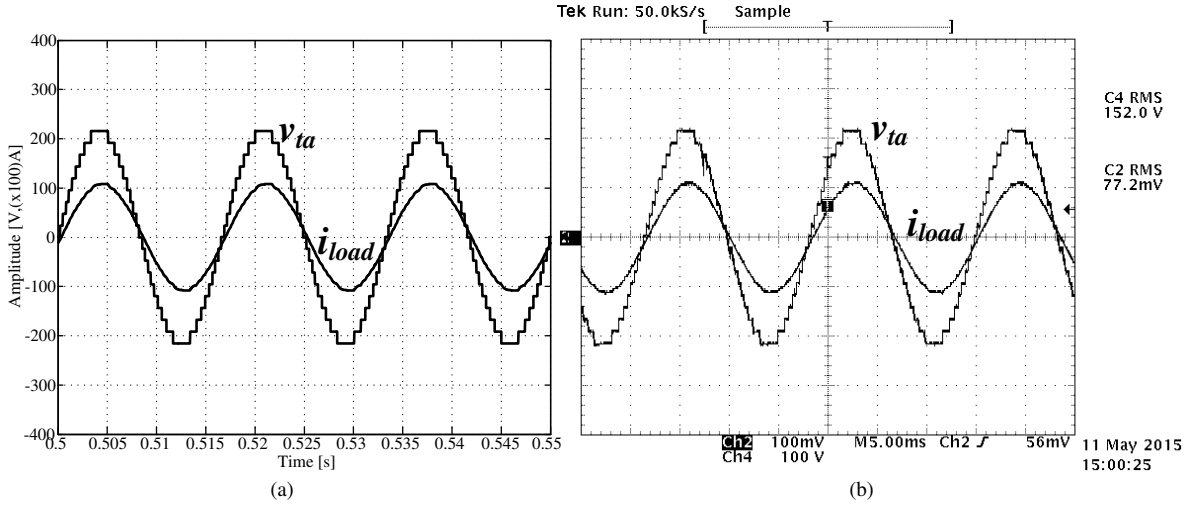
Figure 4:10 - ACMI terminal voltage and its spectrum. (a) Simulation and (b) Experimental.

4.4 Redundant commutations

Different from the SCMI, the ACMI does not face redundant commutations. Each value at the ACMI terminal voltage is made by one, and only one transistor state.

4.5 Concerning the DC-link currents

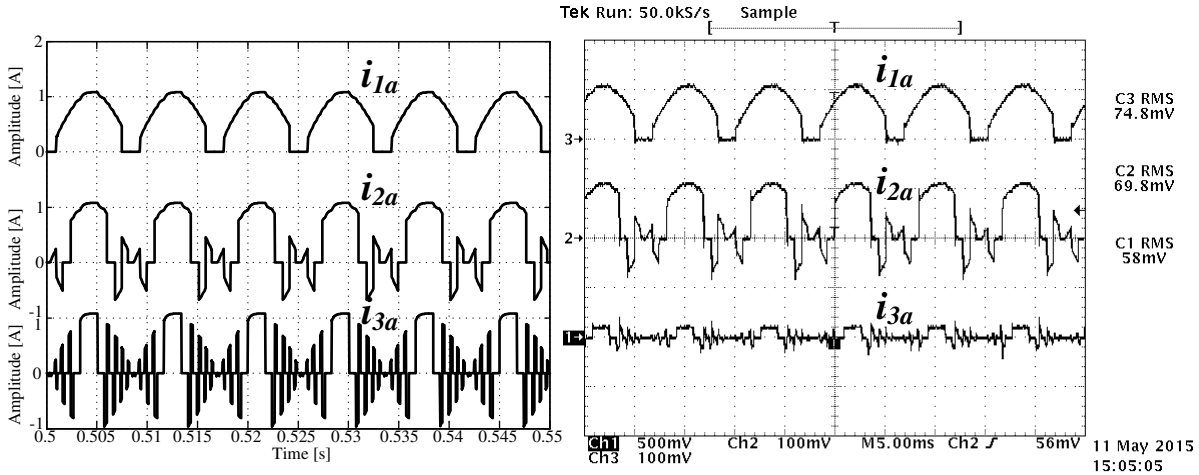
A RL load with two distinguished configuration is connected to the ACMI output in order to verify the DC-link currents. Figure 4:11 presents the ACMI terminal voltage and the load current for R = 200 Ω and L = 57 mH. The load current is sinusoidal and almost in-phase with the voltage.



(a) (b)

Figure 4:11 - ACMI terminal voltage and the load current for R = 200 Ω and L = 57 mH. (a) Simulation and (b) Experimental (Ch2: 0.1V/A).

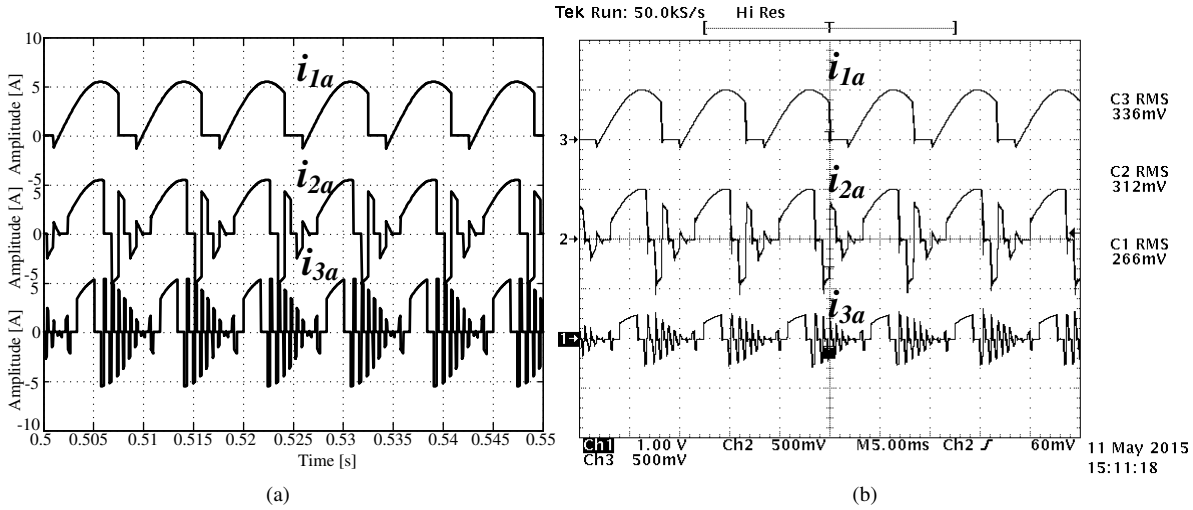
Figure 4:12 presents DC-link current for the three modules. The DC-link current for the upper module has only positive values. The middle and lower modules have moments with negative values and pulsating behavior. The average of all DC-link currents is positive.



(a) (b)

Figure 4:12 - DC-link current for the three modules for R = 200 Ω and L = 57 mH. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch3: 0.1V/A).

Figure 4:13 presents the DC-link current for the three modules for R = 33 Ω and L = 57 mH. The experimental result was collected in high resolution for better visualization of the lower module DC-link current. The DC-link current at the upper module has negative value and it is intensified as the load increases.



(a) (b)

Figure 4:13 - DC-link current for the three modules for R = 33 Ω and L = 57 mH. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch3: 0.1V/A).

The employment of a DC-DC converter for minimizing the effect of a pulsating current is usually not applicable in ACMI, except for the lower module. The upper module switches at 60Hz while the DC-DC converter needs to switch at some tens of kilohertz. The transistors of the DC-DC and the inverter should be sized differently in frequency. Since high-frequency transistors are used in the upper module, the entirely ACMI is better replaced to a conventional H-bridge PWM inverter.

Similarly to the SCMI, capacitors are used in the DC-link of the modules. The capacitor, combined to the internal resistance of the battery, makes a low-pass filter for the DC current. Figure 4:14 presents the DC-link current for the upper module when a capacitors are used in parallel to the batteries, valid for the load R = 200 Ω and L = 57 mH. The current is continuous.

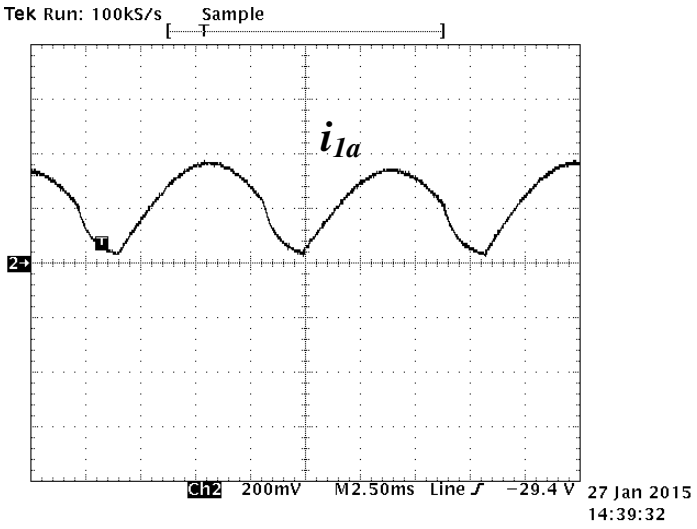


Figure 4:14 - DC-link current for the upper module when capacitors are used in parallel to the batteries (Ch2: 0.1V/A).

Figure 4:15 presents the DC-link current for the middle module. Comparing to the Figure 4:12, the current presents softer transitions.

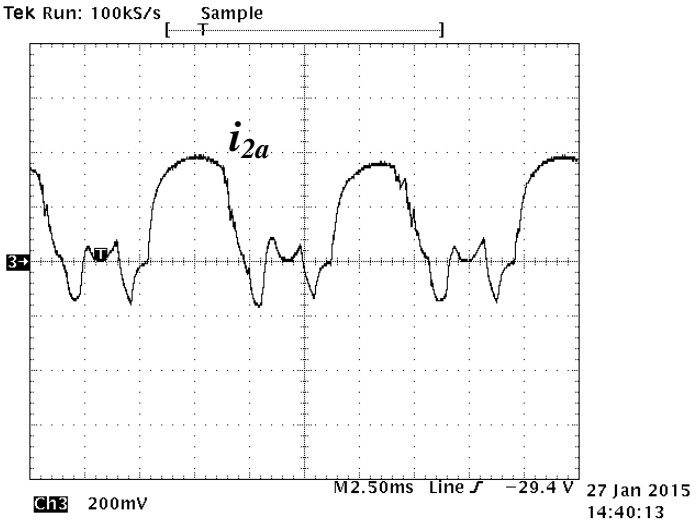


Figure 4:15 - DC-link current for the middle module (Ch3: 0.1V/A).

Figure 4:16 presents the DC-link current for the lower module. Similarly, the current faces lower severe transitions.

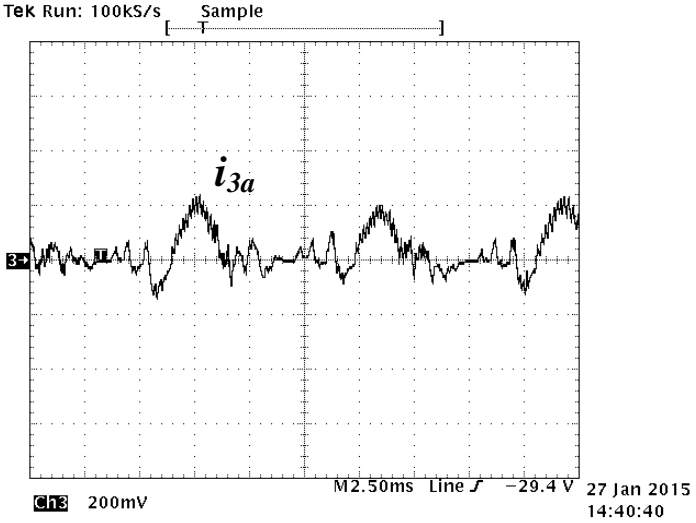


Figure 4:16 - DC-link current for the lower module (Ch3: 0.1V/A).

4.6 Power distribution

Once the DC-link voltages are different in each module, it is expected an unequal power distribution among them. For the sake of simplicity, the analysis covered in this section assumes that the ACMI is injecting active power into the grid with unit power factor, seen by the grid. The ACMI is considered ideal. Figure 4:17 presents the ACMI connected to the grid.

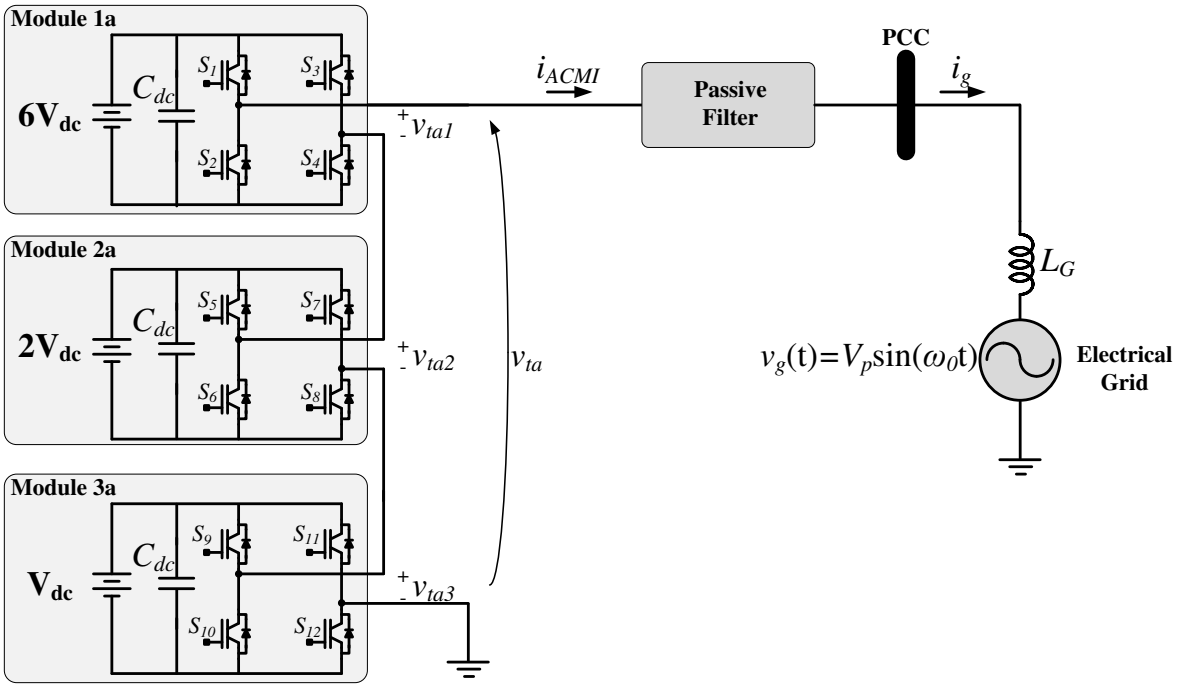


Figure 4:17- The ACMI connected to the grid.

The ACMI terminal voltage is assumed sinusoidal, given by (4.6).

$$v_{ta}(t) = m_a\left(y_u + y_m + y_l\right)V_{dc}\sin(\omega t) \tag{4.6}$$

where m_a is the modulation index and $y_{u,m,l}$ is given by (4.7), for the {1:2:6} ratio.

$$\begin{bmatrix} y_u \\ y_m \\ y_l \end{bmatrix} = \begin{bmatrix} 6 \\ 2 \\ 1 \end{bmatrix} \tag{4.7}$$

And the ACMI output current is given by (4.8).

$$i_{ACMI}(t) = \frac{m_a\left(y_u + y_m + y_l\right)V_{dc}}{Z}\sin\left(\omega t - \varphi\right) \tag{4.8}$$

where φ is the angle between the ACMI current and ACMI terminal voltage and Z is a fictitious load impedance. The angle is not null since the current is synchronized to the grid

The ACMI active power in function of the modulation index in is given by (4.9).

$$p_{ACMI}(m) = \frac{1}{T}\int_{t_0}^{t_0+T} v_{ta}(t)\,i_{ACMI}(t)\,dt \tag{4.9}$$

Replacing (4.6) and (4.8) into (4.9), the active power may be given as (4.10)

$$p_{ACMI}(m_a) = {m_a}^2\frac{\left(y_u + y_m + y_l\right)^2 {V_{dc}}^2\cos(\varphi)}{2Z} \tag{4.10}$$

Normalizing the power by its maximum value, the per unit active power is given by (4.11).

$$p_{ACMI}(m_a) = {m_a}^2 \quad [pu] \tag{4.11}$$

Each module terminal voltage is a function of the modulation index and also of the switching function (s). The per unit power at the upper module is given by (4.12) [66], [67].

$$p_{upper}\left(m_a\right)=\frac{y_u}{\frac{k_r-1}{2}}m_a S_{upper}(m_a) \tag{4.12}$$

where $S_{upper}(m_a)$ is given by (4.13).

$$S_{upper}(m_a)=\frac{4}{m_a\pi}\Re\left\{\sqrt{{m_a}^2-{c_1}^2}\right\} \tag{4.13}$$

And c_1 is the DC value used in the comparator presented in section 5.3 in per unit. In this case, c_1 is given by (4.14).

$$c_1=\frac{y_u}{k_r-1} \tag{4.14}$$

Similarly, the per unit power at the middle module is given by (4.15).

$$p_{middle}\left(m_a\right)=\frac{y_m}{\frac{k_r-1}{2}}m_a S_{middle}(m_a) \tag{4.15}$$

where $S_{middle}(m_a)$ is given by (4.16).

$$S_{middle}(m_a)=\frac{4}{m\pi}\left(\begin{array}{l}\Re\left\{\sqrt{{m_a}^2-{c_2}^2}\right\}+\Re\left\{-2\sqrt{{m_a}^2-{c_1}^2}\right\}+\Re\left\{\sqrt{{m_a}^2-\left(2c_1-c_2\right)^2}\right\}\\+\Re\left\{\sqrt{{m_a}^2-\left(2c_1+c_2\right)^2}\right\}\end{array}\right) \tag{4.16}$$

And c_2 is given by (4.17).

$$c_2=\frac{y_m}{k_r-1} \tag{4.17}$$

The per unit power at the lower module is given by (4.18).

$$p_{lower}\left(m_a\right)=\frac{y_l}{\frac{k_r-1}{2}}m_a S_{lower}(m_a) \tag{4.18}$$

where $S_{lower}(m_a)$ is given by (4.19).

$$S_{lower}(m_a)=\frac{4}{m\pi}\left(\begin{array}{l}\Re\left\{\sqrt{m^2-c_3^{\,2}}\right\}+\Re\left\{-2\sqrt{m^2-c_2^{\,2}}\right\}+\Re\left\{\sqrt{m^2-\left(2c_2-c_3\right)^2}\right\}+\Re\left\{\sqrt{m^2-\left(2c_2+c_3\right)^2}\right\}\\ +\Re\left\{-2\sqrt{m_a^{\,2}-c_1^{\,2}}\right\}+\Re\left\{\sqrt{m_a^{\,2}-\left(c_1+c_2-c_3\right)^2}\right\}+\Re\left\{\sqrt{m_a^{\,2}-\left(c_1+c_2+c_3\right)^2}\right\}\\ +\Re\left\{\sqrt{m_a^{\,2}-\left(2c_1-c_3\right)^2}\right\}+\Re\left\{\sqrt{m_a^{\,2}-\left(2c_1+c_3\right)^2}\right\}+\Re\left\{-2\sqrt{m_a^{\,2}-\left(2c_1-c_2\right)^2}\right\}\\ +\Re\left\{-2\sqrt{m_a^{\,2}-\left(2c_1+c_2\right)^2}\right\}+\Re\left\{\sqrt{m_a^{\,2}-\left(2c_1+2c_2-c_3\right)^2}\right\}\\ +\Re\left\{\sqrt{m^2-\left(2c_1+2c_2+c_3\right)^2}\right\}\end{array}\right) \tag{4.19}$$

And c_3 is given by (4.20).

$$c_3=\frac{y_l}{k_r-1} \tag{4.20}$$

The previous analysis is now evaluated in the two ratios {1:2:6} and {1:3:9}.

Table 4:1 presents the constants used in the equation in order to plot processed power in the modules.

Table 4:1 - The constant used in the equations in order to plot the processed power in each module.

Variable	**Value for {1:2:6}**	**Value for {1:3:9}**
y_u	6	9
y_m	2	3
y_l	1	1
k_r	19	27
c_1	6/18	9/26
c_2	2/18	3/26
c_3	1/18	1/26

Figure 4:18 presents the processed power in each module and the ACMI total power versus the modulation index. The charts are for the ratios {1,2,6} and {1,3,9} and they are normalized to the ACMI total power.

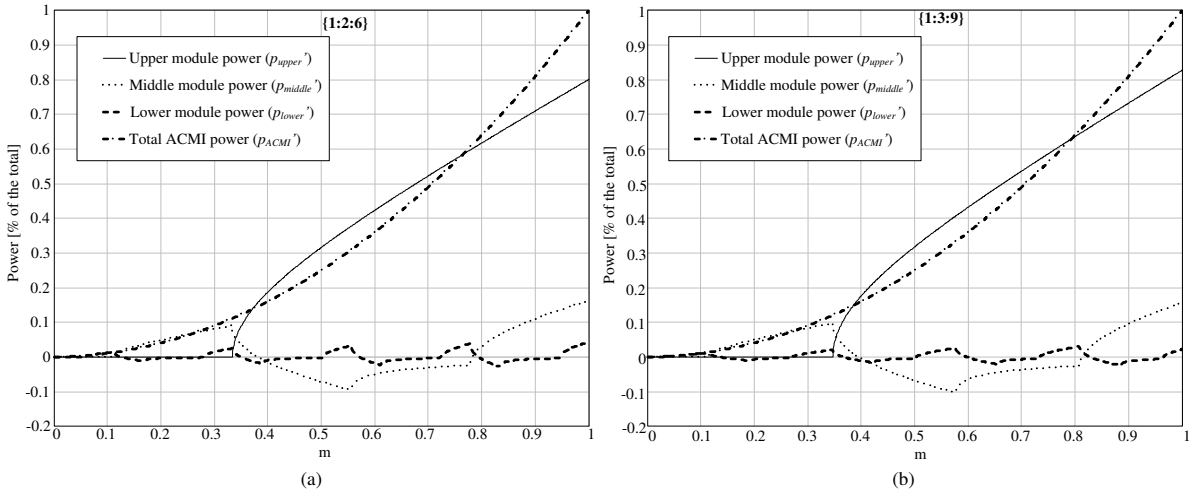


Figure 4:18 - Processed power in each module and the ACMI total power versus the modulation index. (a) For {1:2:6} and (b) for {1:3:9}.

Four features can be highlighted from the chart:

i) There are moments when the processed power is negative in the middle and lower modules, called as regenerative power. It indicates power consumption from a module while the ACMI is intended to supply, resulting in a contradiction. Such behavior may happen even if the ACMI is connected to an isolated passive load. The consumed power comes from the adjacent modules.
Some researches dealing with how to overcome the negative power have been reported in the literature [68], [69]. In [68] the authors use the asymmetrical topology with three modules and present a solution to guarantee positive power for any modulation index. However, the amount of levels at the terminal voltage is reduced from 19 to 13. Additionally, the DC voltages are scaled in the ratio {1:0.408:0.267}. In battery-based storage, such ratio is practically impossible to be achieved. In [69], the authors also use the asymmetrical topology with three modules. The proposal is to replace the upper module by a hybrid module. However, the amount of level is reduced to nine and the DC voltages scaled in the ratio {1:1:2}.

ii) The range where the three modules process positive power simultaneously (without applying any solution) is very limited. For the {1:2:6}, the range comprises the modulation index from 0.94 to 1. In {1:3:9}, from 0.96 to 1. There is also a short range also around m = 0.77 for the {1:2:6} and around m = 0.82 for {1:3:9}.

iii) The upper module can process from 0 to 127% of the total ACMI power for the {1:2:6} and {1:3:9}. For m = 1, the upper module process 80% of the total

power in {1:2:6} and 83% in {1:3:9}. In {1:2:6} for m = 0.76, the upper module process 100% of the ACMI total power. For the range m = [0.36 0.77] in the {1:2:6}, the upper module process more than 100% of the total power. As result, the remaining modules consume the excessive power.

iv) The lower modules processes at most 4.2% of total power in {1:2:6} and 3.2% in {1:3:9}. Processing lower power allows the lower module be modified without compromising the whole operation. For instance, the H-bridge can be replaced by a bidirectional high frequency DC link [70]. Similar analysis can be done to the middle module. This module processes at most 17% in {1:2:6}.

Figure 4:19 presents results for m = 0.93 for {1:2:6}. The variables presented are the PCC voltage, the ACMI current and the instantaneous power for each module. The measurements indicate the active power. The values may change between the simulation and experimental mainly due to the non-idealities found in the prototype. Lead-acid batteries were used in the modules DC links.

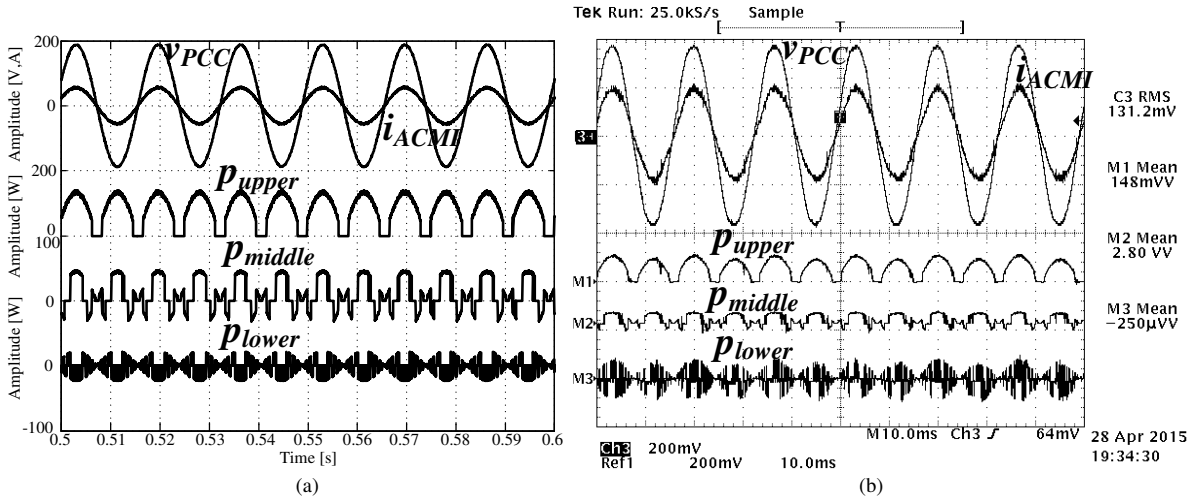


Figure 4:19 - Results for m = 0.93 for {1:2:6}. (a) Simulation and (b) Experimental (Ch3: 0.1V/A).

According to the chart for {1:2:6} and for m = 0.93, the percentage processed on the upper module related to the total power is given by (4.21).

$$p_{upper} = \frac{p_{upper}'}{p_{ACMI}'} = \frac{0.73696}{0.8649} = 85,21\% \tag{4.21}$$

By taking the measurement on the experimental result, the ACMI total power is given by (4.22).

$$p_{ACMI} = REF1_{RMS} \cdot CH3_{RMS} \tag{4.22}$$

$$\therefore p_{ACMI} = 133 \cdot 1.31 = 174.2W \tag{4.23}$$

Experimentally, the percentage processed on the upper module related to the total power is given by (4.24).

$$p_{upper} = \frac{M1_{mean}}{p_{ACMI}} \tag{4.24}$$

$$\therefore p_{upper} = \frac{148}{174.2} = 84,96\% \tag{4.25}$$

Similarly, the percentage processed on the middle module related to the total power according to the chart is given by

$$p_{middle} = \frac{p_{middle}'}{p_{ACMI}'} = \frac{0.1299}{0.8649} = 15.02\% \tag{4.26}$$

Experimentally, the percentage processed on the middle module related to the total power is given by (4.27).

$$p_{middle} = \frac{M2_{mean}}{P_{ACMI}} \tag{4.27}$$

$$\therefore p_{middle} = \frac{28}{174.2} = 16\% \tag{4.28}$$

Summing the results in (4.21) and (4.26) the total is higher than 100%. Therefore, it is expected that the lower module process negative power. This is confirmed on the chart and also on the results. The average power is negative. On the simulation, it is clear that the average value of p_{lower} is negative.

According to the chart, the percentage processed on the lower module related to the total power is given by (4.29).

$$p_{lower} = \frac{p_{lower}'}{p_{ACMI}'} = \frac{-0.001989}{0.8649} = -0.23\% \tag{4.29}$$

The value presented in (4.29) is too low to be verified in a lower-power rate experimental setup. However, the power processed in the lower module was evaluated by simulation and the result is -0.29%.

Figure 4:20 presents experimental results for {1:2:6} and for m = 0.96 and m = 0.98. These results correspond to the region where all modules process positive power and they are easily verified by the positive values showed on the measurements. By verifying the above mentioned equations, it shows that the processed power in each module corresponds to those presented in the chart shown in Figure 4:18.

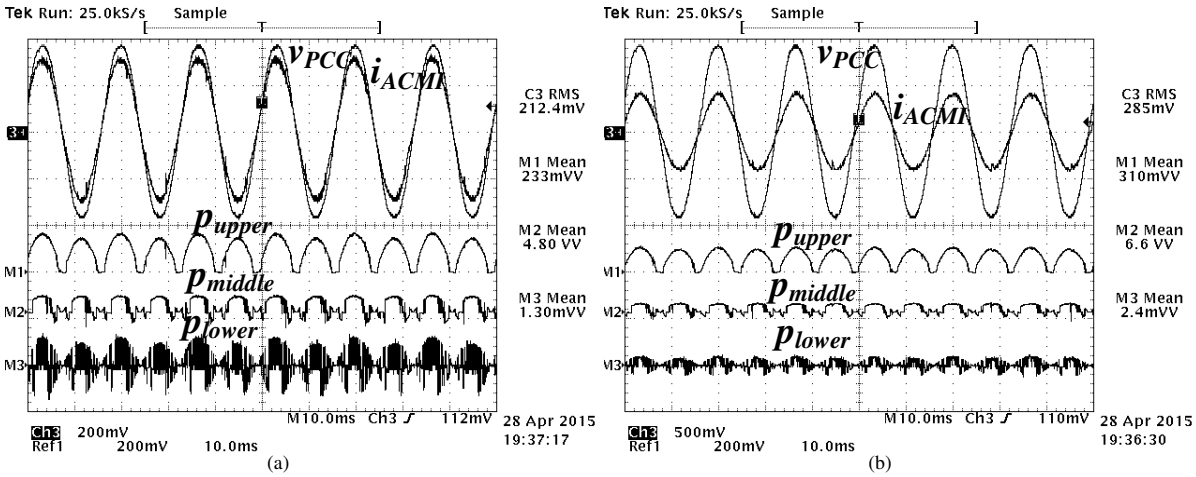


Figure 4:20 - Experimental results for {1:2:6} and for m = 0.96 (a) and m = 0.98 (b) (Ch3: 0.1V/A).

4.7 Why regenerative power must be avoided

Regenerative power must be avoided in storage systems mainly because the conflict which arises in the charge and discharge processes. For example, the Battery Monitoring System (BMS) detects the necessity to charge the batteries. Then, the system begins to charge the batteries. Supposing the occurrence of regenerative power processing in the middle module, the battery banks located at the upper and lower modules will be normally charged. However, the middle module battery bank will be discharged. But the order was to charge all the battery banks. As result, the BMS will not signalize the end of the charging process at the middle module and the system falls in a collapse. Figure 4:21 illustrates the conflict caused by the regenerative power behavior in a charging process.

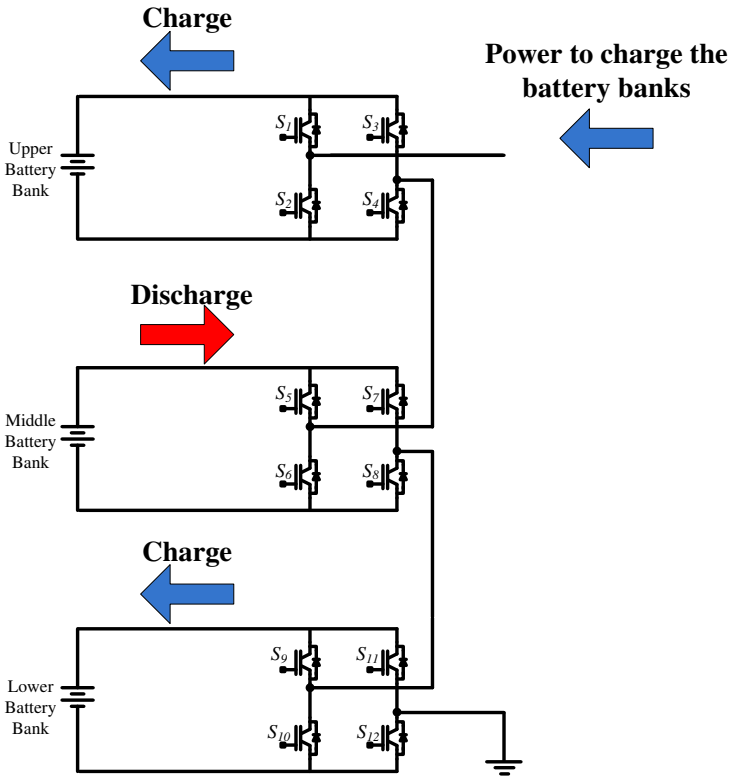


Figure 4:21 - Demonstration of the conflict caused by the regenerative power behavior in a charging process.

4.8 The ACMI output filter

Throughout this chapter, the study is conducted in an ACMI with three modules voltage scaled in {1:2:6}.

The procedure presented in the previous chapter to design the SCMI output filter is valid also for the ACMI. Therefore, the ACMI output inductance is given by (4.30).

$$L_{ACMI} = \frac{V_P{}^2 x_{(\%)}}{2P_{ACMI}\omega_0}\frac{1}{100} \tag{4.30}$$

4.9 Closed-Loop current control

The methodology presented in the previous chapter for designing the current controller is also valid for the ACMI, but adjusting the values on DC voltages to the ratio {1:2:6}.

Figure 4:22 presents the ACMI connected to the grid with closed-loop current control. The ACMI output current is sensed by means of a current sensor and the measured signal is sent to the control strategy block. The PCC voltage is measured in order to be used in a feedforward action.

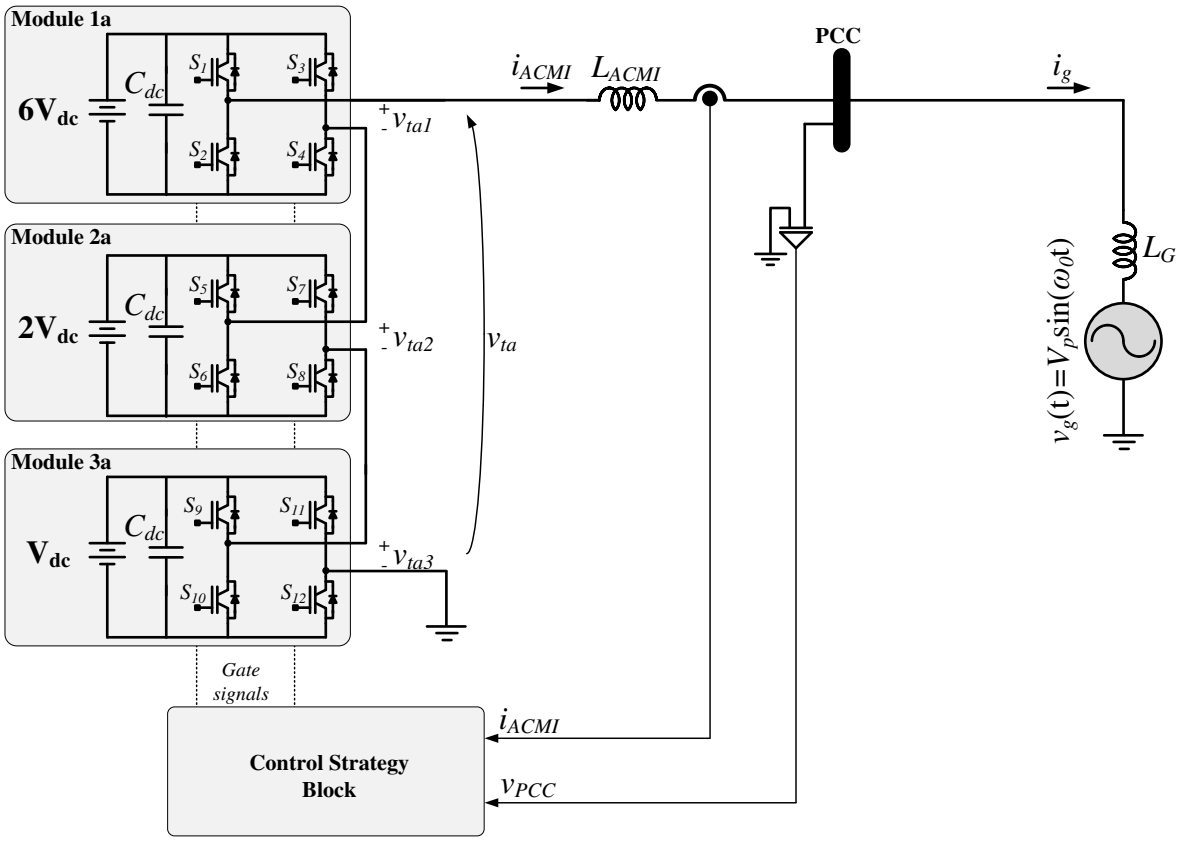


Figure 4:22 - The ACMI connected to the grid with closed-loop current control.

Figure 4:23 presents the control strategy block diagram. The measured current (i_{ACMI}) is subtracted from the current reference (i_{ACMI}*) and the resulting signal (e) is sent to the controller, which, in turn, acts in the ACMI through the modulated signal (u). A voltage feedforward (v_{PCC}) is added to the current controller output signal. The ACMI plus the output filter is represented by a current plant ($I_{ACMI}(s)$).

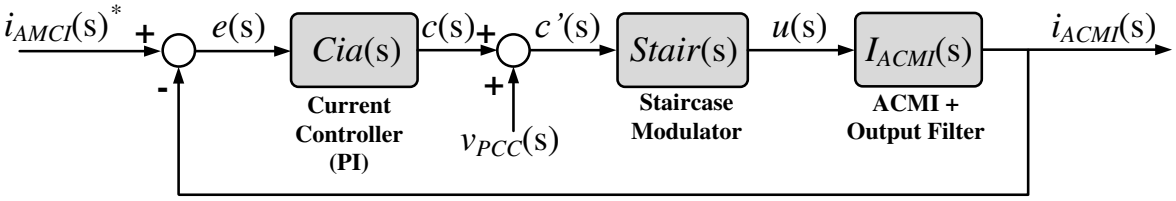


Figure 4:23 - Control strategy block diagram.

The ACMI plus output filter transfer function is given by (4.31).

$$\frac{I_{ACMI}(s)}{\lambda(s)} = \frac{(1+2+6)V_{dc}}{s(L_G + L_{ACMI})} \tag{4.31}$$

The PÌ controller transfer function is given by (4.32).

$$Cia(s) = \frac{\lambda(s)}{e(s)} = \frac{k_{pa}(sT_{PIa}+1)}{sT_{PIa}} \tag{4.32}$$

The closed-loop transfer function that relates the ACMI output filter and its reference, considering the PI controller, is given by (4.33).

$$\frac{I_{ACMI}(s)}{I_{ACMI}{}^{*}(s)} = \frac{(1+2+6)V_{dc}k_{pa}(sT_{PIa}+1)}{s^2T_{PI}(L_G+L_{INV})+s(1+2+6)V_{dc}k_{pa}T_{PIa}+(1+2+6)V_{dc}k_{pa}} \quad (4.33)$$

Neglecting the one-sampling delay [45], the damping factor is given by (4.34).

$$\xi_a = \frac{1}{2}\sqrt{\frac{(1+2+6)V_{dc}k_{pa}T_{PIa}}{L_G+L_{ACMI}}} \quad (4.34)$$

ξ =1 leads to a critically damping response and it is an attractive choice. Moreover, the time constant T_{PI} must be assigned to be much longer than the control delay from the view point of control stability [42]. By setting a value to the T_{PI}, the k_p is found.

4.10 Verifying the current controller

In order to verify the efficacy of the current controller, the ACMI was set to operate as active filter. Figure 4:24 presents the system used to verify the efficacy of the current controller. A nonlinear load made by a diode rectifier with LC filter at the DC-side was used as a source of harmonic currents.

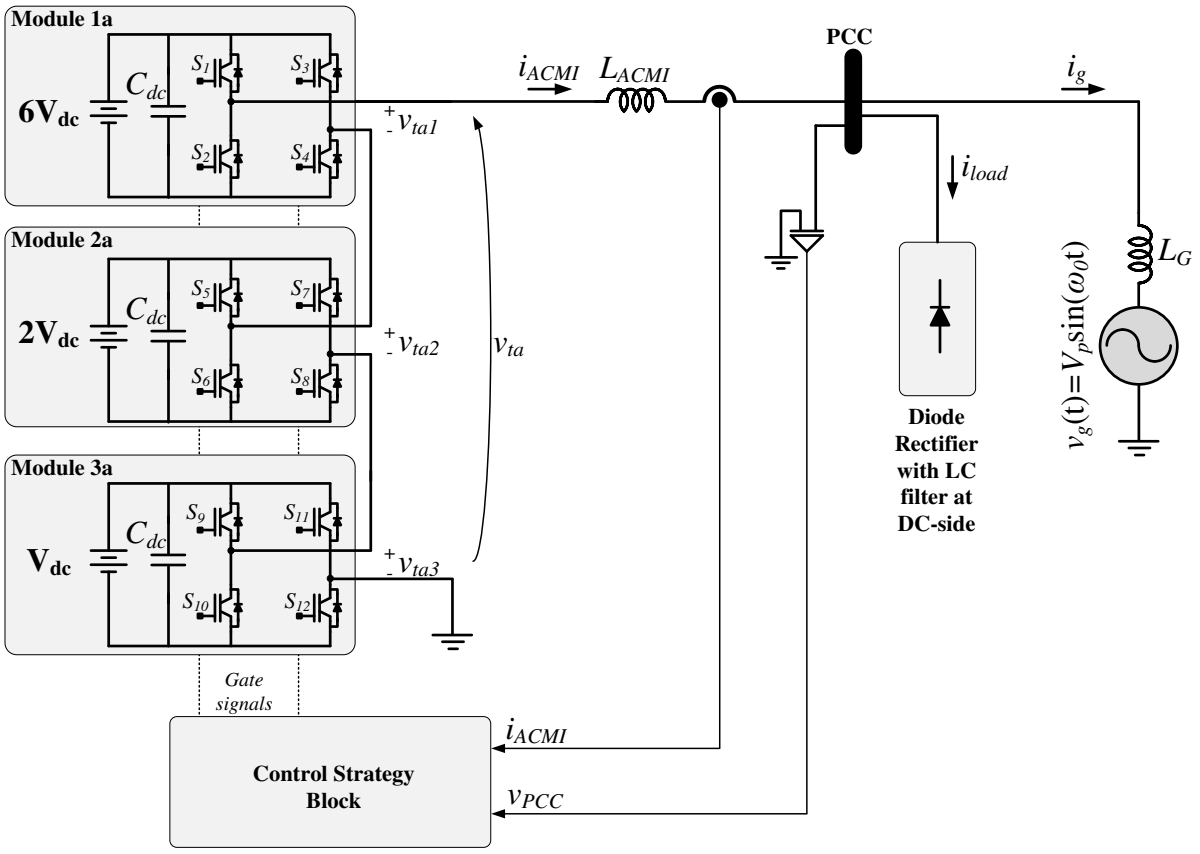


Figure 4:24 - System diagram used to verify the efficacy of the current controller.

The parameters used in the simulation and in the prototype are presented in Table 4:2

Table 4:2- Parameters used in the simulation and in the prototype.

Parameter	**Value**
Grid peak voltage	$V_p = 180$ V
Grid frequency	$f_g = 60$ Hz
Grid inductance	$L_G = 0.3$ mH
Inductance of the rectifier DC-side filter	$L_{rect} = 35$ mH
Capacitance of the rectifier DC-side filter	$C_{rect} = 470$ μF
Rectifier filter load	$R_{rect} = 95$ Ω
SCMI rated power	$P_{ACMI} = 500$ W
Percentage of the base impedance	x% = 5%
ACMI output inductance (according to (4.30)	$L_{ACMI} = 4.25$ mH
DC-link capacitors	$C_{dc} = 2800$ μF
Upper module DC voltage	$6V_{dc} = 144$ V
Middle module DC voltage	$2V_{dc} = 48$ V
Lower module DC voltage	$V_{dc} = 24$ V
Sampling frequency	$F_s = 30$ kHz
Damping factor	$\xi = 1$
PI time constant (adopted)	$T_{PI} = 15$ ms
PI proportional gain (according to (3.29)	$k_p = 0.00561728$

The designed PI was discretized through the same method presented in the previous chapter.

Figure 4:25 present the ACMI output current and its signal reference. Initially, the reference is sinusoidal. Later on, the reference is highly distorted. The designed current controller makes the ACMI output current to follow its reference in both sinusoidal and distorted cases.

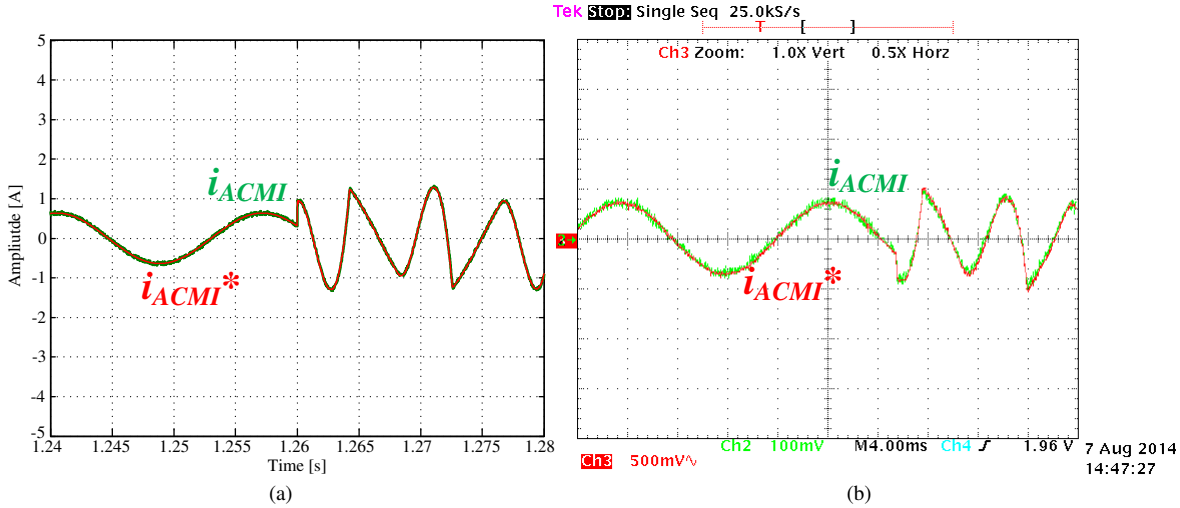


Figure 4:25 - The ACMI output current and its signal reference. (a) Simulation and (b) Experimental (Ch2: 0.1V/A).

Figure 4:26 presents the simulated error signal between the ACMI output current and its reference. A spike happens when the reference is changed.

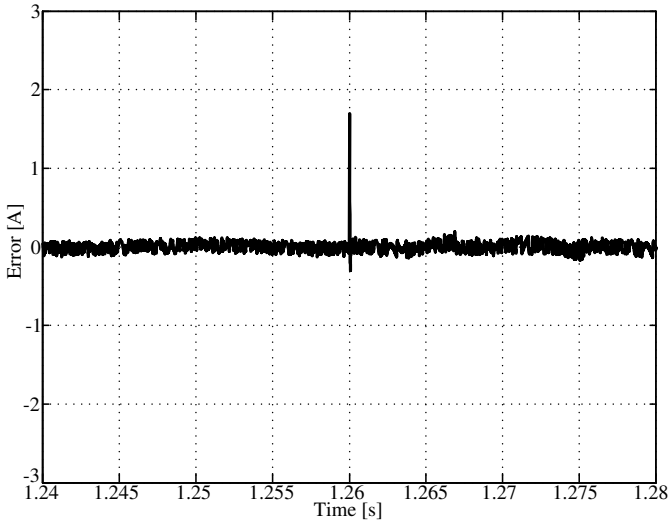


Figure 4:26 - Simulated error signal between the ACMI output current and its reference.

4.11 Influence of the controller proportional gain on the module terminal voltages

This section presents how the current controller proportional gain changes the module terminal voltages. Figure 4:27 presents the upper, middle and lower module terminal voltages, as well the ACMI terminal voltage. This result was collected for the same conditions presented in the previous section. All the voltages are according to the expected waveforms. The upper module switches at 60Hz.

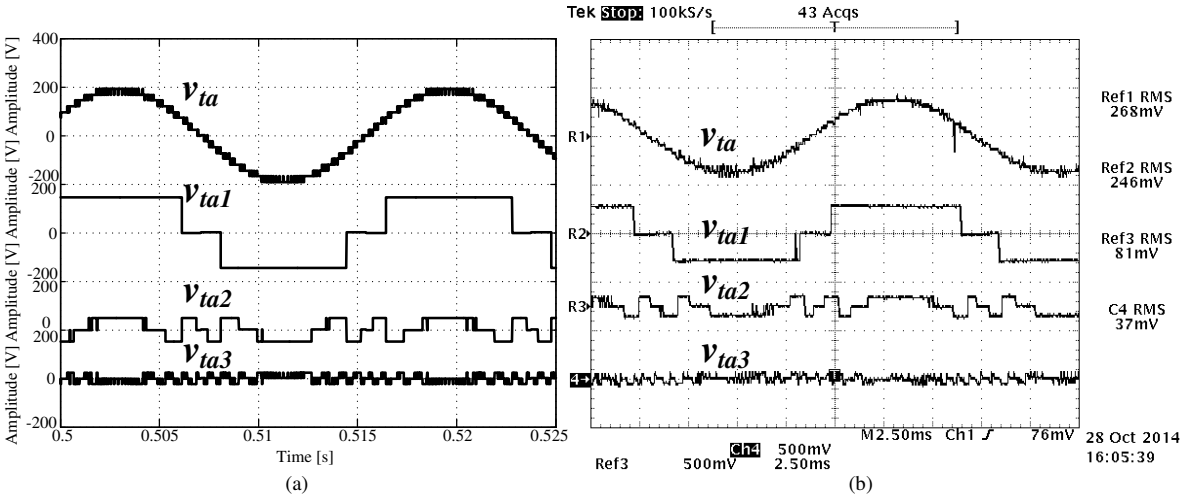


Figure 4:27 - The upper, middle and lower module terminal voltages, as well the ACMI terminal voltage. (a) Simulation and (b) Experimental (Ref1, Ref2, Ref3, Ch4: 0,5V/V).

If the proportional gain increases, the time response becomes faster and the controller increases the ability to compensate higher current di/dt. However, the module voltages present more commutations. Figure 4:28 presents the simulated terminal voltages for the case where the proportional gain has been increased. All the terminal voltages faced an increase in the number of commutation. Increasing the commutation on the upper module may invalidate the ACMI topology. Once the upper module switches at 60 Hz in a normal condition, the semiconductors can have low-speed technologies, such as IGCT. But several commutations in a short time may not be hold by these semiconductors. Therefore, the system dynamic requirements must be chosen carefully in order not to increase the number of commutation on the module voltages.

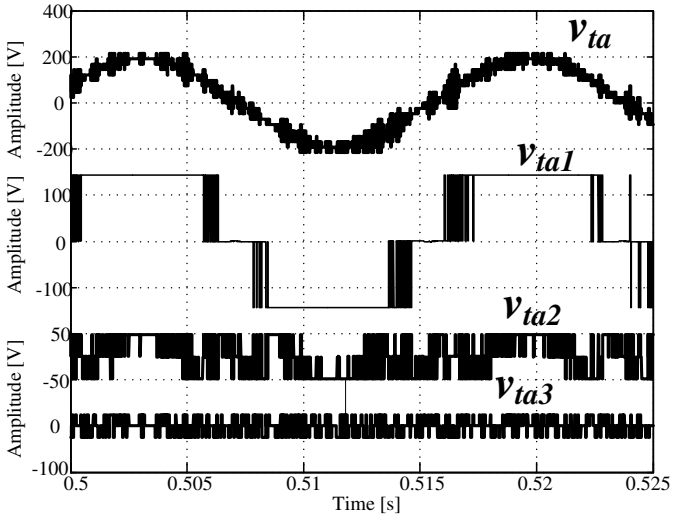


Figure 4:28 – Simulated terminal voltages for the case where the proportional gain has been increased by five.

4.12 Concerning DC-link voltage control

Controlling the DC-link voltages in ACMI is more complex than SCMI mainly due to two facts: there is active power in harmonic frequencies and the regenerative power behavior may lead the controller to a collapse. The first disappears when the ACMI is operating exclusively as STATCOM, once its current has only fundamental component. The collapse happens when the controller applies a temporarily modulation index with a value corresponding to the region of negative power processing, and this is valid for STATCOM and active filters applications. The controller may understand it as an action to increase/reduce the modulation index and its value leads to a deeper point on the referred region.

The active power across each module is given by (4.35).

$$p_{act(1,2,3)} = \frac{1}{T}\int_{t_0}^{t_0+T} \sum_{h=1}^{\infty} v_{ta(1,2,3)h}(t)\, i_{ACMIh}(t)\, dt \tag{4.35}$$

where h is the harmonic order.

Figure 4:29 presents the harmonic content for the upper module terminal voltage and for the ACMI output current. In this case, the ACMI was set to operate as active filter. The low frequency components are coincident. Therefore, active power will be processed on these frequencies.

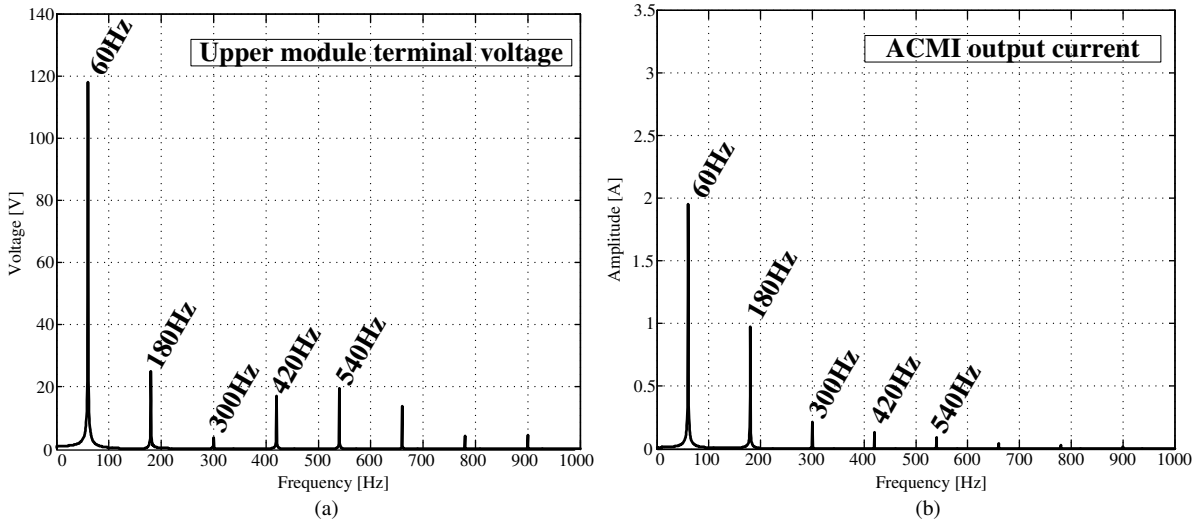


Figure 4:29 - The harmonic content for the upper module terminal voltage (a) and for the ACMI output current (b).

Some applications have been reported in the literature covering DC-link voltage control in ACMI [71]–[74]. The most of them use a resistor in parallel to the DC-link capacitor in order to burn the incoming energy from harmonic components.

4.13 Possibility of employment the ACMI as battery-based storage.

Section 4.6 showed the power distribution across the modules. Since the regions with positive power in all modules are limited, it is relevant to evaluate the possibility of employment the ACMI in battery-based storages. This is motivated mainly because the terminal voltage of the batteries varies according to its State-of-Charge (SOC). Such variation may lead the operation to an undesirable region. This section analyses the allowed variation in the battery terminal voltage. The scenarios are evaluated considering the values in Table 4:2. The following assumptions are applied:

i) Lead-acid and lithium-ion batteries were considered;
ii) The nominal voltage for the lead-acid batteries is 12V;
iii) The nominal voltage for the lithium-ion batteries is 3.6V;
iv) The terminal voltage can vary from 10.2V to 13.5V for lead-acid batteries;
v) The terminal voltage can vary from 3.4 to 3.9 for Lithium-Ion batteries;
vi) All battery terminal voltages in each scenario vary equally;
vii) The semiconductors are ideal;
viii) The ACMI is operating at nominal power.

The modulation index (m_a) is given by (4.36).

$$m_a = \frac{V_{ta1\_pk}}{\sum V_{dc}} \tag{4.36}$$

where (v_{ta1_pk}) is the ACMI terminal peak voltage at fundamental frequency.

Figure 4:30 presents a simplified diagram for the fundamental frequency of the ACMI connected to the grid.

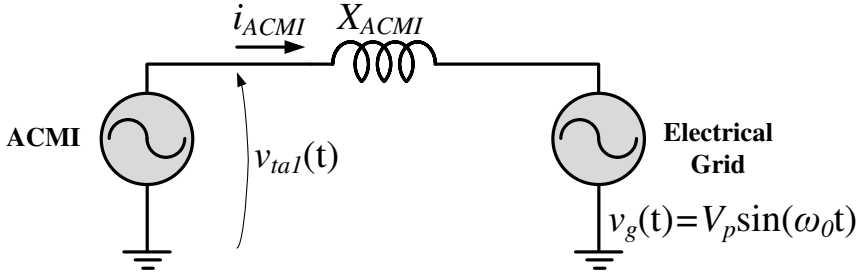


Figure 4:30 - Simplified diagram for the fundamental frequency of the ACMI connected to the grid.

Applying the Kirchhoff's voltage law, the ACMI terminal voltage is given by (4.37).

$$v_{ta}(t) = i_{ACMI}(t) X_{ACMI} + v_g(t) \tag{4.37}$$

The ACMI output RMS current is given by (4.38)

$$i_{ACMI\_RMS} = \frac{P_{ACMI}}{V_P / \sqrt{2}} \tag{4.38}$$

Therefore, the ACMI terminal peak voltage is given by (4.39).

$$V_{ta1\_pk} = \frac{2P_{ACMI}X_{ACMI}}{V_P} + V_P \tag{4.39}$$

4.13.1 Scenario 1: The ACMI with lithium-ion batteries, in {1:2:6} and connected to a 127 V grid

Each level of the output voltage corresponds to six series connected batteries. The V_{dc} voltage is 21.6V. Referring to Figure 4:18a, the region where all modules process positive power is m_a = [0.945 1.0]. The maximum allowed battery terminal voltage is given by (4.40).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_pk}}{6{\cdot}9m_a}\right|_{m_a=0.945} \tag{4.40}$$

$$\therefore V_{dc\_\max} = 3.70V \tag{4.41}$$

The minimum allowed battery terminal voltage is given by (4.54).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_pk}}{6{\cdot}9m_a}\right|_{m_a=1} \tag{4.42}$$

$$\therefore V_{dc\_\min} = 3.49V \tag{4.43}$$

The obtained interval for the battery terminal voltage is applicable. The operation fits the assumption (*v*). A BMS should be used to guarantee the operation within the obtained interval.

This scenario was simulated in order to verify its consistence. Figure 4:31 presents the power across the modules and the ACMI output current. All modules are processing positive power. The ACMI current is sinusoidal.

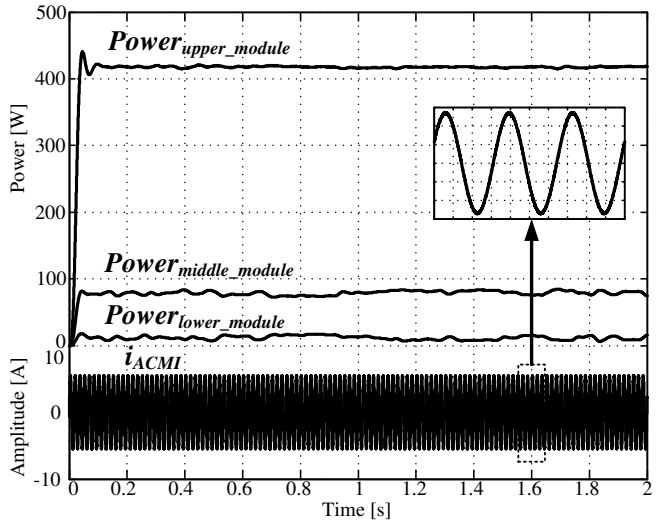


Figure 4:31 - Power across the modules and the ACMI output current.

4.13.2 Scenario 2: The ACMI with lead-acid batteries, in {1:3:9} connected to a 110 V grid

Now, each level corresponds to the voltage of one battery. The V_{dc} nominal voltage is 12V. The grid peak voltage is 155.56V and the ACMI terminal peak voltage is 165.85V.

The maximum allowed battery terminal voltage is given by (4.44)

$$V_{dc\_\max} = \left.\frac{V_{ta1\_pk}}{13m_a}\right|_{m_a=0.96} \tag{4.44}$$

$$\therefore V_{dc\_\max} = 13.29V \tag{4.45}$$

The minimum allowed battery terminal voltage is given by (4.46).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_\mathrm{pk}}}{13m_a}\right|_{m_a=1} \tag{4.46}$$

$$\therefore V_{dc\_\min} = 12.75V \tag{4.47}$$

The obtained interval fits the assumption (*iv*). However, the interval is close to the upper border.

4.13.3 Scenario 3: The ACMI with Lithium-ion-batteries, in {1:3:9} and connected to a 127 V grid

Each level corresponds to four series connected batteries. The V_{dc} voltage is 14.4V. The maximum allowed battery terminal voltage is given by (4.48).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_pk}}{4{\cdot}13m_a}\right|_{m_a=0.96} \tag{4.48}$$

$$\therefore V_{dc\_\max} = 3.78V \tag{4.49}$$

The minimum allowed battery terminal voltage is given by (4.50).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_pk}}{4{\cdot}13m_a}\right|_{m_a=1} \tag{4.50}$$

$$\therefore V_{dc\_\min} = 3.63V \tag{4.51}$$

The obtained range for the battery terminal voltage is also applicable.

4.13.4 Scenario 4: The ACMI with Lead-Acid batteries, in {1:3:9} and connected to a 127 V-grid

Each level corresponds to two series connected batteries. The V_{dc} voltage is 24V. The maximum allowed battery terminal voltage is given by (4.52).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_pk}}{2{\cdot}13m_a}\right|_{m_a=0.96} \tag{4.52}$$

$$\therefore V_{dc\_\max} = 7.57V \tag{4.53}$$

The minimum allowed battery terminal voltage is given by (4.54).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_pk}}{2{\cdot}13m_a}\right|_{m_a=1} \tag{4.54}$$

$$\therefore V_{dc\_\min} = 7.23V \tag{4.55}$$

The obtained range for the battery terminal voltage is impossible to be operated. Therefore, this scenario must be discarded.

4.13.5 Scenario 5: The ACMI with lead-acid batteries, in {1:2:6} and connected to a 127 V grid

Each level corresponds to two series connected batteries. The V_{dc} voltage is 24V. The maximum allowed battery terminal voltage is given by (4.52).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_pk}}{2{\cdot}9m_a}\right|_{m_a=0.945} \tag{4.56}$$

$$\therefore V_{dc\_\max} = 11.10V \tag{4.57}$$

The minimum allowed battery terminal voltage is given by (4.54).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_\mathrm{pk}}}{2{\cdot}9m_a}\right|_{m_a=1} \tag{4.58}$$

$$\therefore V_{dc\_\min} = 10.50V \tag{4.59}$$

The obtained interval is possible to be operated, but the operation is limited in short part of the SOC curve.

4.13.6 Scenario 6: The ACMI with lead-acid batteries, in {1:2:6} and connected to a 127 V grid with a sag profile

In this scenario the 127Vrms grid is under a sag profile. The grid is assumed to be in 114.3Vrms (10% lower than 127V). The V_{dc} voltage is 24V. The maximum allowed battery terminal voltage is given by (4.52).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_\mathrm{pk}}}{2{\cdot}9m_a}\right|_{m_a=0.945} \tag{4.60}$$

$$\therefore V_{dc\_\max} = 10.08V \tag{4.61}$$

The minimum allowed battery terminal voltage is given by (4.54).

$$V_{dc\_\min} = \left.\frac{V_{ta1\_\mathrm{pk}}}{2{\cdot}9m_a}\right|_{m_a=1} \tag{4.62}$$

$$\therefore V_{dc\_\min} = 9.53V \tag{4.63}$$

Comparing to the previous scenario, the range of operation worsens when the grid voltage presents sag profile.

4.13.7 Extending the operation region with lead-acid batteries

The analyzed scenarios demonstrated the possibility to use lithium-ion batteries in ACMI without taking care about the regenerative power. Nevertheless, for lead-acid batteries, the possibility is restricted. The obtained terminal voltage limits the operation in the SOC curve. Such limitation is undesirable and usually exhaustive to be obeyed. A method to extend the operation region in the SOC curve is discussed in this section.

The methodology consists in replacing the lower module to a high-frequency bidirectional module. The replacement makes the regenerative power, exclusively to this

module, be neglected in curve of Figure 4:18. In occurrence of regenerative power, the bidirectional module transfers the incoming power to the grid. Once the lower modules process around 4% of the total power, the new module can be switched with PWM at tens of kilohertz, reducing the passive elements used to filter the transferred power. In [70] the authors proposed a high-frequency module using a high-frequency transformer. The implantation of a high-frequency link is beyond the scope of this thesis.

By neglecting the lower module processed power in the analysis of scenario 5, the region with positive power becomes m_a = [0.78 1.0].

The maximum allowed battery terminal voltage passes to be given by (4.64).

$$V_{dc\_\max} = \left.\frac{V_{ta1\_\mathrm{pk}}}{2{\cdot}9m_a}\right|_{m_a=0.78} \tag{4.64}$$

$$\therefore V_{dc\_\max} = 13.45V \tag{4.65}$$

The minimum allowed battery terminal voltage keeps 10.5V. Such values are feasible to be performed. The terminal voltage of the battery may vary from 10.5 to 13.45V. The SOC curve is used on its totality. Therefore, the ACMI can be used in storages with lead-acid batteries.

4.14 AC Voltage Control

The ACMI may also be designed to operate in isolated grids, in voltage-control mode. This section presents the procedure to control the AC voltage.

4.14.1 Modifying the ACMI output filter

The ACMI output filter must have a capacitor to guarantee a controlled and stable AC voltage. The capacitor is designed in order not to change more than 3% of the current power factor. Then, the maximum allowed reactive power drained by the capacitor is given by (4.66).

$$Q_{ACM\,\mathrm{Im}ax} = \tan\left(\arccos(0.97)\right) P_{ACMI} \tag{4.66}$$

The maximum capacitance to guarantee (4.66) is given by (4.67).

$$C_{ACM\,\mathrm{Im}ax} = \frac{Q_{ACM\,\mathrm{Im}ax}}{V_{PCCrms}{}^2 \omega_0} \tag{4.67}$$

According to the parameters presented in
Table 4:1 the maximum capacitance is given by (4.68)

$$C_{ACM\,\mathrm{Im}ax} = 20.6uF \tag{4.68}$$

Since the maximum allowed values is known, the choice of the capacitance should satisfied the constraints presented in (4.69), where the resonance frequency must be within the interval of ten times higher than the grid frequency and lower than half of the switching frequency. There is no switching frequency in ACMI due to the staircase modulation. Nevertheless, for design purposes, the switching frequency is 5 kHz.

$$10 f_g < f_{res} < \frac{f_{sw}}{2} \tag{4.69}$$

The resonance frequency is given by (4.70).

$$f_{res} = \frac{1}{2\pi\sqrt{L_{ACMI} C_{ACMI}}} \tag{4.70}$$

The resonance frequency is chosen to be 2040 Hz (34th harmonic) and according to the parameters presented in

Table 4:1, the ACMI capacitance is given by (4.71).

$$C_{ACMI} = 1.36uF = 2x0.68nF \tag{4.71}$$

Figure 4:32 presents the ACMI with the designed LC filter. The capacitor is placed after the current sensor. Two distinguished ACMI currents are pointed out. One before the LC filter and another, after the LC filter.

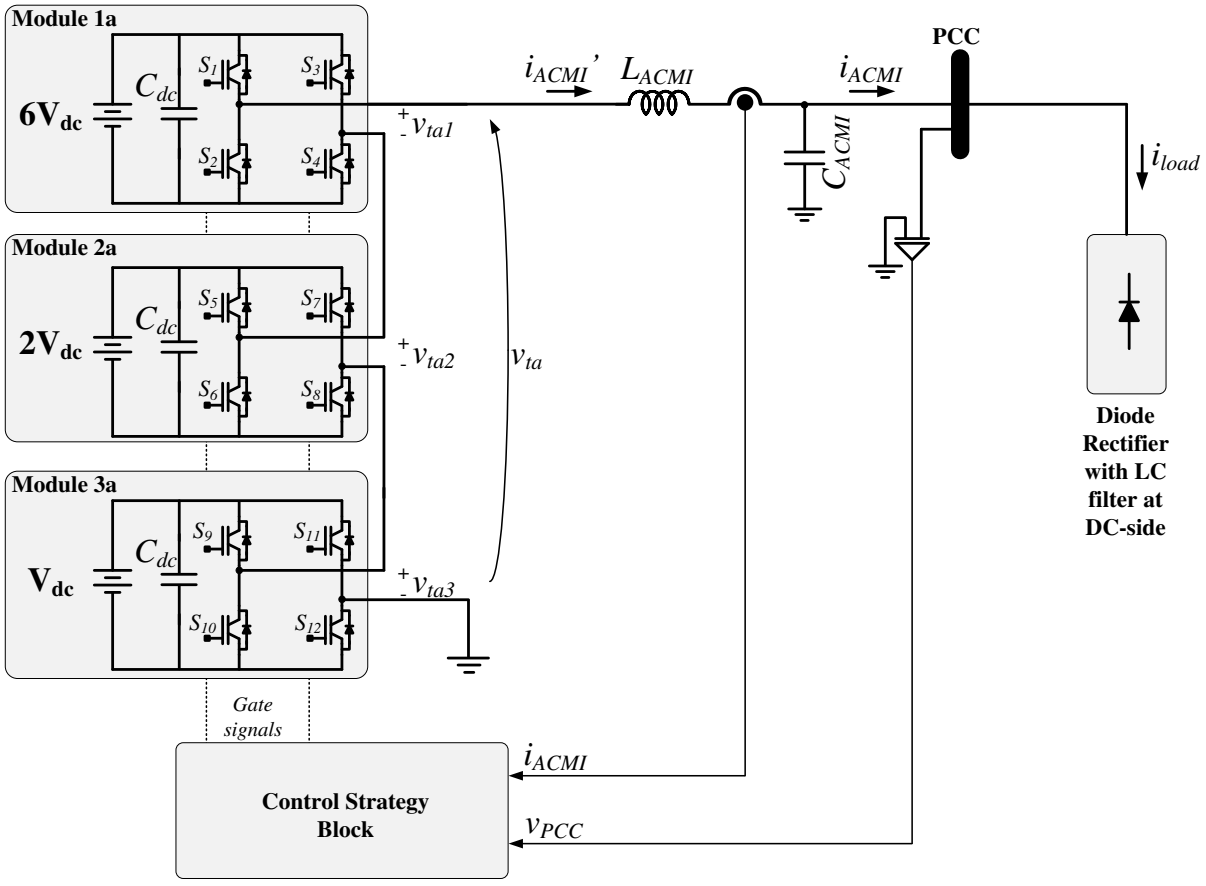


Figure 4:32 - The ACMI with the designed LC filter.

4.14.2 Closed-loop AC voltage control

Figure 4:33 presents a simplified block diagram for the control strategy. The measured PCC voltage is subtracted from the reference and the resulted signal is sent to the controller, which, in turn, acts in the ACMI through the staircase modulator.

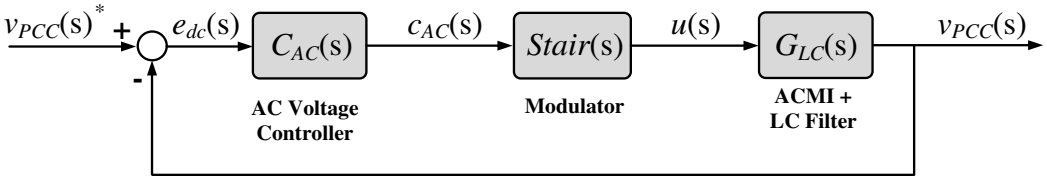


Figure 4:33 - A simplified block diagram of the control strategy.

The ACMI plus LC filter transfer function is given by (4.72).

$$G_{LC}(s) = \frac{(1+2+6)V_{dc}}{L_{ACMI}C_{ACMI}\left[s^2 + \frac{1}{R_L C_{ACMI}} + \frac{1}{L_{ACMI}C_{ACMI}}\right]} \tag{4.72}$$

4.14.3 Proportional-Resonant Controller

A Proportional-Resonant (PR) controller is used to control the PCC voltage. This section presents the procedure to design a PR controller made by an Infinite Impulse Response (IIR) filter. The resonant part is used to extract one harmonic component from a signal containing several components. Figure 4:34 presents a diagram of how the resonant part works. The tuned frequency (f_{nf}) is desired frequency. All other frequencies are attenuated (filtered).

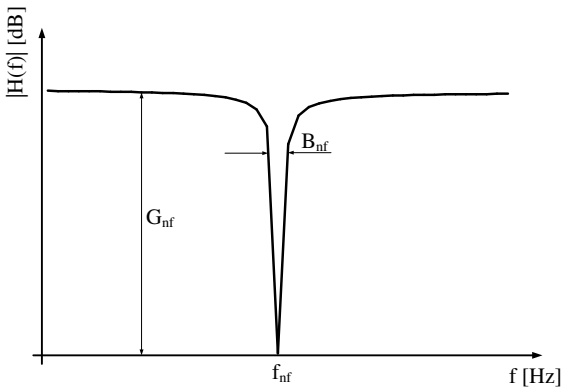


Figure 4:34 - Diagram of how the resonant part works.

The PCC voltage is controlled at 60 Hz. Therefore, the output of the resonant part is a sinusoidal waveform at 60 Hz. Figure 4:35 presents details of the resonant part.

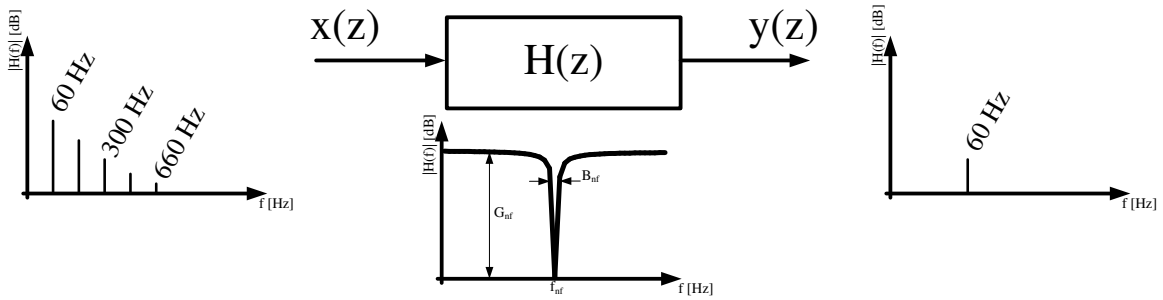


Figure 4:35 - Details of the resonant part.

The following section presents a step-by-step way to design the resonant part of the PR controller.

i) Defining the desired parameters

According to the Figure 4:34, three parameters must be defined. They are: the tuned frequency in Hz (f_{nf}), the bandwidth of the PR in Hz (B_{nf}) and the gain in real values (G_{nf}). The bandwidth is the thickness of the signal around the tuned frequency. A good choice is any value around 1% of the tuned frequency. The gain is preferentially chosen as one in order not to lose information from the input signal.

ii) The transfer function of the resonant part

The transfer function of the resonant part is given by (4.73) [75].

$$H(z) = \frac{y(z)}{x(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{4.73}$$

Or in a recursive way as (4.74).

$$y(n) = \left[b_0 x(n) + b_1 x(n-1) + b_2 x(n-2)\right] - \left[a_0 x(n) + a_1 x(n-1) + a_2 x(n-2)\right] \tag{4.74}$$

where n is the current sample.

The next step is to obtain the resonant part coefficients based on the parameters given in step 1.

iii) Obtaining the coefficients

The coefficients are obtaining by discretizing an analog resonant filter by means of the Z-transformation.

A constant C_t is defined as (4.75).

$$C_t = \frac{G_{nf} {B_{nf}}^2}{2\sqrt{{\omega_{nf}}^2 - 0.25{B_{nf}}^2}} e^{-0.5 B_{nf} T_a} \sin\left(T_a \sqrt{{\omega_{nf}}^2 - 0.25{B_{nf}}^2}\right) \tag{4.75}$$

The b_0 coefficient is given by (4.76).

$$b_0 = G_{nf} B_{nf} T_a \tag{4.76}$$

The b_1 coefficient is given by (4.77).

$$b_1 = T_a\left[(-1)G_{nf}B_{nf}e^{-0.5B_{nf}T_a}\cos\left(T_a\sqrt{\omega_{nf}{}^2 - 0.25B_{nf}{}^2}\right) - C_t\right] \quad (4.77)$$

The b_2 coefficient is null.

$$b_2 = 0.00000 \quad (4.78)$$

The a_0 coefficient is one.

$$a_0 = 1.00000 \quad (4.79)$$

The a_1 coefficient is given by (4.80).

$$a_1 = (-1)2e^{-0.5B_{nf}T_a}\cos\left(T_a\sqrt{\omega_{nf}{}^2 - 0.25B_{nf}{}^2}\right) \quad (4.80)$$

The a_2 coefficient is given by (4.81).

$$a_2 = e^{-B_{nf}T_a} \quad (4.81)$$

The proportional gain is added to (4.73) and may be tuned to guarantee minimum steady-state error.

4.14.4 LC passive damping

The use of a PR controller requires a damping in the LC filter in order not to avoid its natural resonance. The damping can be passive or active. The passive solution is a resistance series connected to the capacitor of the LC filter. Its value must be the same to the capacitive reactance at the resonance frequency, given by (4.82) [40].

$$R_{damp} = X_{cACMI\_fres} = \frac{1}{2\pi f_{res}C_{ACMI}} \quad (4.82)$$

4.14.5 Results for ACMI with PR controller

The parameters used in the simulation and in the prototype are presented in Table 4:3.

Table 4:3- Parameters used in the simulation and in the prototype.

Parameter	**Value**
Resonance frequency	f_{nf} = 60 Hz
Resonance bandwidth	B_{nf} = 1.59 Hz
Resonance gain	G_{nf} = 1
b0 coefficient	b_0 = 3.330088212805e-4
b1 coefficient	b_1 = 3.329825312222e-4
b2 coefficient	b_2 = 0

a0 coefficient	$a_0 = 1.000000000000$
a1 coefficient	$a_1 = -1.999509161318$
a2 coefficient	$a_2 = 0.99966704662$
Damping resistor	$R_{damp} = 15\ \Omega$

Figure 4:36 present the PCC voltage and its reference in a reference step. The PCC voltage follows its reference without steady-state error, showing the efficacy of the designed PR. This result was collected with no load connected to the ACMI.

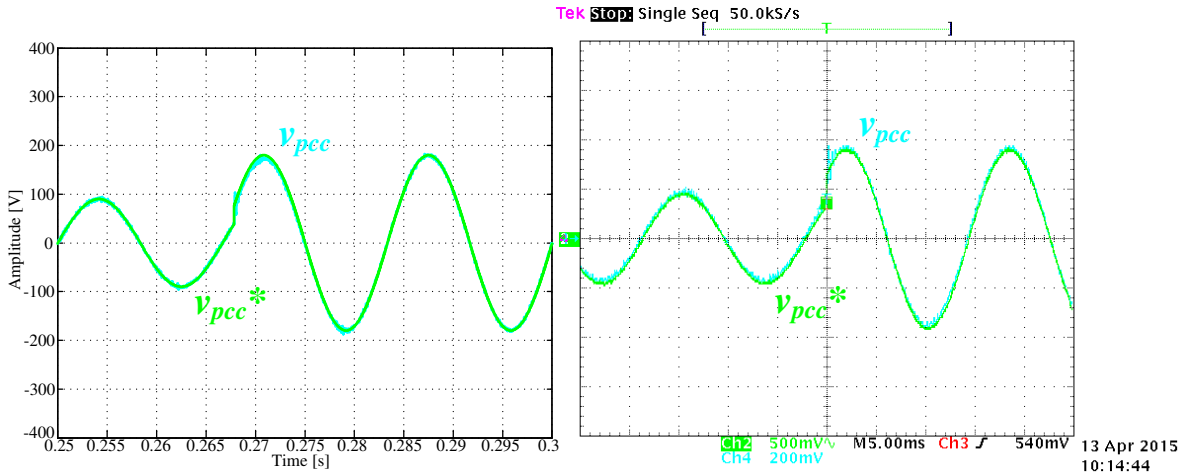


Figure 4:36 - The PCC voltage and its reference in a reference step. (a) Simulation and (b) Experimental.

Figure 4:37 presents the simulated error signal between the PCC voltage and its reference. A negative spike happens when the reference has its value changed. The error comes back to the steady-state value rapidly.

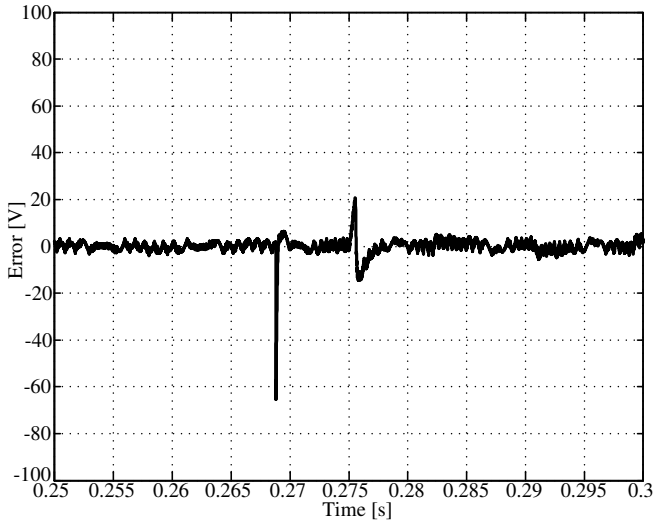


Figure 4:37 - Simulated error signal between the PCC voltage and its reference.

Figure 4:38 presents the PCC voltage and the ACMI current before and after the LC. The PCC voltage is sinusoidal and no distortions appear due to the distorted current. The current before and after the LC filter are very close, indicating that the designed passive damping has negligible influence on the ACMI processed power.

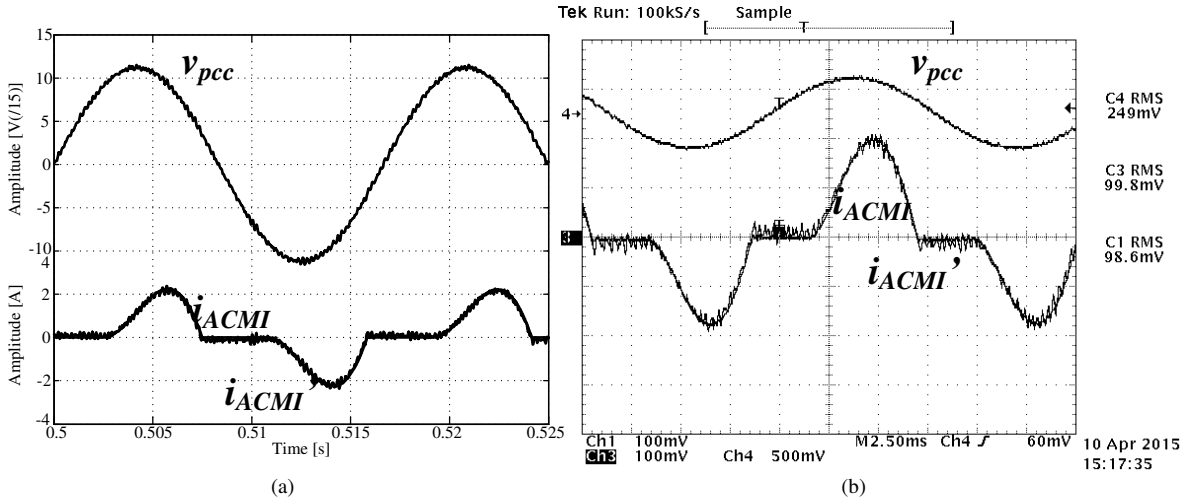


Figure 4:38 - The PCC voltage and the ACMI current before and after the LC filter. (a) Simulation and (b) Experimental (Ch4: 0.5V/V; Ch1, Ch3: 0.1V/A).

Figure 4:39 present the ACMI terminal voltage, the upper module terminal voltage, the PCC and the ACMI current.

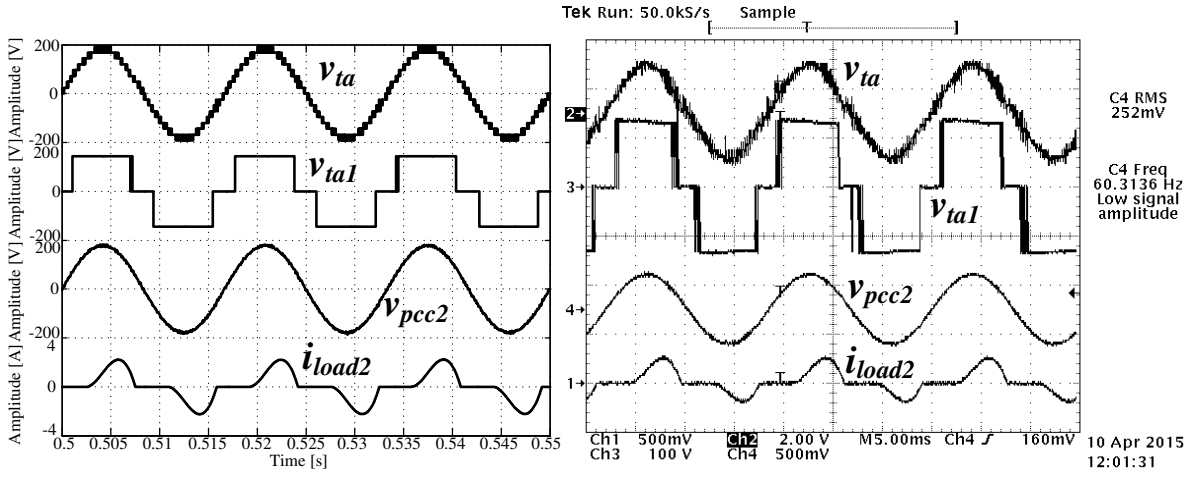


Figure 4:39 - The ACMI terminal voltage, the upper module terminal voltage, the PCC and the ACMI current. (a) Simulation and (b) Experimental (Ch4, Ch2: 0.5V/V; Ch1: 0.1V/A).

4.14.6 PI controller with feedforward action

An alternative to control the AC voltage is to use a PI controller with feedforward action of the load current. One advantage of this method is that the damping structure is not need. However, the load current must be measured. In a scenario with several loads, all load currents must be measured. Figure 4:40 presents a simplified diagram of the control strategy

with a PI controller. The current control loop is an inner loop of this strategy. The feedforward of the load current is added after the AC voltage controller.

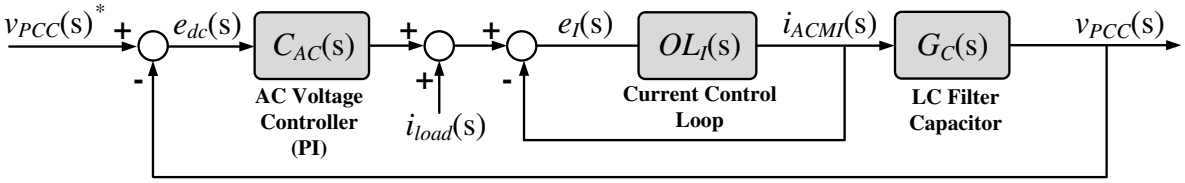


Figure 4:40 - Simplified diagram of the control strategy with PI controllers.

Once the inductor of the LC filter is considered within the current control loop, the dynamic behavior of the voltage loop is dictated by the capacitor of the LC filter [42]. The transfer function of the LC filter capacitor is given by (4.83).

$$G_C(s) = \frac{1}{sC_{ACMI}} \tag{4.83}$$

For tuning the PI, the load current can be considered as disturbance. The closed-loop transfer function can be written as (4.84).

$$\frac{i_{ACMI}{}^*(s)}{i_{ACMI}(s)} = \frac{1}{\tau_i s + 1} \tag{4.84}$$

where τ_i is the time constant of the closed-loop current control.

The AC voltage controller transfer function is given by (4.85).

$$C_{AC}(s) = k_{AC}\frac{s + z_{AC}}{s} \tag{4.85}$$

The voltage open-loop transfer function is given by (4.86).

$$OL_{AC}(s) = \frac{k_{AC}}{\tau_i C_{ACMI}}\left(\frac{s + z_{AC}}{s + \tau_i^{-1}}\right)\frac{1}{s^2} \tag{4.86}$$

At low frequencies, the phase of the open-loop transfer function tends to -180° due to the double pole at origin.

When an open-loop has double pole at the origin and one real, the symmetrical method [76] may be applied for tuning the PI parameters. The desired phase-margin δ_{AC} is given by (4.87)

$$\delta_{AC} = \sin^{-1}\left(\frac{1 - \tau_i z_{AC}}{1 + \tau_i z_{AC}}\right) \tag{4.87}$$

The cut-off frequency is given by (4.88).

$$\omega_c = \sqrt{z_{AC}\tau_i^{-1}} \tag{4.88}$$

The proportional gain is given by (4.89).

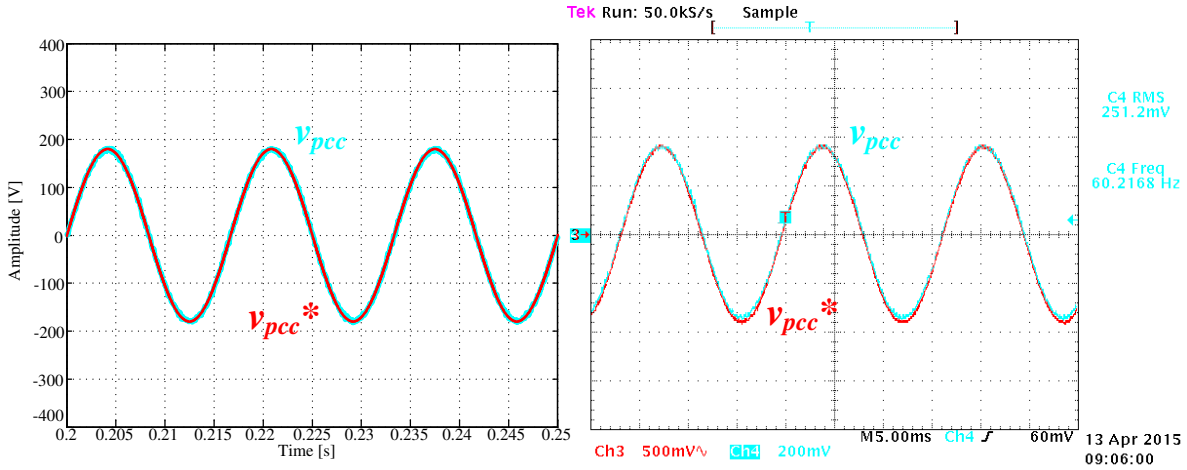
$$k_{AC} = C_{ACMI}\omega_c \tag{4.89}$$

The parameters of the designed controller are presented in Table 4:4.

Table 4:4 - Parameters of the designed controller.

Parameter	**Value**
Time constant of the current control loop (Table 4:2)	τ_i = 15 ms
Desired phase margin	δ_{AC} = 60°
PI zero (4.87)	z_{AC} = 4.78 Hz
Cut-off frequency (4.88)	ω_c = 15.469 Hz
PI proportional gain (4.89)	k_{AC} = 0.021

Figure 4:41 presents the PCC voltage and its reference signal without load. The PCC voltage follows its reference without error, showing the efficacy of the designed PI controller.



(a) (b)

Figure 4:41 - PCC voltage and its reference signal without load. (a) Simulation and (b) Experimental.

Figure 4:42 presents the ACMI terminal voltage, the upper module terminal voltage, the PCC voltage and the load current. The control strategy with PI controller does not change the ACMI features. Moreover, there are no distortions in the PCC voltage when a nonlinear load is connected to the ACMI.

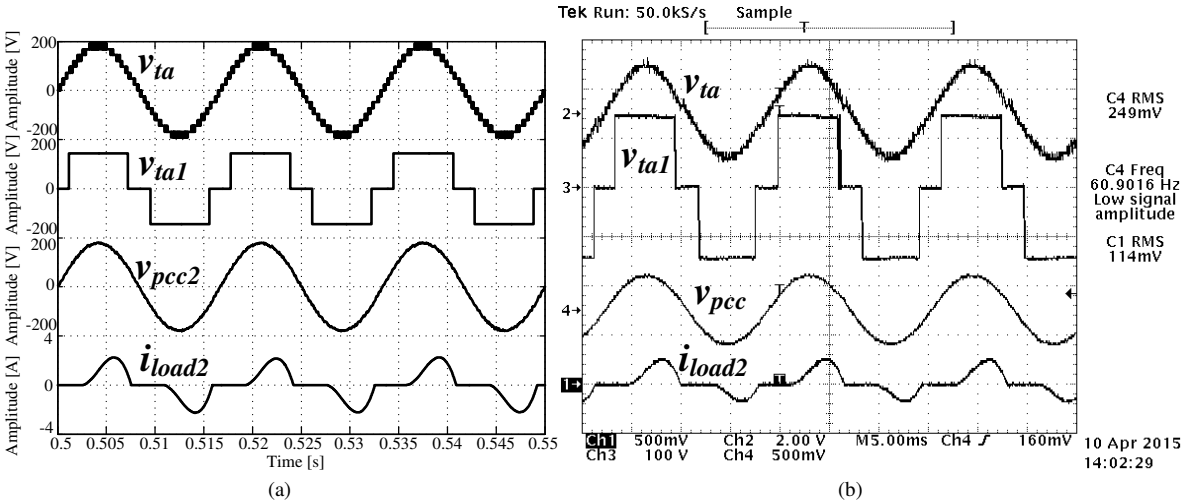


Figure 4:42 - ACMI terminal voltage, the upper module terminal voltage, the PCC voltage and the load current. (a) Simulation and (b) Experimental (Ch4, Ch2: 0.5V/V; Ch1: 0.1V/A)..

4.15 ACMI prototype

Figure 4:43 presents the prototype of the ACMI used in this chapter.

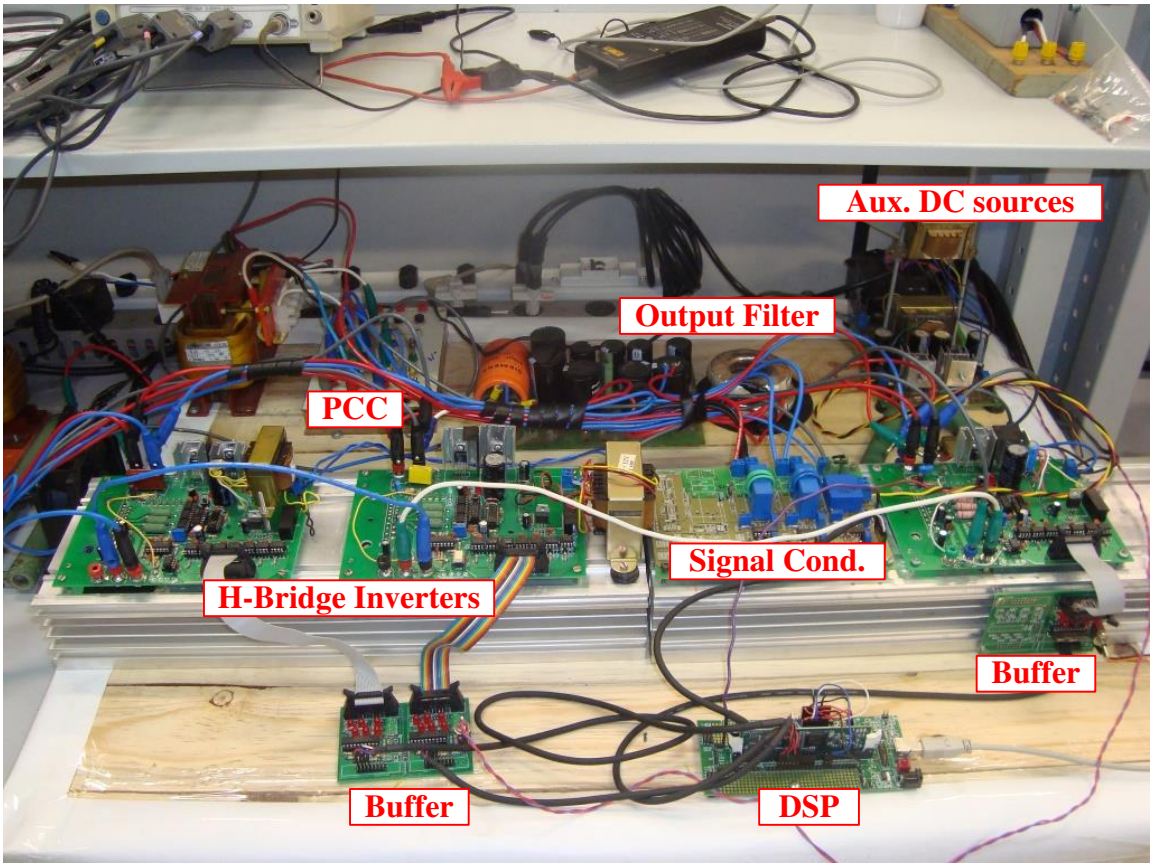


Figure 4:43 - The prototype of the ACMI used in this chapter.

4.16 Three-phase ACMI

This section presents the three-phase ACMI and an operation as active filter [77]–[79]. The studies described previously are extended to three-phase. The prototype used in this

section belongs to the project “Active Power Filter for More Electrical Airplane Variable Frequency Systems, 2013” from the University of Campinas – UNICAMP. The results were collected by applying the studies presented in this chapter.

Figure 4:44 presents the three-phase ACMI with three-modules each phase. The module voltages are scaled in {1:3:9}. The terminal voltages v_{a3}, v_{b3} and v_{c3} are referred to the ground.

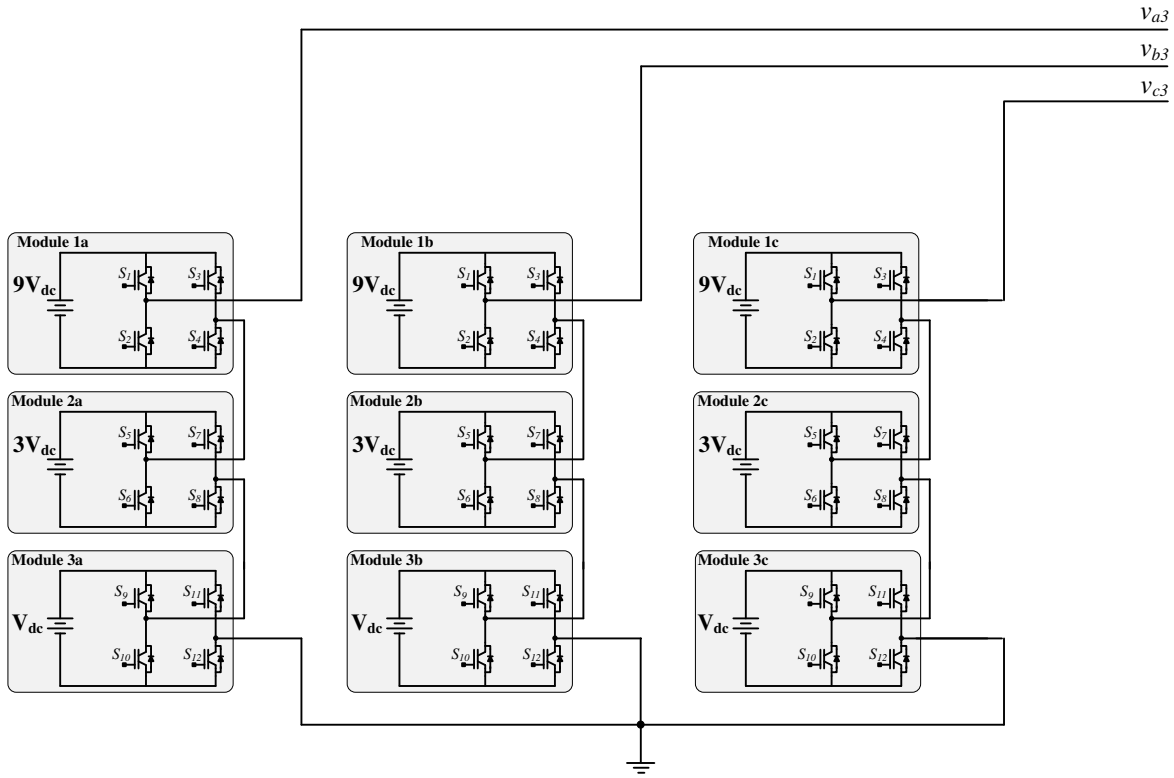


Figure 4:44 – Three-phase ACMI with three-modules each phase.

Figure 4:45 presents the three-phase voltage related to the ground. Each phase-to-ground voltage contains 27 levels. The voltage THD obtained in the simulation is 2.6%.

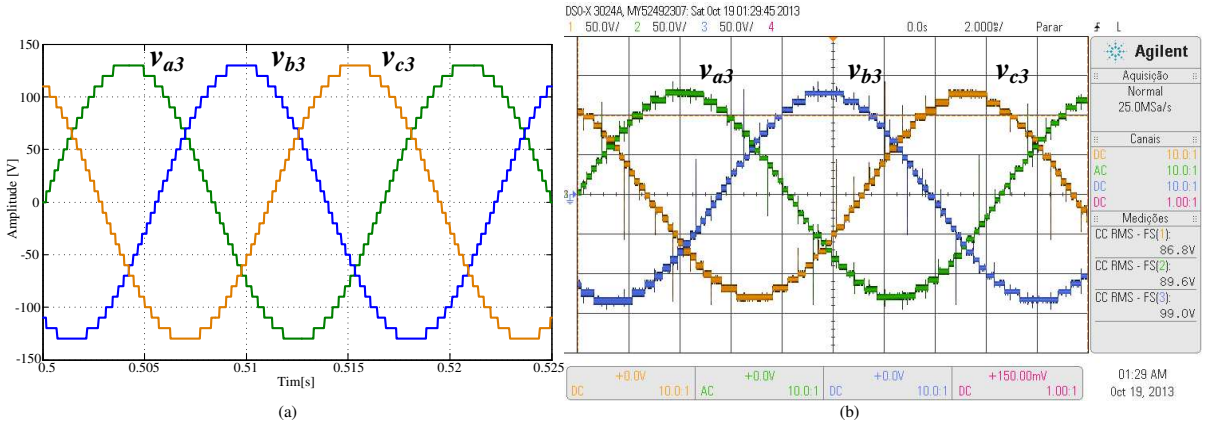


Figure 4:45 - ACMI three-phase voltage related to the ground.

The three-phase ACMI operating as active filter was evaluated. Figure 4:46 presents the three-phase ACMI connected to a grid. A nonlinear load made by three-phase diode rectifier with LC filter at the DC side is connected at PCC.

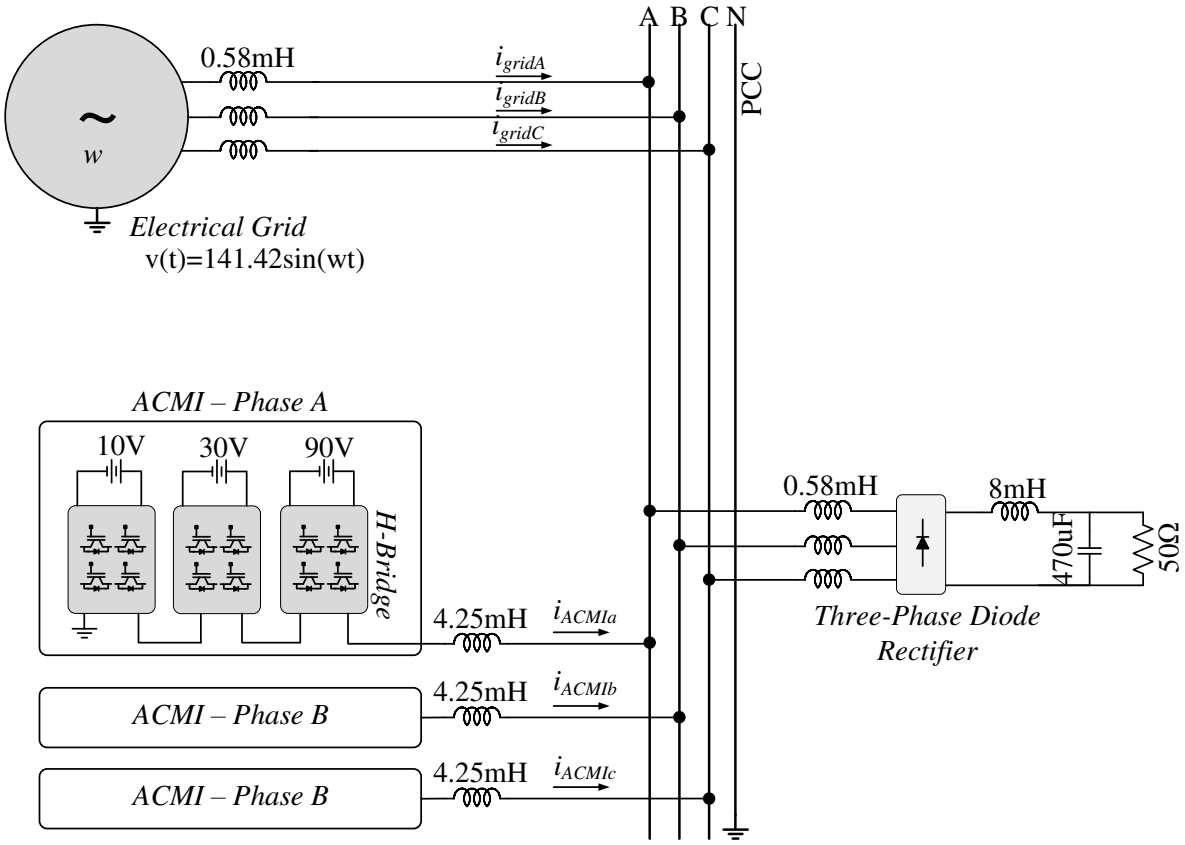


Figure 4:46 - Three-phase ACMI operating as active filter was evaluated.

Figure 4:47 presents the three-phase grid current and the ACMI current for phase A. At t = 0.2515s the ACMI begins to operate as active filter. Before that, the grid current is the distorted load current. As soon as the ACMI begins to operate, the grid current becomes sinusoidal.

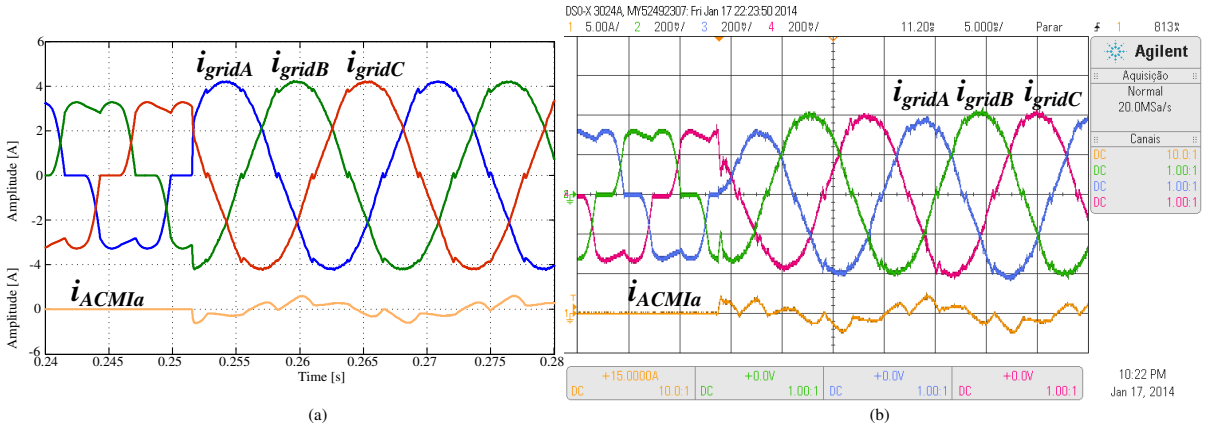


Figure 4:47 -Three-phase grid current and the ACMI current for phase A.

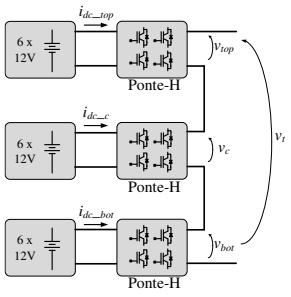
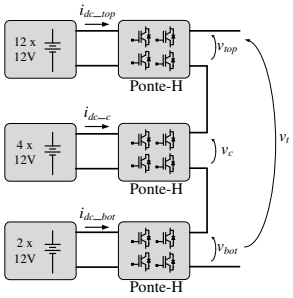
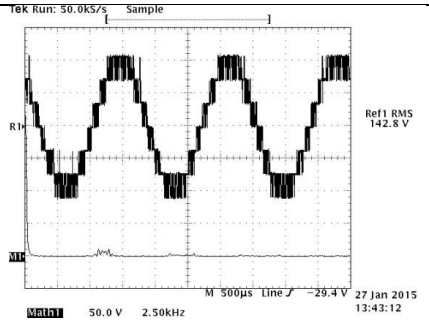
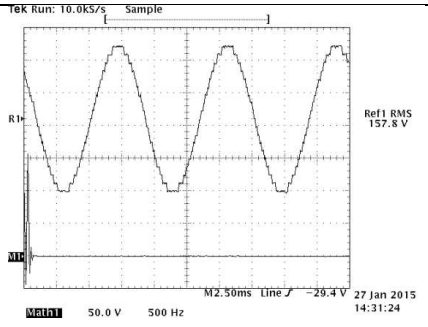
5 SUMMARIZING THE FEATURES FOUND IN SCMI AND ACMI

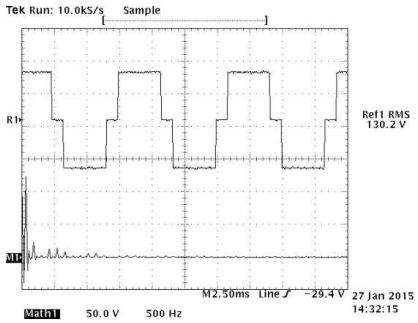
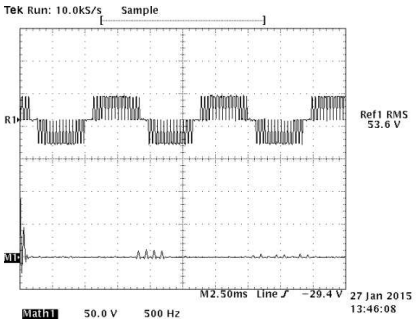
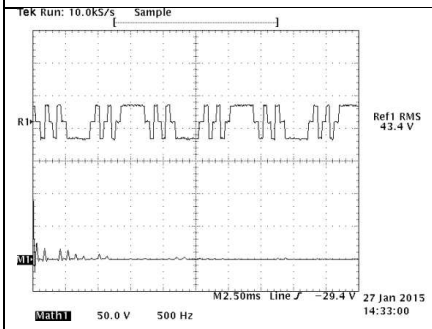
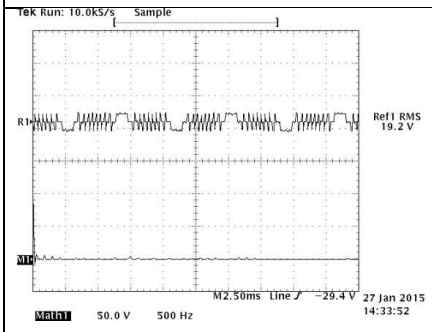
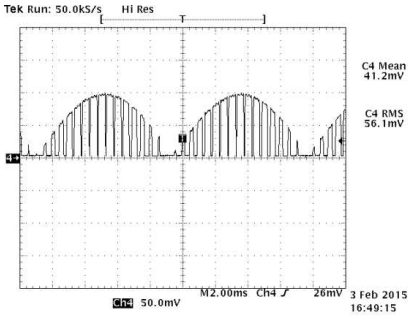
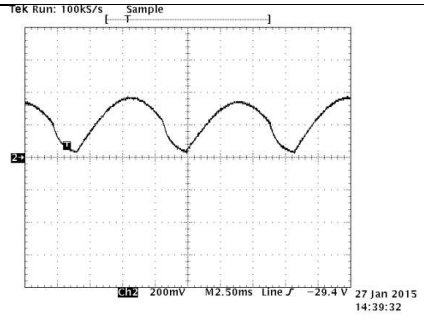
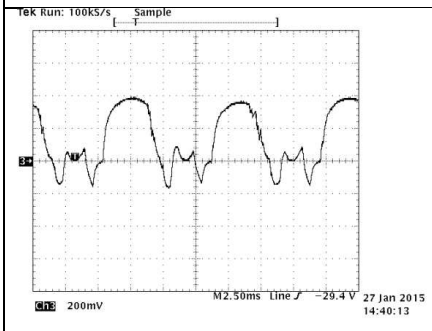
This chapter summarizes the features found in SCMI and ACMI with three modules. Additionally, a short comparison is presented. The objective is not to rank the topologies, but only show their feature side-by-side.

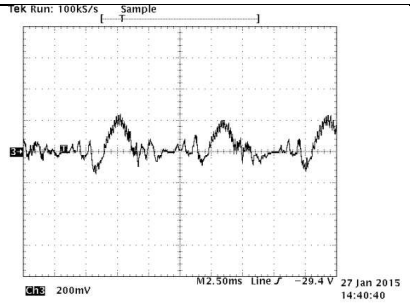
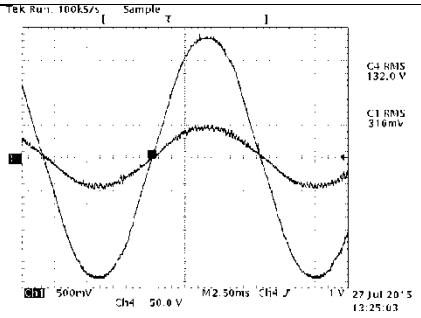
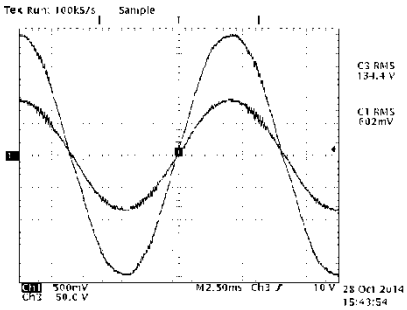
The SCMI and ACMI topologies have similar features. The terminal voltage is close to a sinusoidal waveform. The output filter has reduced volume. The way how the topologies processes the power depends on the modulation. Usually, the SCMI is modulated by PWM while the ACMI by staircase. The first makes a balanced distribution of the power across the modules. The second, the division of the power into the modules is not linear and depends on the modulation index. Even though the nonlinear power distribution, the ACMI topology can be used in storage system with lithium-ion batteries without the need of modifying the physical structure. It is not worth to use more than three modules in ACMI. The main reason is because the voltage THD is just slightly reduced.

Board 5:1 presents the features found in SCMI and ACMI topologies as well as some comments.

Board 5:1 – Features found in SCMI and ACMI topologies with three modules.

Quantity	SCMI	ACMI	Comments
Topology			
Terminal Voltage and its spectrum			Seven levels in SCMI and 19 in ACMI. Spectrum around 6 kHz in SCMI while in ACMI the harmonic spectrum is negligible.

Upper module terminal voltage and its spectrum			The same waveform for the three modules in SCMI. In SCMI, the spectrum is the fundamental plus switching components. In ACMI, the switching frequency is 60 Hz. There are low frequency components.
Middle module terminal voltage and its spectrum			Similarly, low frequency components on ACMI middle module terminal voltage.
Lower module terminal voltage and its spectrum			In ACMI, the RMS voltage in the lower module is low, compared to the terminal voltage. This may justify the employment of a high-frequency DC-link.
DC-link current in the upper module			The same waveform for SCMI. The current is pulsating. In ACMI, the current is continuous (due to the capacitor).
DC-link current in the middle module			In ACMI, negative values.

DC-link current in the lower module			Similarly, negative values in the DC-link current..
Synchronized output current			Both SCMI and ACMI output current are sinusoidal and in-phase related to the PCC voltage.

6 PROPOSAL OF AN INTERACTIVE BATTERY-BASED STORAGE SYSTEM

This chapter proposes an Interactive Battery-Based Storage System (IBBS). The interaction means the capability of the IBBS to operate coordinately to local and centralized controllers and to perform ancillary functions. Moreover, the IBBS in conjunction to other interactive distributor power elements result in a synergist operation of the grid. Concepts about smart-grids are also presented in order to clarify how the interaction contributes to the smart-grid realization.

The proposal is verified through a BBS built in an ACMI with three modules voltage scaled in {1:2:6} due to its fast dynamic behavior and its high quality waveforms. Nevertheless, the proposal can be employed to any other BBS topology[1].

6.1 The interactive battery-based storage in an intelligent distribution system

Figure 6:1 presents a simplified diagram of the IBBS connected to an intelligent distribution system. The distribution system is called throughout this thesis as smart micro-grid. The IBBS contains eighteen 12V/7Ah lead-acid batteries shared in three banks. The smart micro-grid is single-phase and it has the main generation, two feeders, two PCCs and central and local controllers. Each PCC has a nonlinear load. PCC2 has also a single-phase squirrel-cage induction motor. Initially, the switch S_1 is opened. The IBBS is connected to the PCC2 and a DG emulator is connected to the PCC1. The DG emulator and the IBBS have their own DSP. A local management controller is made between the IBBS and the DG emulator. The DSP of the IBBS holds the local controller. The variables used in the control strategy and in the controllers are represented by small arrows. The communication is made through the Serial Peripheral Interface (SPI) [80].

[1] It is assumed that the BBS based on other topologies are capable to make its output current to follow the reference signal without steady-state error. Additionally, some output filters, like the LCL, may change the manner how the system responds transitorily.

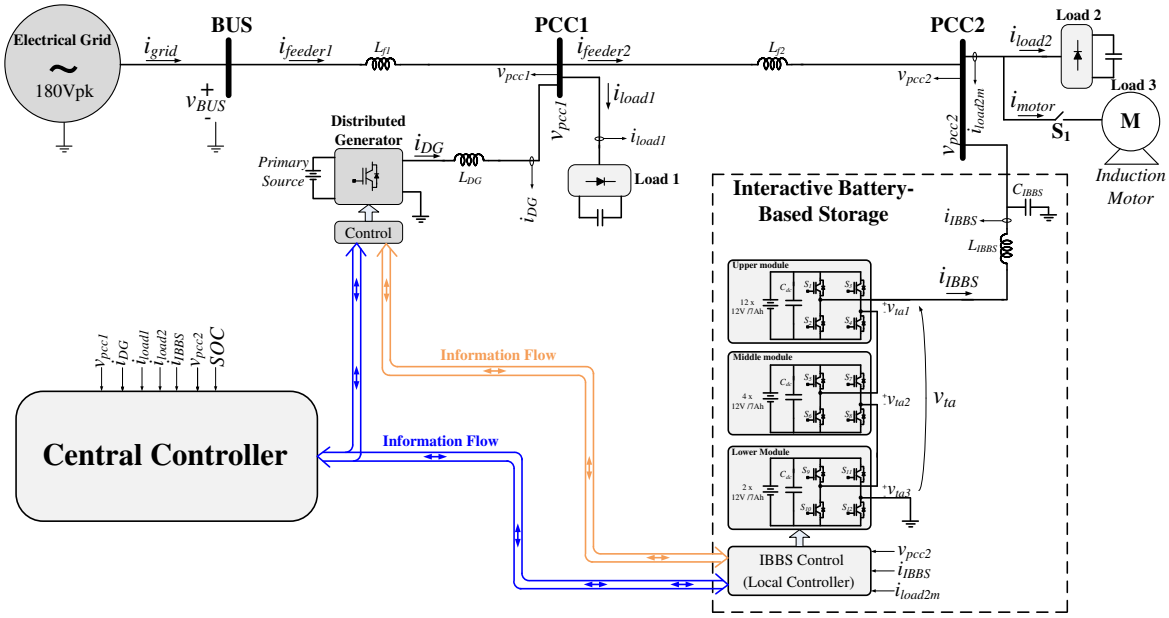


Figure 6:1 - Simplified diagram of the IBBS connected to a smart micro-grid.

The parameters used in the simulation and in the prototype are presented in Table 6:1.

Table 6:1 - Parameters used in the simulation and in the prototype.

Parameter	**Value**
Grid peak voltage	$V_p = 180$ V
Grid frequency	$f_g = 60$ Hz
Feeder 1 inductance	$L_{f1} = 0.3$ mH
Feeder 2 inductance	$L_{f2} = 0.15$ mH
DG nominal power	$S_{DG} = 1$ kVA
DG inductance	$L_{DG} = 4.25$ mH
IBBS nominal power	$S_{IBBS} = 500$ VA
Load 1: Inductance of the rectifier DC-side filter	$L_{rect1} = 35$ mH
Load 1: Capacitance of the rectifier DC-side filter	$C_{rect1} = 470$ µF
Load 1: Rectifier filter load	$R_{rect1} = 95$ Ω
Load 2: Inductance of the rectifier DC-side filter	$L_{rect2} = 35$ mH
Load 2: Capacitance of the rectifier DC-side filter	$C_{rect2} = 470$ µF
Load 2: Rectifier filter load	$R_{rect2} = 200$ Ω
Load 3: Induction motor apparent power	$S_m = 100$ VA
Percentage of the base impedance	x% = 5%
Sampling frequency	$F_s = 30$ kHz

6.2 The Phased-Locked Loop

The PLL is responsible for guaranteeing the synchronization between the current reference and the PCC voltage. The synchronization is required when the IBBS in injecting active power or charging the batteries. The PLL is based on vector algebra [81] and it makes use of the orthogonality concepts for phase detection. Such concepts bring more flexibility to track the frequency and allow working with distorted voltages.

Figure 6:2 presents a simplified block diagram of the PLL. The principle is to synthesize an orthogonal unitary sinusoidal function ($u_{\perp}$) related to the PCC2 voltage. The result (*dp*) of the internal product between the synthesized function and the PCC2 voltage must converge to a null average value. The instantaneous argument (θ) is obtained by the PI controller output variable (ω), which, in turn supplies a constant output value. A feedforward reference (ω_n) is included in order to improve the dynamic response. An adaptive moving average filter is used to compute the internal product average value. Since the IBBS control strategy is developed in a digital environment, a block related to the sampling delay is included, which is called in the diagram as Delay Function.

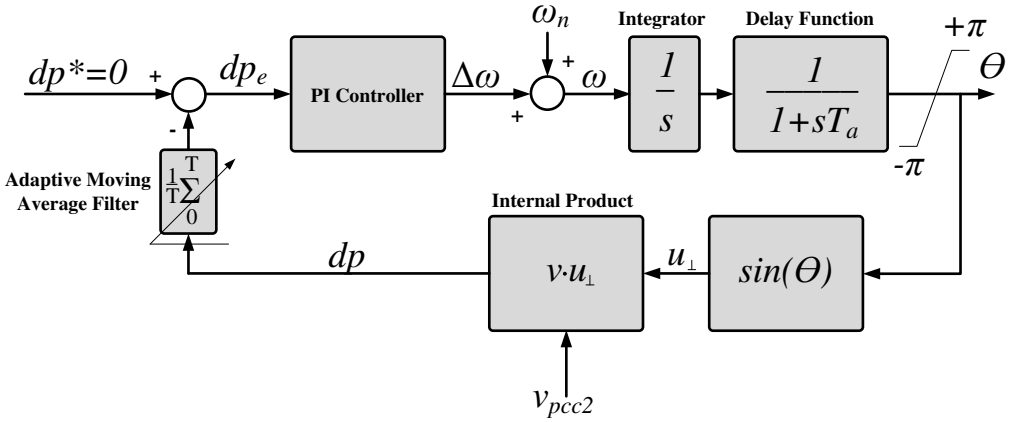


Figure 6:2 - A simplified block diagram of the PLL used in the IBBS.

The internal product of two instantaneous *n*-sized vectors is the sum of term-by-term product of their elements, as given by (6.1).

$$v \cdot u \equiv [v_1 \; v_2 \; \ldots \; v_n][u_1 \; u_2 \; \ldots \; u_n] = v_1u_1 + v_2u_2 + \ldots + v_nu_n \tag{6.1}$$

Two non-null vectors are orthogonal under the interval [t_1 t_2] if (6.2) is satisfied.

$$v \perp u \Leftrightarrow \int_{t_1}^{t_2} w(t)\left[v(t)u(t)\right]dt = 0 \tag{6.2}$$

where *w(t)* is a weighing function slightly positive. If this function is given by (6.3), then the average value of the internal product of two orthogonal vectors is null, as showed in (6.4).

$$w(t) = \frac{1}{t_2 - t_1} \tag{6.3}$$

$$\therefore \overline{v \cdot u_{\perp}} \equiv \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \left[v(t) u(t) \right] dt = 0 \tag{6.4}$$

Digitally, the equation (6.4) is given by (6.5).

$$\overline{v \cdot u_{\perp}}(k) = \frac{1}{m\Delta} \sum_{i=1}^{m} \left[v(k - i\Delta) u(k - i\Delta) \right] = 0 \tag{6.5}$$

where Δ is the sampling interval, m is the number of samples in a period, k is the sampling counter and i is the circular counter.

When the IBBS is set to inject active power into the PCC2 with unit power factor, valid for non-distorted voltage, seen from the PCC2, its current reference is given by (6.6).

$$i_{IBBS\_inj}{}^{*}(t) = I_{IBBSinj} \sin\left(\theta(t) + \pi/2 \right) \tag{6.6}$$

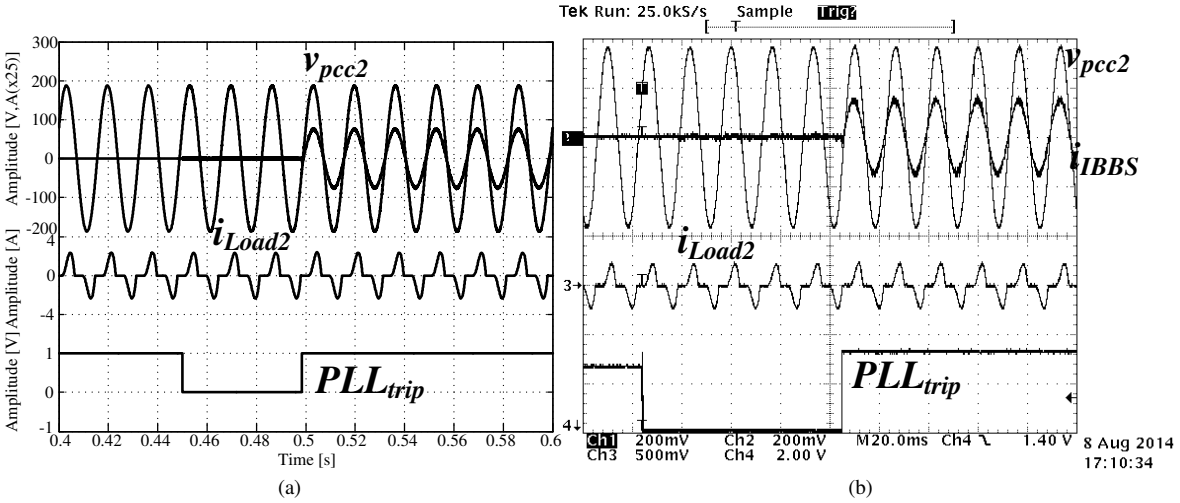
where θ is the PCC2 voltage angle, supplied by the PLL. The term $I_{IBBSinj}$ is supplied by the central controller and it is limited to the IBBS power rate.

When the IBBS is set to charge the batteries with unit power factor, seen from PCC2, its current reference is given by (6.7). The reference faced an 180° phase displacement.

$$i_{IBBS\_char}{}^{*}(t) = I_{IBBSchar} \sin\left(\theta(t) + \pi/2 + \pi \right) \tag{6.7}$$

The two above current references can be added to other references.

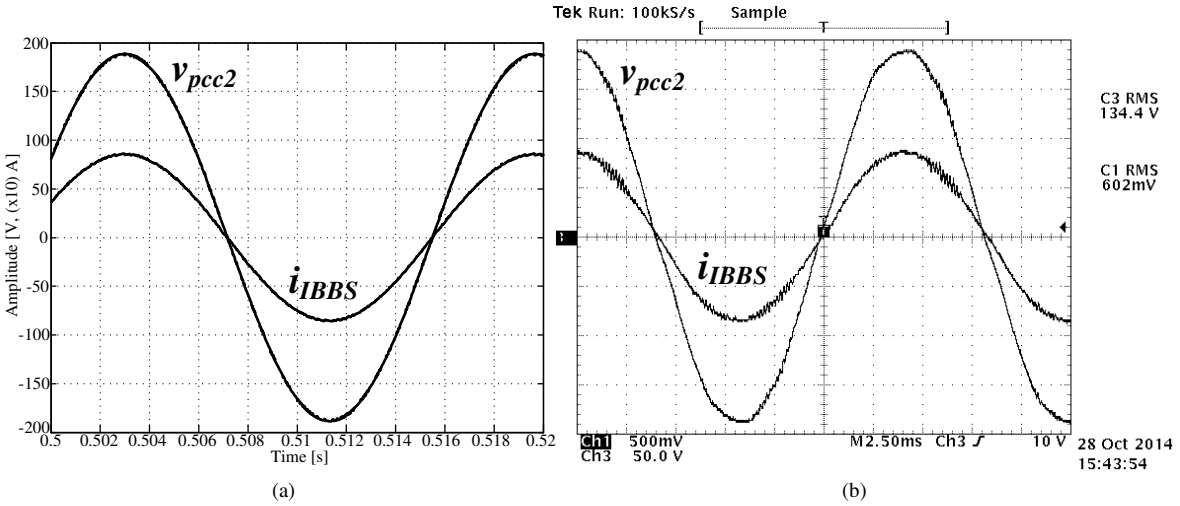
Figure 6:3 presents the results for the moment when the IBBS is connected to the PCC2. The falling-edge in the PLL trip signal represents the moment when the IBBS is connected. Once the PCC2 voltage angle is unknown, the IBBS waits the PLL to synchronize the current reference with the PCC2 voltage. The synchronization is achieved when the PLL error is lower than 2%. Once achieved (rising-edge), the IBBS injects active power into the grid with sinusoidal current. There is no phase displacement between the voltage and current. The load current is kept unchanged and no unpredictable behavior has occurred on the measured variables. Two important points: (i) this section also represent the IBBS in stand-by mode. The IBBS is operating with null current reference, between the PLL trip edges. (ii) the IBBS waits the PLL to synchronize only on the first connection to the PCC. After that, the IBBS begins to inject active power with unit power factor instantaneously when demanded.



(a) (b)

Figure 6:3 - Results for the moment where the IBBS is connected to the PCC2. (a) Simulation and (b) Experimental (Ch2: 0.5V/V; Ch1, Ch3: 0.1V/A).

Figure 6:4 presents the PCC2 and IBBS current in steady-state condition.



(a) (b)

Figure 6:4 - The PCC2 and IBBS current in steady-state condition. (a) Simulation and (b) Experimental (Ch1: 0.1V/A).

Figure 6:5 presents results for transition between charging and discharging process, both with unit power factor seen from the PCC2. The transition is made by changing the IBBS current reference from (6.6) to (6.7). Initially, the IBBS current is in-phase with PCC2. After the transition, it is in counter-phase. The load current does not notice the transition and no severe transitory has occurred. Moreover, the presented transition shows a bi-directionality capability of the IBBS.

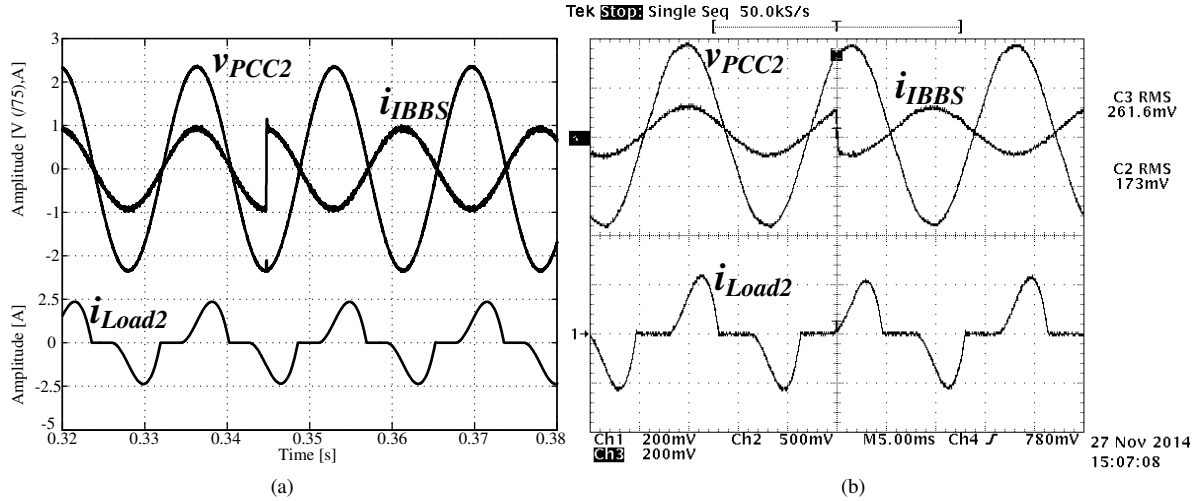


Figure 6:5 - Results for transition between charging and discharging process. (a) Simulation and (b) Experimental (Ch3: 0.5V/V; Ch1, Ch2: 0.1V/A).

6.3 Technical impacts of the IBBS on the grid

The IBBS is considered a DG when active power is injected into the grid. This section presents a case study showing how DGs impact technically on a power system. The impacts are more evident when bulk power is handled. The case study evaluates the power losses and voltage profile quantities. Figure 6:6 presents a fictitious distribution system. The system contains the main generation, 11 bar, linear and nonlinear loads and the IBBS connected at the bar 9.

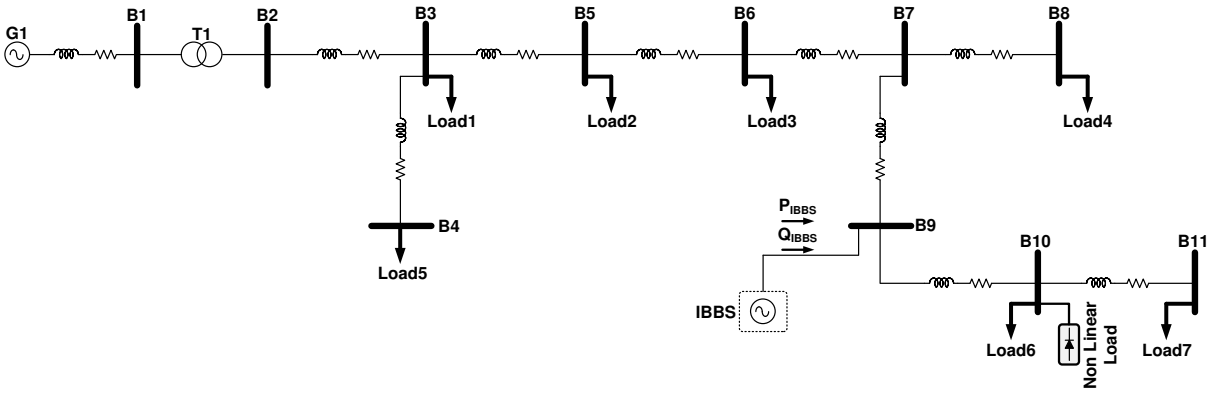


Figure 6:6 - Fictitious distribution system.

The case study begins evaluating the impact on the power losses along the system due to the connection of the IBBS at bar 9. The IBBS is considered ideal and its nominal power is 150 kW. The results were collected in steady-state conditions. Figure 6:7 presents the power losses through the feeders for phase A according to the amount of active power the IBBS is injecting. The IBBS is operating with unity power factor. Initially (at $P_{IBBS} = 0$), the IBBS is not injecting power and the power losses are 1242 W. As the IBBS injects more active power, the losses begin to reduce. The lower point is the moment where the circulating

current has its lower value. However, for values higher than 110 kW, the losses begin to be higher than the case with no IBBS. This phenomena occurs mainly due to the fact the IBBS is injecting more active power than that required by the loads.

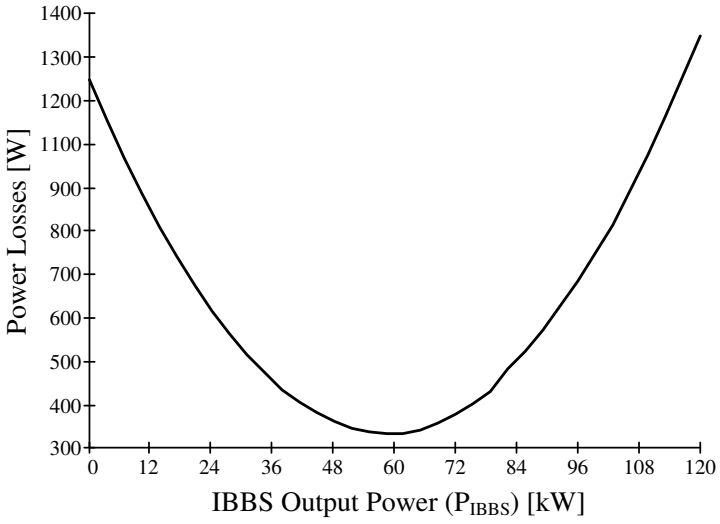


Figure 6:7 - Power losses through the feeder for phase A according to the amount of active power the IBBS is injecting.

Now the case study leads to the evaluation of the voltage profile. Figure 6:8 presents the voltage profile in all bars for different injected power values. With no IBBS, it is possible to notice all bars have voltage below the nominal value. As the amount of injected power rises, the voltage profile also rises.

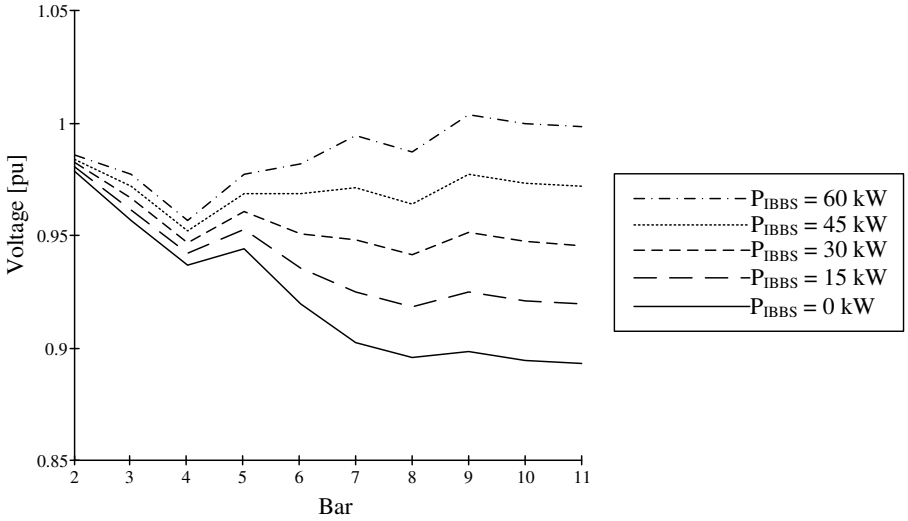


Figure 6:8 - Voltage profile in all bars against the injected power.

The amount of power injected affects the voltage profile [82]. Therefore, it is possible to take advantage of this capability in order to use the IBBS as a voltage regulator. Another way to regulate the voltage is to inject reactive power concomitantly. The technique to inject or consume reactive power in order to regulate the voltage profile is the principle of

operation of a STATCOM. Figure 6:9 presents the voltage profile in all bars for values of reactive power injection. This study is performed keeping the active power equal to 35 kW.

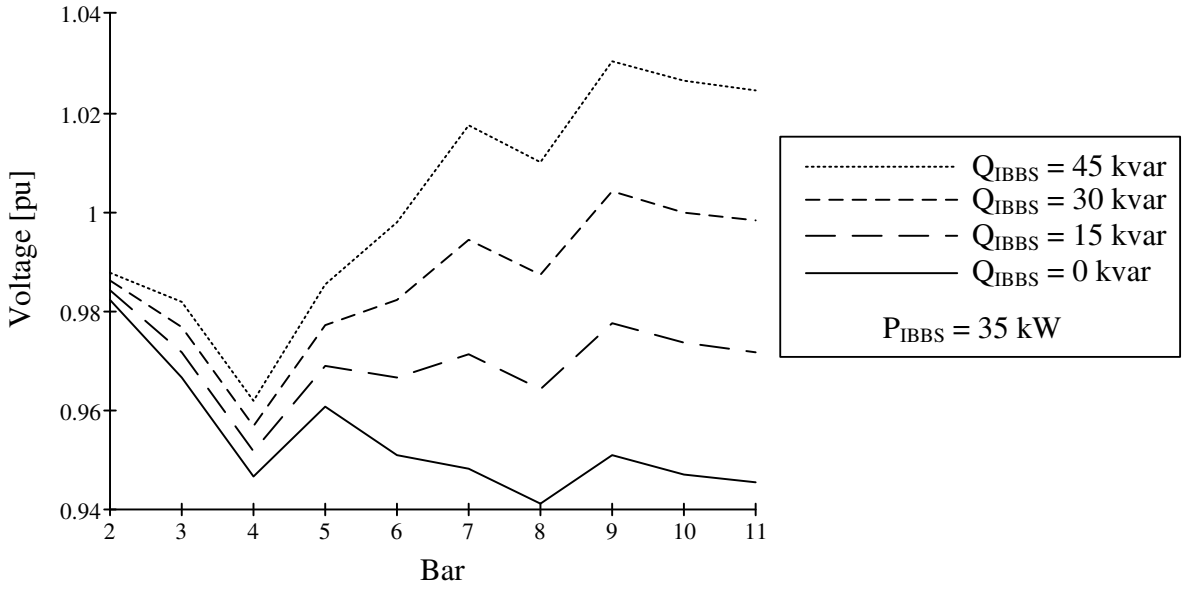


Figure 6:9 - The voltage profile in all bars for some values of reactive power injection.

Likewise, the IBBS can be used to reduce a bar voltage by consuming reactive power. The connection of the IBBS into the system may also change the power factor, the voltage and current THD, the unbalance, and so on [83].

6.4 System standardization

The DG penetration affects quantities in the electric system. In order to avoid causing damage or improper operation, there are some standards which suggest recommendations to be followed for safe connection of new DGs. As the design and behavior of the transmission and distribution levels are different, there are different constraints for each level. Figure 6:10 presents a simplified diagram of the system levels and the applied standardization. Bulk power and distribution systems have specific standardization while in the transmission level there is a conflict [84].

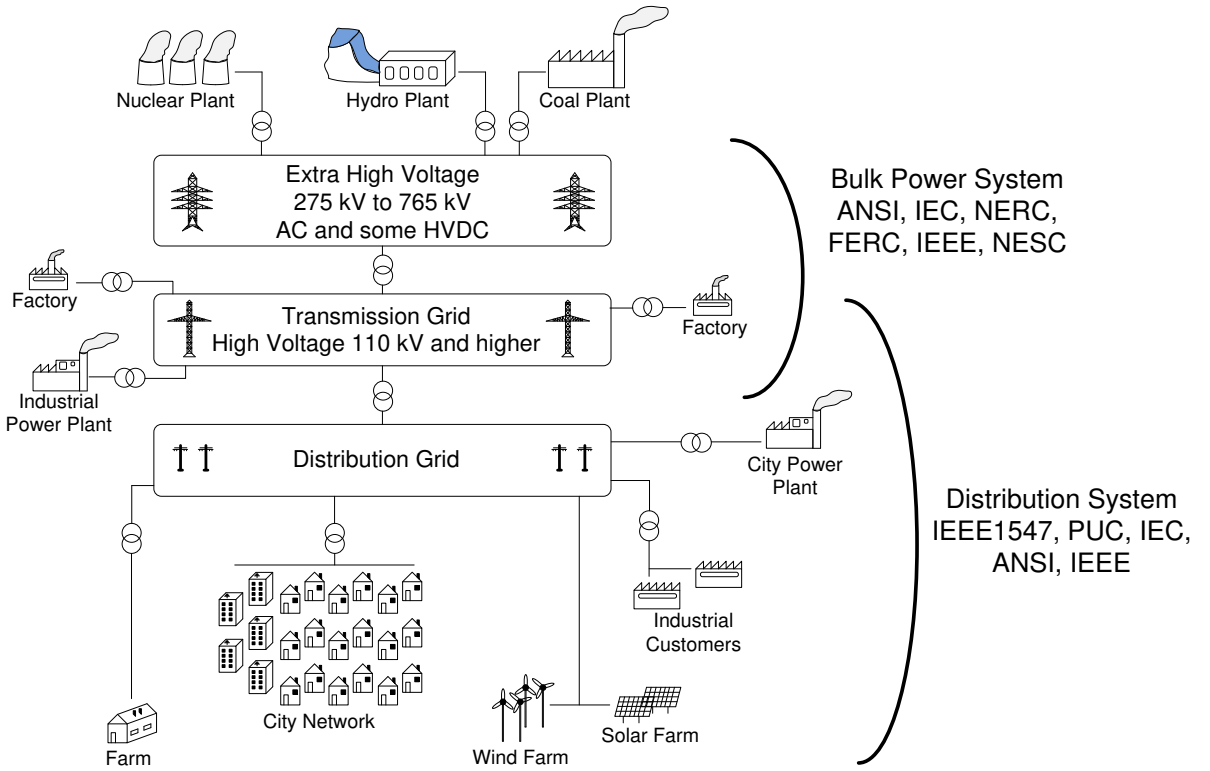


Figure 6:10 - Simplified diagram of the system levels and the applied standardization.

One of the most important standards related to the interconnection of DG into the electrical distribution system is IEEE 1547 (parts of which are also incorporated into UL 1741[85]) [86]. IEEE 1547 establishes criteria and requirements that all DG must adhere to in order to connect to the electrical power system. The requirements shall be met at the point of common coupling and they are applicable to all distributed resources technologies with aggregate capacity of 10 MVA or less.

The criteria concerns mainly voltage and frequency variation limits, synchronization aspects, intentional and unintentional islanding and response to abnormal conditions.

6.5 Estimating the Battery State-of-Charge (SOC)

Applications covering batteries should consider a model which describes its behavior. The model may include several parameters like SOC, terminal voltage, cell temperature, internal pressure, and so on. Battery models are commonly found in the literature [87]–[89]. The use of a more complex or simplified model depends on the application. A simplified model indicating the SOC and the State-of-Health (SOH) is sufficient for the IBBS proposed in this thesis. The batteries were simulated through the model available in PSIM software version 9.3.

Figure 6:11 presents a typical SOC curve for a lead-acid battery. The battery terminal voltage is around 12V for the whole range of charge, except on the borders. Two points are highlighted: the charged, at 95% of charge, and discharged, at 40%. These points are used to considerer the battery charged and discharged by the central and local controllers. They are valid for null current and after the battery chemical reactions being at rest. The choice of these values is based on spinning reserve criteria [90]. This criteria allows the IBBS to compensate for unpredictable imbalances between load and generation caused by sudden outages of generating units, errors in load forecasting, starting a motor or unexpected deviations of generating units from their production schedules [91].

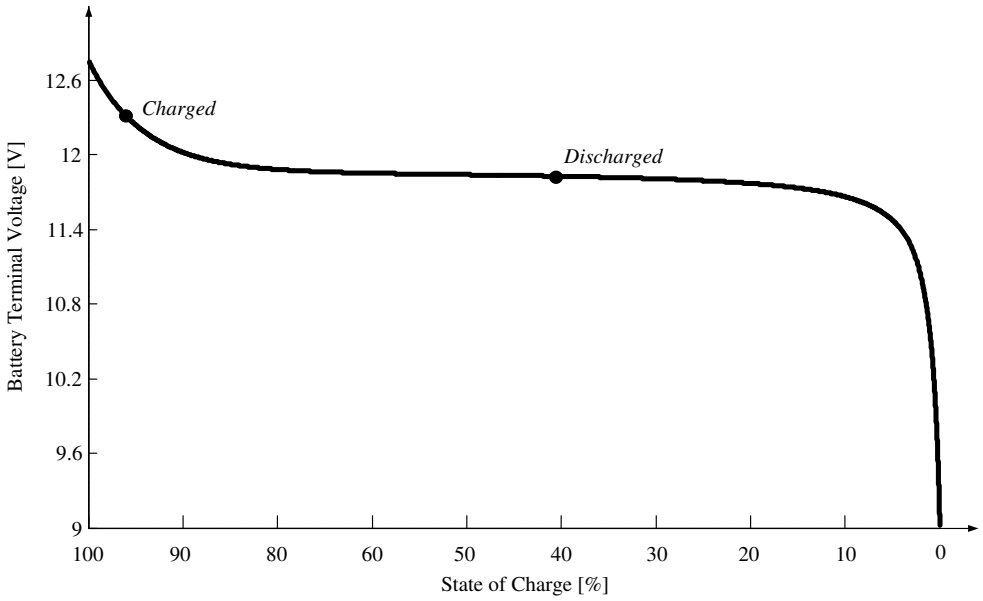


Figure 6:11 - Typical SOC curve for a lead-acid battery.

The battery SOC is not directly measured. Estimation must be done. A simplified way to estimate it is given by (6.8).

$$SOC(t) = 100\left(\frac{Q_{nom} - \int_{\tau_0}^{\tau} i_{bat}(t)\,dt}{Q_{nom}}\right) \tag{6.8}$$

where Q_{nom} and i_{bat} are the battery nominal charge and instantaneous current, respectively.

6.6 Estimating the battery State-of-Health (SOH)

The battery SOH is a measurement used to qualify the battery condition. The SOH states the age and degradation of a battery and may be estimated by means of verifying the following behaviors: increased float current, increased battery impedance, high cell voltage variation and reduce ability to receive charge.

Counting the number of cycles is an attractive manner to estimate the SOH. A high value is an indicative of an old battery. Therefore, each charging cycle is counted and its value is sent to the central controller. The counter is given by (6.9). Each time this equation is computed, the result is sent to the central controller. The battery datasheet usually supplies the number of cycles in battery life-time.

$$i_{\text{charge}}(k) = i_{\text{charge}}(k-1) + 1 \tag{6.9}$$

6.7 Ancillary functions

The proposed IBBS can perform different functions other than just injecting power into the grid or charging the batteries. Such functions can also be performed simultaneously. Even though almost all system operators presently do not allow DG to perform ancillary functions, this issue will certainly be under discussion in the coming years. Applications of power compensator with ancillary functions can be found in [77], [79], [92], [93].

This section describes how the proposal makes a storage capable to perform ancillary functions. The operation is divided into seven modes. They are:

i) Mode 1: Active power injection;
ii) Mode 2: Batteries charging;
iii) Mode 3: Active power injection and active filtering simultaneously;
iv) Mode 4: Active filter exclusively;
v) Mode 5: Harmonic currents compensation;
vi) Mode 6: Reactive power compensation;
vii) Mode 7: Stand-by.

Figure 6:12 presents a simplified block diagram of the manner how the modes are selected. The IBBS is embedded with a decision-taker algorithm. The central controller sends information to the IBBS to be used as inputs in the algorithm. The information is about the amount of demanded active power from the grid, and decisions of full or partial power quality compensation. The premises behind how the central controller decides these quantities are presented in next sections. For now, it is sufficient to considerer that the central controller already knows these information and sends them to the IBBS. The diagram shows also the use of one current controller for all modes of operation. Such controller is that one presented in section 6.9. The Conservative Power Theory (CPT) [94], [95] is used to obtain the current reference for the modes where the power quality is under requirement.

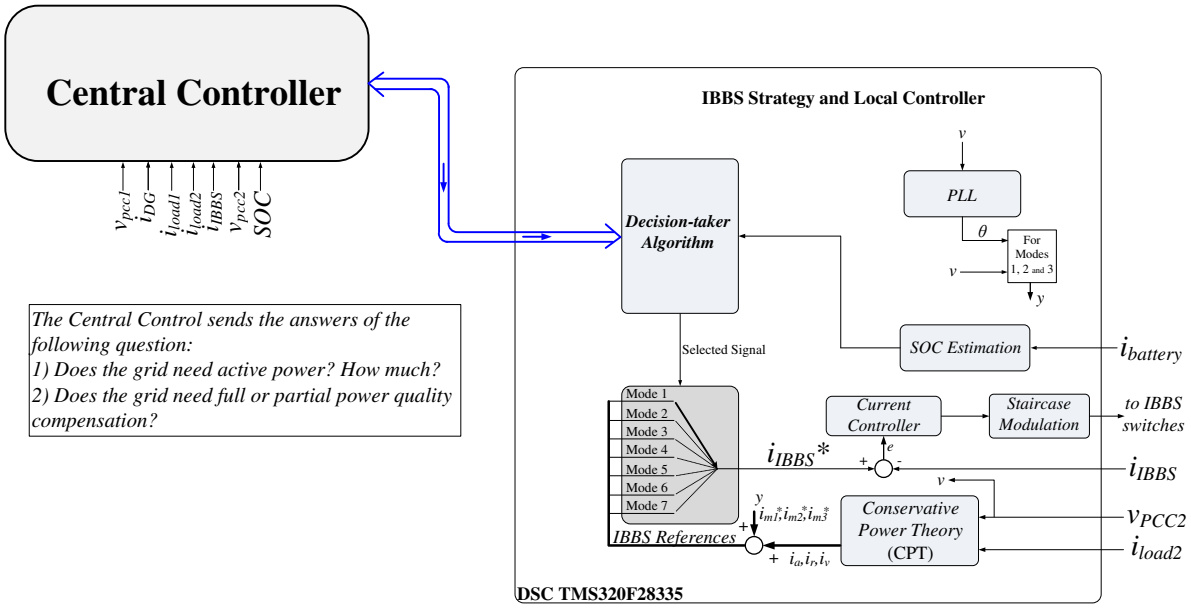


Figure 6:12 - Simplified block diagram of the manner how the modes are selected.

6.7.1 The conservative power theory

The CPT was first introduced by Tenti and Mattavelli in [96] and it was recently reformulated [94], [95]. The CPT is a time-domain theory that can be applied to single- or multiphase system with or without neutral conductor. It is based on the orthogonal decomposition of electrical variables, resulting electrical quantities with physical meaning. Each quantity represents load characteristics like consumed active power, stored energy, phase displacement between voltage and current, unbalancing and so on. Moreover, the CPT does not need any variable transformation. Some applications of the CPT are presented in [78], [97]–[101] . The CPT definitions, valid for any periodic waveform, are:

The average value of a variable x is given by (6.10).

$$\overline{x} = \frac{1}{T}\int_0^T x(t)dt \tag{6.10}$$

The time-integral of a variable x is given by (6.11).

$$x_{\int}(t) = \int_0^T x(\tau)d\tau \tag{6.11}$$

The unbiased integral of a variable x is given by (6.12).

$$\hat{x}(t) = x_{\int}(t) - \overline{x}_{\int}(t) \tag{6.12}$$

where the second term of (6.12) is the average value of (6.11). The unbiased term means average value.

The time-derivative of a variable x is given by (6.13).

$$\breve{x}(t) = \frac{dx(t)}{dt} \tag{6.13}$$

The unbiased integral and the time-derivative present the following properties:

$$\begin{aligned} &\hat{\breve{x}} = \breve{\hat{x}} = x \\ &\langle x, \breve{x} \rangle = \langle x, \hat{x} \rangle = 0 \\ &\langle x, \breve{y} \rangle = -\langle \breve{x}, y \rangle \\ &\langle x, \hat{y} \rangle = -\langle \hat{x}, y \rangle \\ &\langle \breve{x}, \hat{y} \rangle = \langle \hat{x}, \breve{y} \rangle = -\langle x, y \rangle \end{aligned} \tag{6.14}$$

where $\langle \cdot, \cdot \rangle$ is the internal product.

The RMS value of a variable x is represented by (6.15).

$$X_{rms} = \|x\| \tag{6.15}$$

For a given voltage $v(t)$ and a current $i(t)$, the active current, responsible for carrying active power, is given by (6.16).

$$i_a(t) = \frac{\langle v(t), i(t) \rangle}{\|v\|^2} v(t) \tag{6.16}$$

In a similar way, the reactive current, responsible for carrying reactive energy, is given by (6.17).

$$i_r(t) = \frac{\langle \hat{v}(t), i(t) \rangle}{\|v\|^2} \hat{v}(t) \tag{6.17}$$

The residual current is given by (6.18).

$$i_v(t) = i(t) - i_a(t) - i_r(t) \tag{6.18}$$

The residual current contains all quantities that do not carry neither active nor reactive energy.

6.7.2 The mode references

Each operation mode has its own current reference as follows.

i) Mode 1: Injecting active power with unity power factor

The IBBS supplies active power to the grid with unity power factor, if the grid voltage is free of distortion. The central controller informs the amount of power to be injected (Pref), respecting the IBBS limitation. The mode 1 reference is a sinusoidal waveform and in-phase with the PCC2 voltage, given by (6.19).

$$i_{m1}^{*} = \frac{P_{ref}}{\|v_{PCC2}\|}\sqrt{2}\sin\left(\theta + \pi/2\right) \tag{6.19}$$

ii) Mode 2: Charging the batteries with unity power factor

In this mode, the IBBS charges the batteries with unity power factor seen from the PCC2 and its voltage is free of distortions. Therefore, the mode 2 reference is sinusoidal, but now 180 degree phase shifted related to the PCC2 voltage. The mode 2 reference is given by (6.20).

$$i_{m2}^{*} = \frac{P_{ref\_bat}}{\|v_{PCC2}\|}\sqrt{2}\sin\left(\theta + \pi/2 + \pi\right) \tag{6.20}$$

where P_{ref_bat} is the power reference which must be drawn from the grid to charge the batteries.

iii) Mode 3: Injecting active power and operating as active filter simultaneously

The mode 1 is combined to active filtering. The IBBS injects active power and compensates load harmonic currents and reactive power simultaneously. The mode 3 reference is given by (6.21)

$$i_{m3}^{*} = \frac{P_{ref}}{\|v_{PCC2}\|}\sqrt{2}\sin\left(\theta + \pi/2\right) + i_{r2} + i_{v2} \tag{6.21}$$

iv) Mode 4: Operating exclusively as active filter

In this mode, the IBBS compensates the load harmonic current and the reactive energy. As result, the grid current presents a sinusoidal waveform and the PCC2 reaches the unity power factor. The mode 4 reference is given by (6.22).

$$i_{m4}^{*} = i_{load2} - i_{a2} \tag{6.22}$$

v) Mode 5: Harmonic compensation

Now, only the load harmonic currents are compensated. Therefore, the PCC2 may not present unity power factor, but the grid currents is sinusoidal. The mode 5 reference is given by (6.23).

$$i_{m5}^{*} = i_{load2} - i_{a2} - i_{r2} = i_{v2} \tag{6.23}$$

vi) Mode 6: Reactive energy compensation

Similarly, only the load reactive energy is compensated by the IBBS. Therefore, the IBBS current is a 90° phase-shifted sinusoidal waveform related to the PCC2 voltage while the grid current contains the load harmonic current. The mode 6 reference is given by (6.24).

$$i_{m6}^{*} = i_{load2} - i_{a2} - i_{v2} = i_{r2} \tag{6.24}$$

vii) Mode 7: Stand-by

Here, the IBBS is set to do nothing. The current must be null. Therefore, the mode 7 reference is given by (6.25).

$$i_{m7}^{*} = 0 \tag{6.25}$$

6.7.3 The decision-taker algorithm

The decision-taker algorithm is responsible for choosing the operation mode. The algorithm is embedded in the IBBS, but there is no restriction to run it in the central controller. Moreover, it is assumed that requested decision fits the IBBS power rate.

Researches covering decision-takers were presented in the literature and some of them will be briefly described here. Reference [102] presents a cooperative operation among some Distributed Energy Resource (DER) aiming loss reduction in a feeder by setting their active and reactive power references. The decision of how much should be the DER active and reactive power references comes from an optimized algorithm with voltage profile along the feeder as input variables. In reference [103], a synergistic control between a static reactive compensator and an active filter is presented. The decision how they must operate is based on the conservation of instantaneous complex power in a part of the network. Reference [104] presents a single-phase voltage source inverter capable to supply active and reactive power into the grid. The decision of the amount of power is based on the price of energy and power quality requirements.

The decision-taker algorithm proposed in this thesis is based on the following assumptions: the terminal voltage of the battery bank is evaluated. If its value is equal to the lower threshold point in the SOC curve, the IBBS is set to operate in mode 1. The IBBS is kept under mode 1 until the batteries have been fully charged. Otherwise, the decision-taker asks to the central controller if the grid needs active power. Figure 6:13 presents fictitious curves for load demand and generation. When load demand is higher than the generation, the grid needs active power.

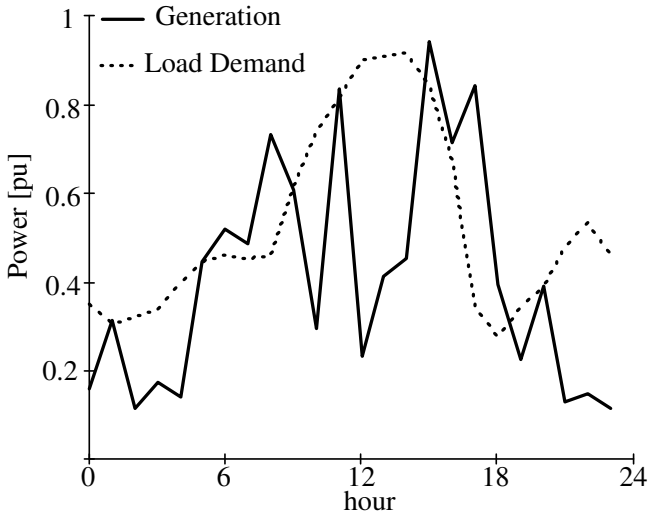


Figure 6:13 - Fictitious curves for load demand and generation.

If the grid needs active power, then the IBBS operates under mode 2. Otherwise, the IBBS waits the next decisions, which are based on the analysis of the energy quality at the PCC2.

The energy quality analysis consists of knowing the current THD and the voltage magnitude, both of them at the PCC2. Here, it is assumed that the grid fits power quality requirements when the feeder 2 current THD is lower than 5%, related to its fundamental, and the voltage magnitude value is within the range between 0.95 and 1.1 p.u.. Low current THD is interesting to the grid because a current with low distortion tends not to distort meaningfully the voltage waveform. The voltage magnitude and the current TDH are supposed to be known by the central controller and informed to the IBBS. Once the IBBS receives the information, the next decision is to know if it is necessary apply energy quality improvement. If the feeder 2 current THD is lower than 5% or the voltage magnitude is out of the specific range, then the IBBS will operate to improve the energy quality. But before that, the IBBS needs to decide if the compensation will be full or partial. Full compensation means the IBBS supplying all the reactive energy and harmonic currents from the nonlinear load. On the other hand, partial compensation means either reactive energy or harmonic currents compensation. If the feeder 2 current THD is higher than 5% and the voltage magnitude value is within the allowed range, the IBBS will perform full compensation. In this case, the IBBS will change to mode 3, if mode 2 is set, or it will operate in mode 4. If full compensation is not required, there is the possibility to apply partial compensation. If the feeder 2 current THD is higher than 5% and the voltage magnitude value is higher the specified range, harmonic currents compensation is performed. The IBBS is set to operate in mode 5. However, if the feeder 2 current THD is already lower than 5%, reactive energy compensation may be

applied. For doing that, the voltage magnitude value must be within or lower than the range. In such occasion, the IBBS is set to operate in mode 6.

After energy quality improvement, if applicable, the battery terminal voltage is evaluated again in order to verify if the batteries were fully charged. If yes, the IBBS stop charging the batteries and operates under mode 7. Otherwise, the IBBS evaluates if there is any mode set into it. If not, the IBBS operates under mode 7. After that, the cycle begins again. Figure 6:14 presents the decision-taker flowchart.

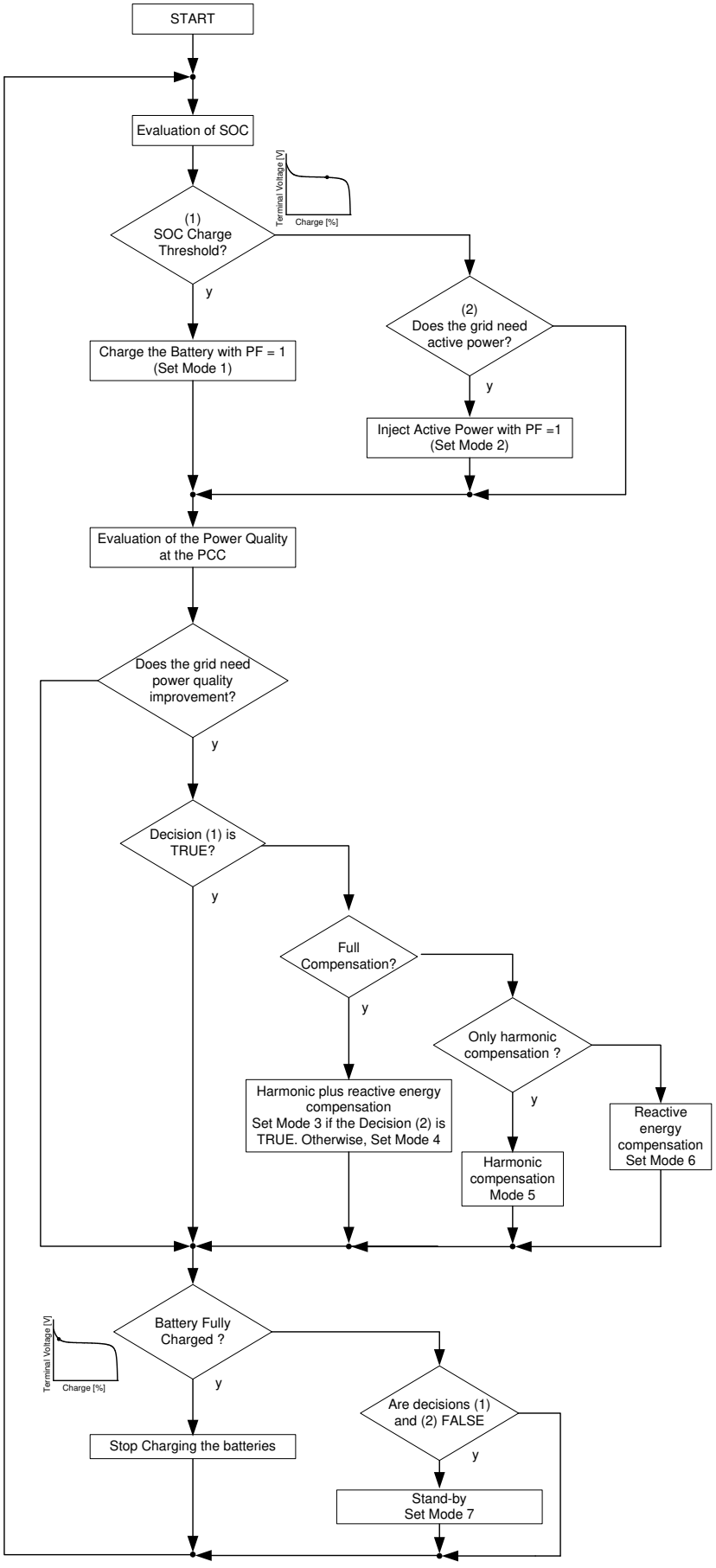


Figure 6:14 - Decision-taker flowchart.

6.7.4 Results for the IBBS with ancillary functions

The seven operation modes were experimentally verified. Figure 6:15 presents the waveforms during transition from mode 1 to mode 3. Initially, the IBBS is injecting active power into the grid with unity power factor. The feeder 2 current is highly distorted due to the non-linear load. The IBBS begins to operate also as active filter. It compensates the harmonics and the reactive energy of the load. Consequently, the IBBS current presents a distorted waveform and the feeder 2 current becomes sinusoidal and in-phase with the PCC2 voltage.

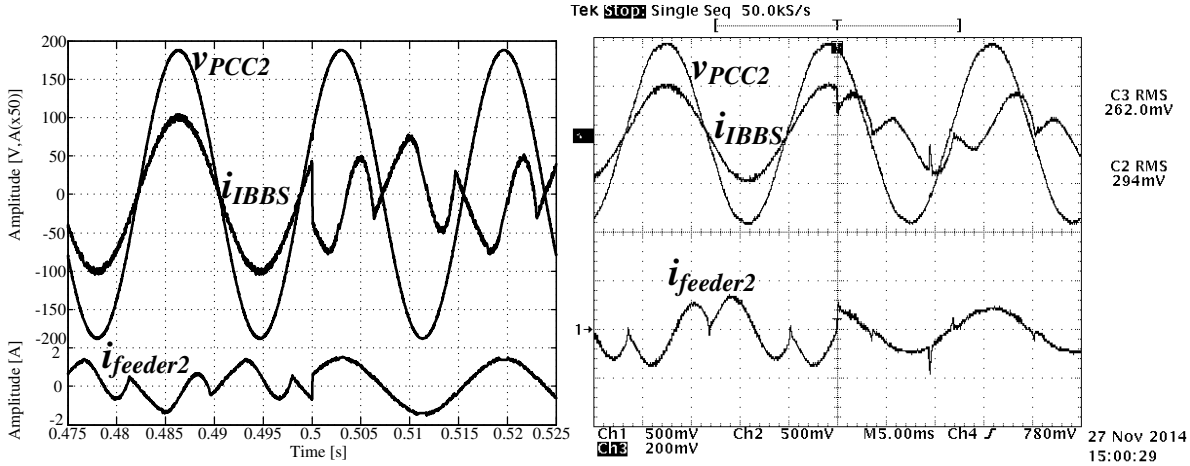
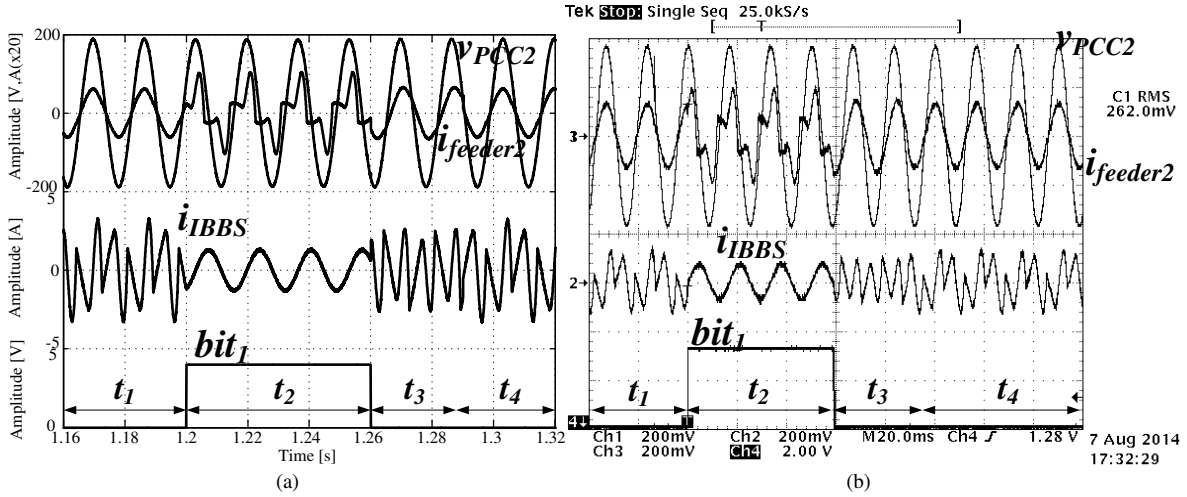


Figure 6:15 - Waveforms during transition from mode 1 to mode 3. (a) Simulation and (b) Experimental (Ch3: 0.5V/V; Ch1, Ch2: 0.1V/A).

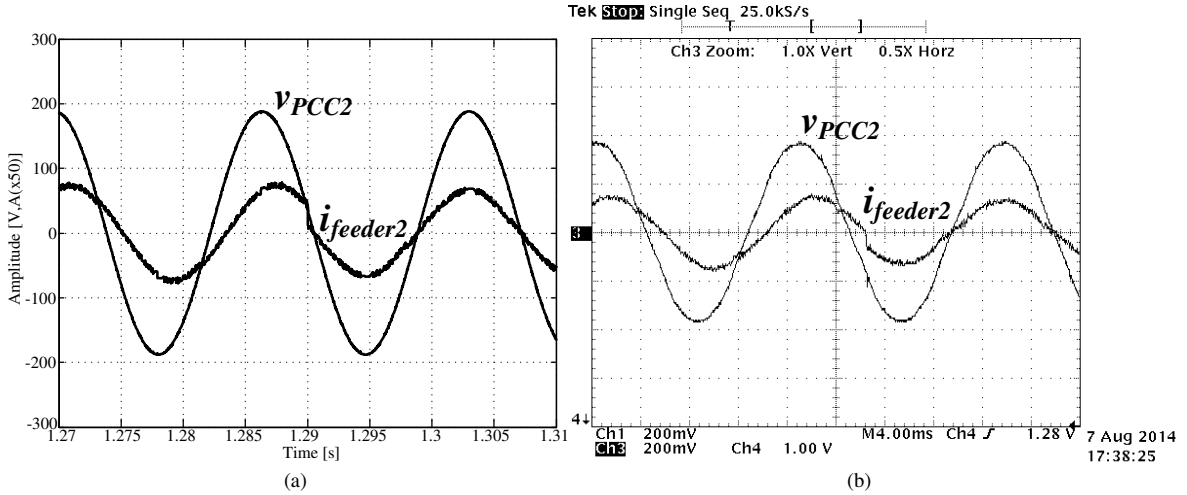
Figure 6:16 presents waveforms during the modes 4, 5 and 6. During the interval t1, the IBBS operates in mode 4, exclusively as active filter. The feeder 2 current is sinusoidal and in phase with the PCC2 voltage and the IBBS current is highly distorted. Right after, the IBBS changes from mode 4 to 6. The IBBS is now compensating only the load reactive energy. Its current is a sinusoidal waveform and 90 degree phase-shifted related to the PCC2 voltage. Later, during interval t3, the IBBS operates in mode 5, where only the harmonic currents from the load are compensated. The feeder 2 current is sinusoidal, but in out-of-phase related to the PCC2 voltage. The phase displacement between the feeder 2 current and the PCC2 voltage means the reactive energy consumed by the load. At the end, the IBBS comes back to the mode 4. All transitions occurred instantaneously, indicating the fast dynamic response of the IBBS.



(a) (b)

Figure 6:16 – Waveforms during the modes 4, 5 and 6. (a) Simulation and (b) Experimental (Ch1: 0.5V/V; Ch2, Ch3: 0.1V/A).

Figure 6:17 shows the PCC2 voltage and feeder 2 current in zoom during the last transition. Initially, the feeder 2 current is in out-of-phase related to the PCC2 voltage. Later, they are in phase, indicating the reactive energy compensation together with the harmonic compensation.



(a) (b)

Figure 6:17 - The PCC2 voltage and feeder 2 current in zoom during the last transition. (a) Simulation and (b) Experimental (Ch3: 0.5V/V; Ch1: 0.1V/A).

Figure 6:18 presents waveforms during a load step. In the scope trigger instant, 50% of the nominal load is included. The feeder 2 current keeps its sinusoidal waveform and in-phase with the PCC voltage.

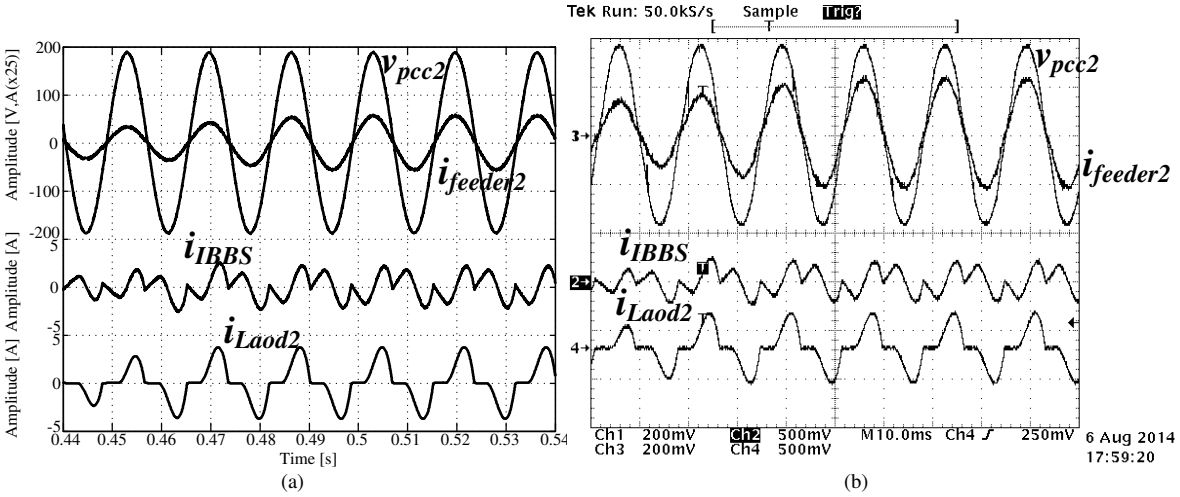


Figure 6:18 - Waveforms during a load step. (a) Simulation and (b) Experimental (Ch3: 0.5V/V; Ch1, Ch2, Ch4: 0.1V/A).

Results for modes 1 and 7 were already presented in Section 6.2.

Figure 6:19 presents results for the IBBS operating exclusively as active filter when a controlled rectifier is connected at PCC2. Initially, the IBBS is stand-by mode. The feeder 2 current is the controlled rectifier load current. Later, the feeder 2 current becomes sinusoidal. The feeder 1 current keeps distorted because the harmonic currents from the load 1 is not being compensated.

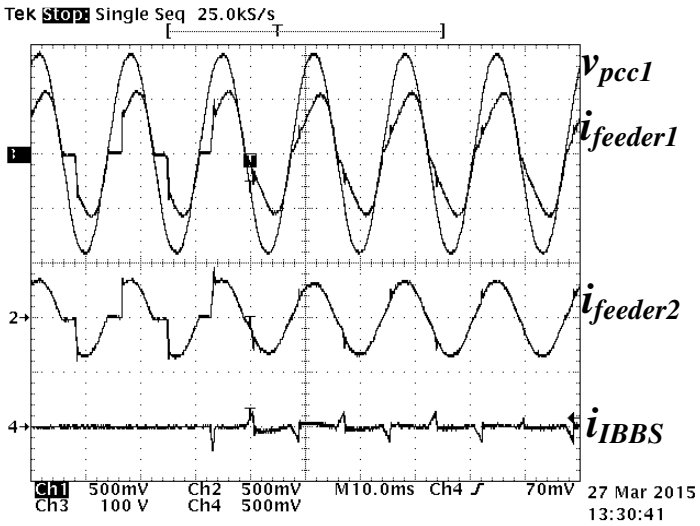


Figure 6:19 - Results for the IBBS operating exclusively as active filter when a controlled rectifier is connected at PCC2 (Ch3: 0.5V/V; Ch1, Ch2, Ch4: 0.1V/A).

6.7.5 Motor Starting Method

The IBBS has a special mode dealing with the starting process of a squirrel-cage induction motor. The method consists of a direct-on-line connection of the motor in PCC2, achieved by turning on the S_1 switch showed in Figure 6:1. The current drained by the motor

is initially supplied by the IBBS. Afterward, the IBBS gently transfers the motor current to the feeder 2. The result is a softer starter of the motor seen by feeder 2.

Figure 6:20 present results when S_1 switch is turned on. The motor is connected to PCC2 at the narrow position. The feeder 2 current is kept null. The IBBS is supplying the motor current. The nonlinear load at PCC2 was removed for better visualization of the feeder 2 current.

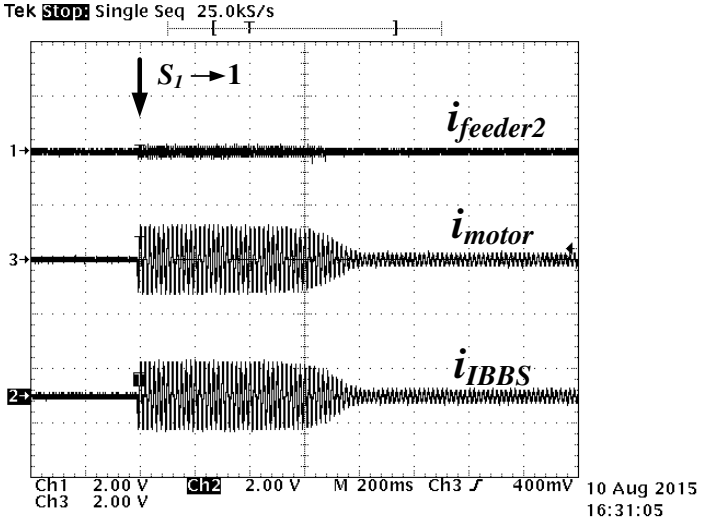


Figure 6:20 – Results when S_1 switch is turned on (Ch1, Ch2, Ch3: 0.1V/A).

Figure 6:21 presents results right after the S_1 switch is turned on. The IBBS supplies immediately the motor current. The feeder current suffers a slight swell due to the required time needed by IBBS to fill up the buffer used in the control strategy.

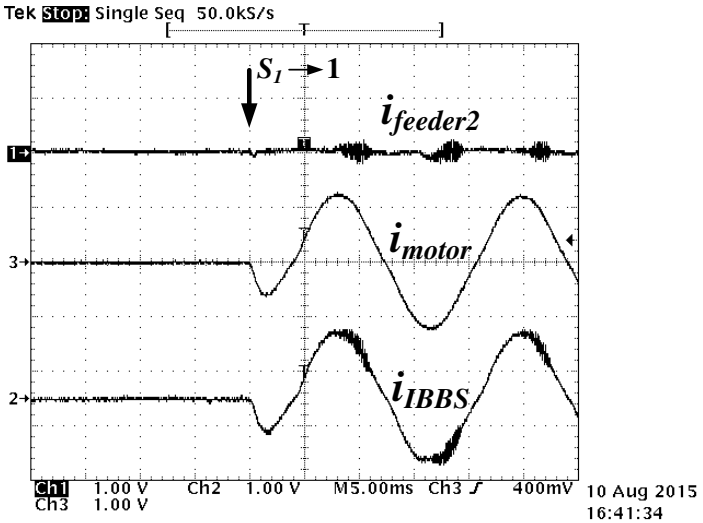


Figure 6:21 – Results right after the S1 switch is turned on (Ch1, Ch2, Ch3: 0.1V/A)..

Figure 6:22 presents results in steady-state condition. The feeder 2 current is null while the IBBS current is the motor current.

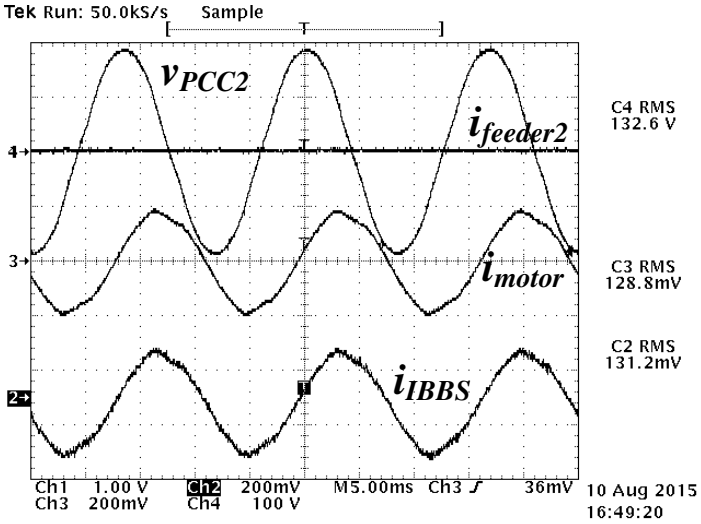


Figure 6:22 - Results in steady-state condition (Ch4: 0.5V/V; Ch1, Ch2, Ch3: 0.1V/A).

Figure 6:23 results during the moment of transference of the motor current from the IBBS to the feeder 2. The feeder 2 receives the motor current slowly while the motor current is kept unchanged. At the end, the IBBS current is null.

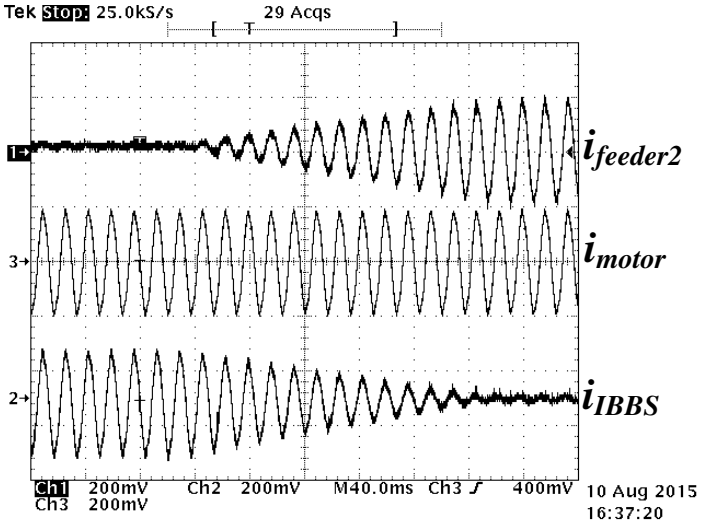


Figure 6:23 - Results during the moment of transference of the motor current from the IBBS to the feeder 2 (Ch1, Ch2, Ch3: 0.1V/A).

6.8 Hierarchical architecture

The central controller needs to define the amount of power the IBBS will inject into the grid and if the power quality improvement will be full or partial. Such information may be decided by the central controller or received from an upper agent, like a system operator. A hierarchical architecture appears when multiple agents are involved in taking decision of the system operation [105]–[107]. Each agent has limitation to take decisions. An agent must ask to an upper agent if the decision is beyond its responsibility. Figure 6:24 presents a typical hierarchical architecture with four layers. Other layers may be added

through it as well as other agents in each layer. The information handled by each layer is determined through specific criteria. The upper agent is the governmental policies, which usually deals with information about meeting the load demand, new investments and energy price. The System Operator (SO) deals with reservoir levels in hydro plants, activation of thermal plants and solutions for drought period. The central and local controllers operate with more detailed information, like voltage profile, current and voltage THD, battery temperature, etc. The next sections present details and results about how the proposed IBBS is applied in an hierarchical decision architecture.

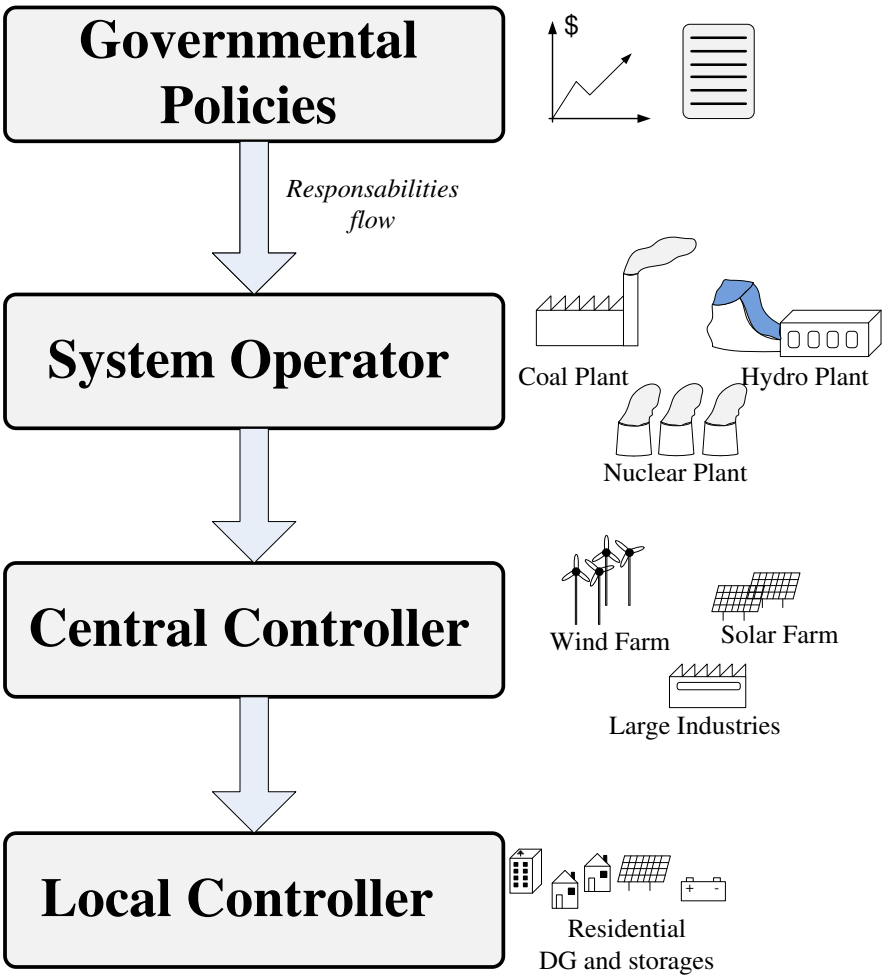


Figure 6:24 - Typical hierarchical architecture with four layers.

6.9 Local controller

Local controller usually deals with more information than centralized [108], [109]. Several details about the grid may be transferred among DGs connected close to each other which may be unnecessary or undesirable for the centralized controller. An example is the battery temperature information in a storage system. This information may be useful for local controller. A nearby DG may support the storage in order to get the situation

normalized. This alleviates the need of travelling the information to the centralized controller and the response of returning to the nearby DG.

Operation with local controller is performed in this section in an over temperature scenario. The following events occur.

i) The central controller establishes that the BUS bar must receive 340 W with unit power factor

ii) The local controller decides based on the DG primary source and the SOC curve that the IBBS supplies 68% of the demanded power while the DG supplies 32%.

iii) The IBBS detects over temperature on a battery bank.

iv) The IBBS wants to reduce its delivered power by half in order to get the situation normalized.

v) The local controller asks to the DG if there is available power to be supplied.

vi) In affirmative answer, the DG increases its delivered power and the IBBS, reduces.

v) The situation is normalized.

vi) Local controller establishes again the statements presented in ii.

Figure 6:25 presents the results for the moment when the IBBS reduces by half its injected power. The IBBS current is reduced by half while the DG current is increased. The grid current is kept unchanged, showing that the requirement imposed by the central controller is obeyed. Similar results were obtained during the moment where the situation was normalized.

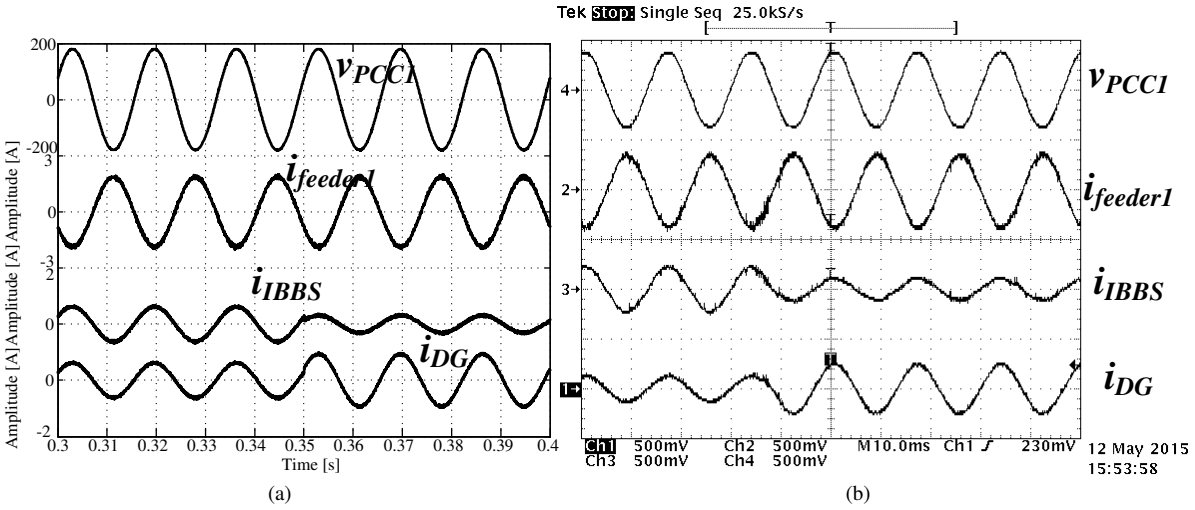


Figure 6:25 - Results for the moment where the IBBS reduces by half its injected power. (a) Simulation and (b) Experimental (Ch4: 0.5V/V; Ch1, Ch2, Ch3: 0.1V/A).

6.10 Centralized controller

In centralized structure, a single controller is intended to manage a great part of the grid. This type of controller is advantageous when there is a specific goal, such as loss reduction. This may be achieved by setting DG injected power set-points. The decision about the optimum set-point for the DGs is usually based on an optimized algorithm. Voltage and current along the system are the primary inputs for these algorithms. From them, a variety of information can be obtained like apparent power, power factor, unbalances, etc. Such variables are good for real-time decisions. The centralized controller may also be capable of daily planning. Input variables about the prediction of load demand, solar irradiation, wind speed and energy price along one day may be helpful for an optimum planning. Storage devices may have their contribution to the uninterrupted supply improved by precise scheduling of their charging and discharging processes. Figure 6:26 presents the behavior of the solar irradiation, the load demand curve and the wind speed along one day. The centralized controller can compute or receive these curves from the system operator and run an algorithm to best determine how the DG and storage elements should operate along the day. As result, the system may offer better reliability and lower cost compared to a traditional distribution system.

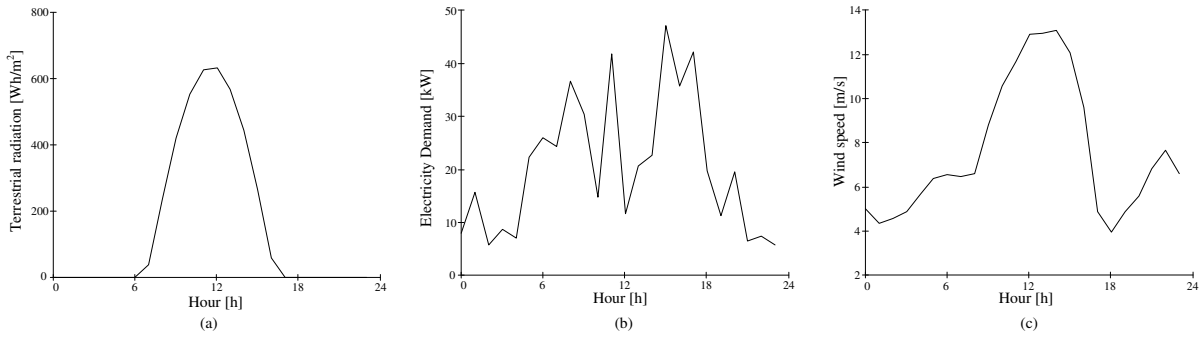


Figure 6:26 - Behavior of the terrestrial irradiation (a), the load demand curve (b) and the wind speed (c) along one day.

The operation of the IBBS together with the centralized controller is performed. The DG is emulated as a Wind Generator (WG) system. The DG is mentioned as WG interchangeably. Its delivered power is intermittent. The central controller measures the WG output current and the PCC1 voltage, computes its active power and send it to the IBBS. Additionally, the central orders to the IBBS to compensate the floating power delivered by the WG. The result is a constant power received from the WG and the IBBS. The nonlinear loads are removed for better visualization of the grid current.

Figure 6:27 presents the output cumulative power in function of the wind speed for the WG and for the IBBS. The region delimited by *A* is the WG operation points. For wind speeds from zero to approximately 10 m/s, the WG supplies active power according to available energy from the wind. Any sudden increase or reduction in the wind speed reflects in the profile of the supplied power. For wind speeds higher than 10 m/s, the WG reaches its nominal power and the pitch control [110] guarantees the safety operation. The region *B* is the IBBS operation points. The IBBS supplies active power during low wind speed moments. In such moments, the sum of the delivered power from the IBBS and the WG is constant. The IBBS operates only for wind speeds higher than approximately 4 m/s due to the most WG systems begin to operate after such speed [84].

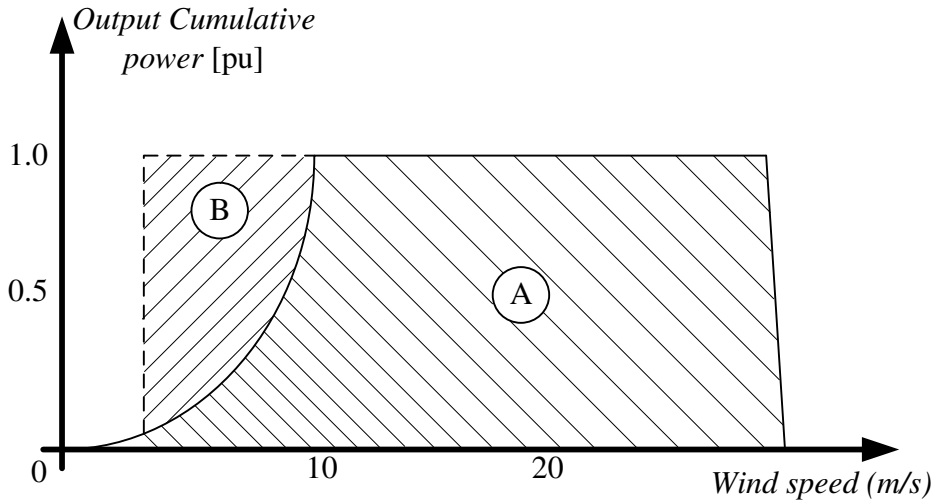


Figure 6:27 - Output cumulative power in function of the wind speed for the WG and for the IBBS.

Figure 6:28 presents results for floating power compensation in a large time scale. The DG current changes according to the emulated wind. At the narrow position, the amplitude of the IBBS output current is modified according to the DG current. The amplitude of the grid current is kept constant, indicating the reception of constant power.

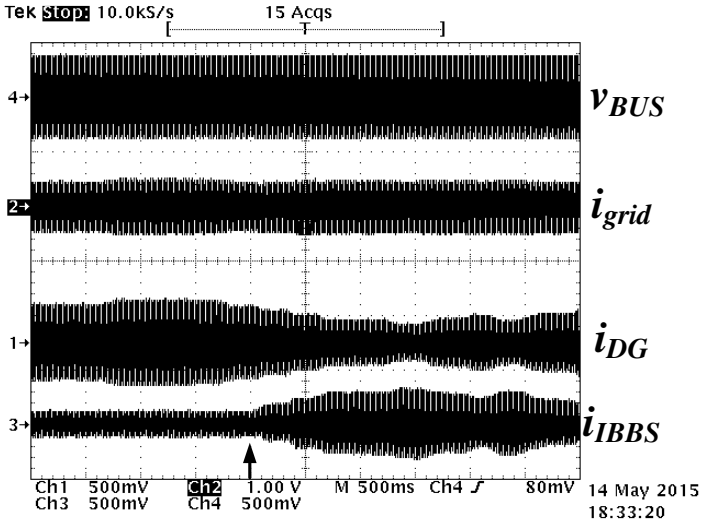


Figure 6:28 - Results for floating power compensation in a large time scale (Ch4: 0.5V/V; Ch1, Ch2, Ch3: 0.1V/A).

Figure 6:29 presents the previous result with a zoom in the dashed box (central of the screen). The DG and IBBS current are sinusoidal and in-phase related to the BUS voltage. The grid current is also sinusoidal, but in counter-phase related to the BUS voltage, indicating the receiving of power.

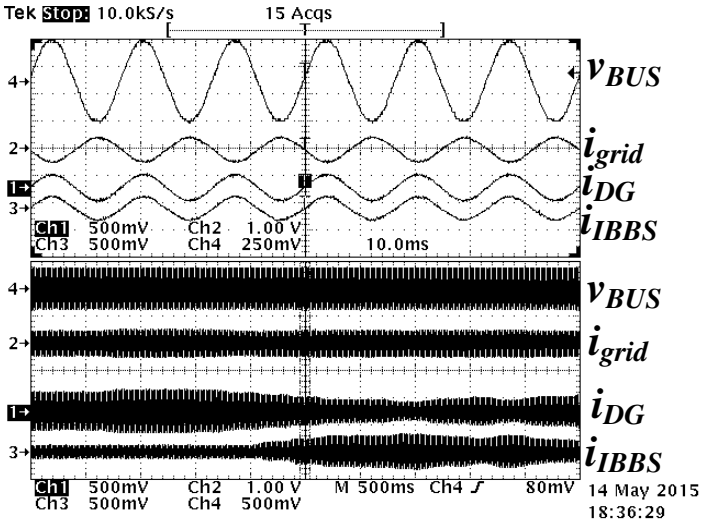


Figure 6:29 - The previous result with a zoom (upper) in the dashed box (Ch4: 0.5V/V; Ch1, Ch2, Ch3: 0.1V/A).

The example is led to a scenario with charging the IBBS batteries with energy from the WG system. The central controller still requires constant power from the both WG and IBBS. Without the IBBS, the WG system would apply the pitch control if its available power is higher than the required by the central control, resulting in energy wasting. However, the IBBS can use such energy to charge its batteries, if the SOC curve admits it.

Figure 6:30 presents results for charging the batteries with excessive energy from the WG system. The DG and IBBS current have their amplitudes modified along the time,

indicating the fulfillment of requirement imposed by the central controller. The zoom shows the moment where the IBBS batteries are charged, evidenced by the counter-phase IBBS current related to the BUS voltage.

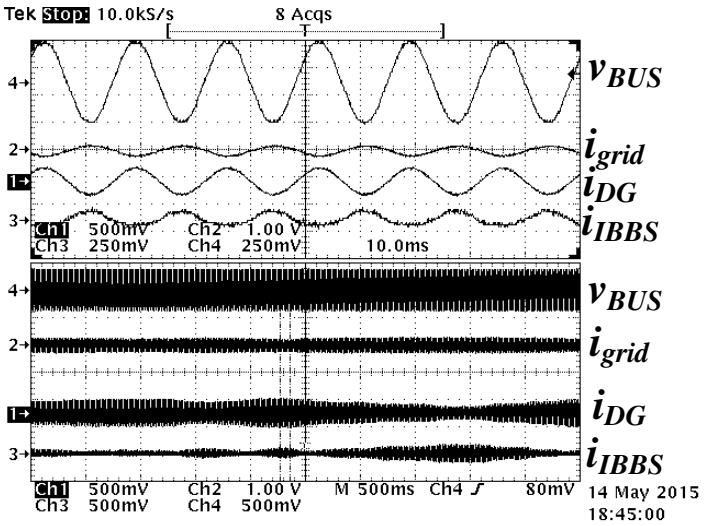


Figure 6:30 - Results for charging the batteries with excessive energy from the WG system (Ch4: 0.5V/V; Ch1, Ch2, Ch3: 0.1V/A).

6.11 Synergistic operation

This section presents a synergistic operation of the smart micro-grid. The main goal is to make the distribution system presented in Figure 6:1 to operate as a single element. The principle of operation is to handle the feeder currents by means of the IBBS and the DG. The central and local controllers are involved in this operation. Figure 6:31 presents the representation of the system as a single element.

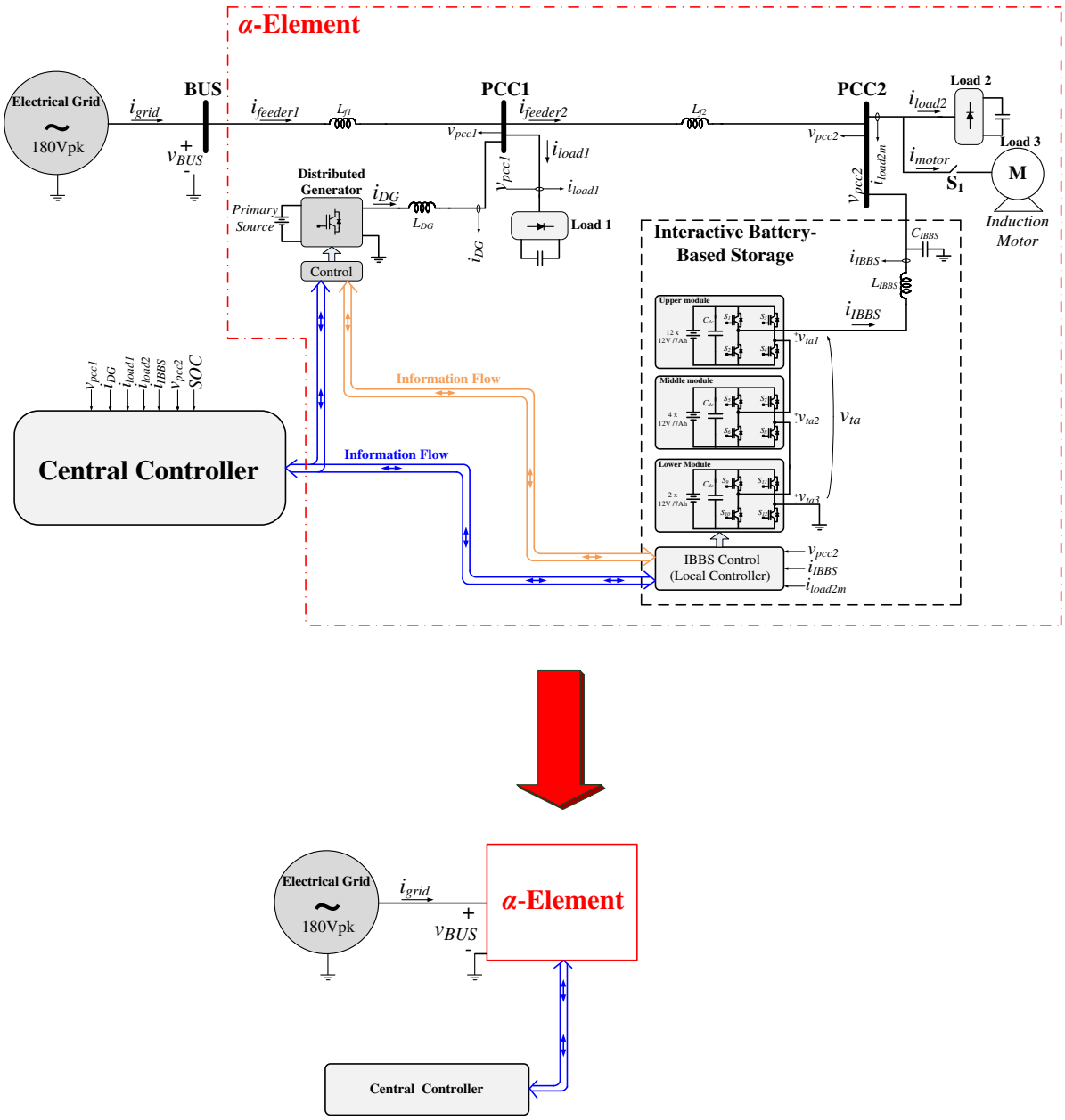


Figure 6:31 - Representation of a part of the system as a single element.

By means of IBBS, the DG and local controller, the element can behave according to requirements imposed by the central controller. Three requirements are covered: cancellation of the input current, operation under sinusoidal input current and injection of active power into the grid. Theses requirement are independent of each other and the loads inside the element are fed all the time.

i) Requirement 1: Cancelling the input current

In this requirement, the α-element has its input current cancelled while the loads keep working. Moreover, the electrical grid maintains connected. A system operator may be interesting in cancelling the current of a feeder when distribution losses reduction is under

concern. By cancelling the feeder current, the distribution losses in such feeder is also cancelled. Therefore, the requirement 1 objective can be expressed in mathematical form as presented in (6.26).

$$i_{grid}(t) \to 0 \quad \text{as} \quad i_{feeder1}(t) \to 0 \quad \text{and} \quad i_{feeder2}(t) \to 0 \tag{6.26}$$

In order to cancel the current of the feeders, it is sufficient to set the DG to supply the current drained by load 1 and the IBBS to supply the current drained by load 2, as stated in (6.27).

$$i_{DG}(t) = i_{load1}(t) \quad \text{and} \quad i_{IBBS}(t) = i_{load2}(t) \tag{6.27}$$

The DG current can also be given by (6.28).

$$i_{DG}(t) = i_{a\_load1}(t) + i_{r\_load1}(t) + i_{v\_load1}(t) \tag{6.28}$$

The IBBS current can also be given by (6.29).

$$i_{IBBS}(t) = i_{a\_load2}(t) + i_{r\_load2}(t) + i_{v\_load2}(t) \tag{6.29}$$

Figure 6:32 presents initial results for fulfillment of requirement 1. Initially, both DG and IBBS are turned off. The IBBS turns on at the scope trigger position. Before that, the feeder 1 and 2 have high distorted currents. As soon as IBBS begins to operate, the feeder 2 has its current cancelled. The IBBS current is the current (not shown) of the load 2. The feeder 1 has its current decreased, but it is still highly distorted due to the DG is still turned off.

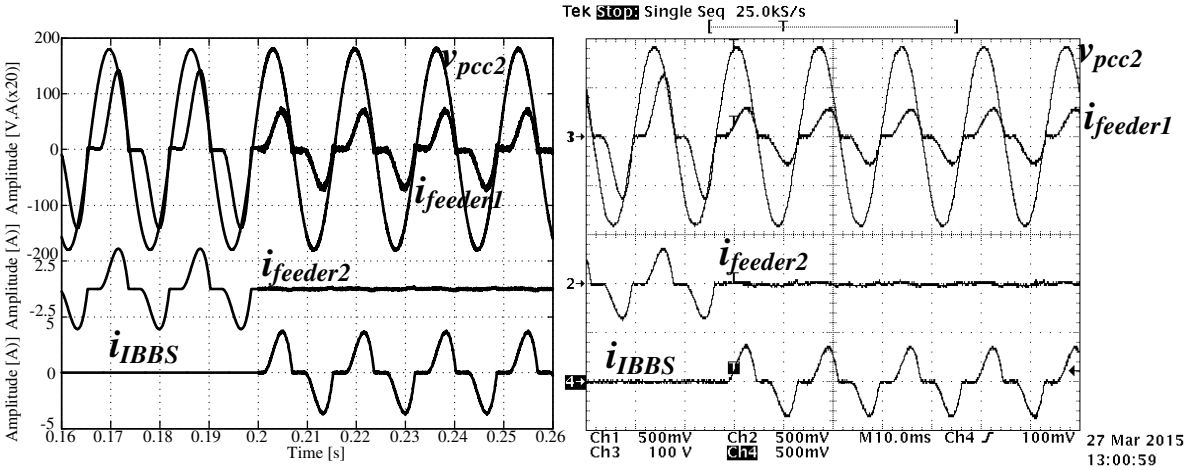


Figure 6:32 - Initial results for fulfillment of requirement 1. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch4: 0.1V/A).

Figure 6:33 presents final results for fulfillment of requirement 1. The DG current is the load 2 current. Both feeder 1 and 2 have null current. The requirement 1 is fulfilled. The grid current is cancelled while the loads keep fed. The cancellation of the feeder currents was cancelled sequentially for better visualization, but they could be done simultaneously.

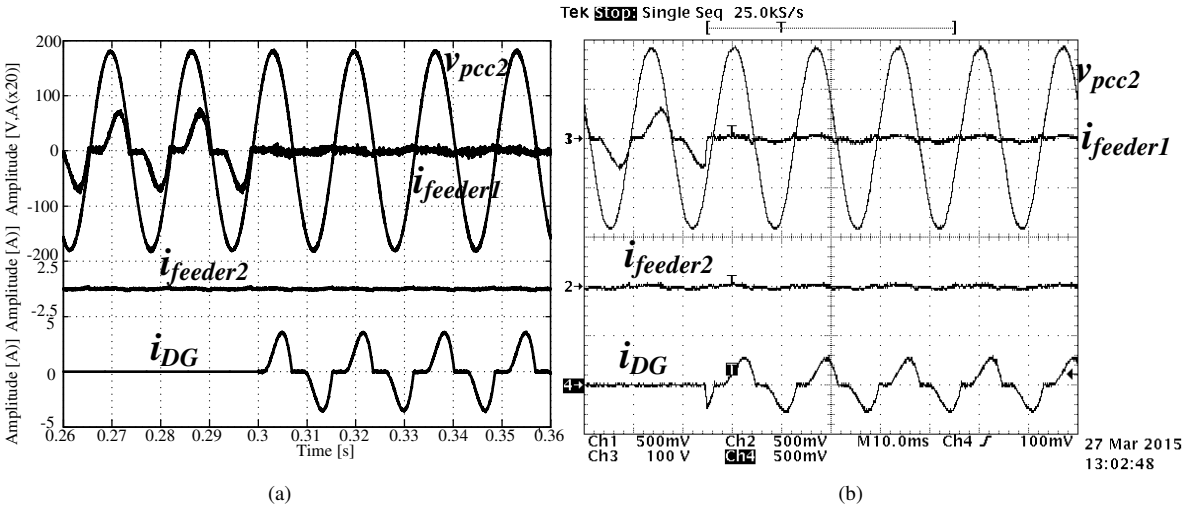


Figure 6:33 – Final results for fulfillment of requirement 1. (a) Simulation and (b) Experimental Ch1, Ch2, Ch4: 0.1V/A).

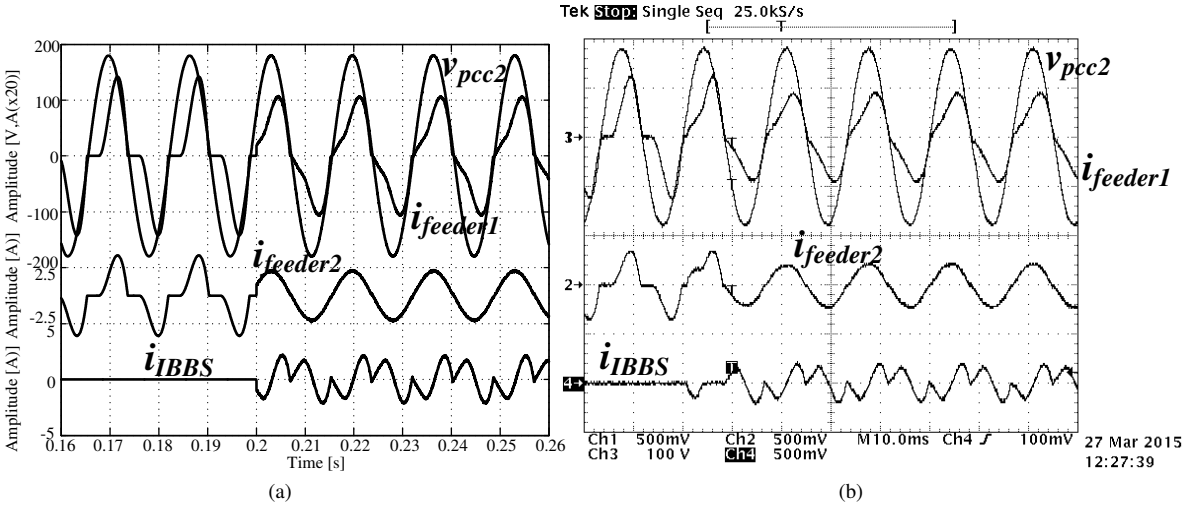
ii) Requirement 2: Sinusoidal input current

In this requirement, the α-element operates under sinusoidal input current. The IBBS and DG supply the reactive energy and the void current of the nonlinear loads while the grid supplies the active power. Operation with sinusoidal input current in a bar downstream may be interesting to a system operator when distorted currents are damaging the PCC voltages. Here, it is assumed that the PCC voltage is distorted due to the nonlinear load current. The central measures the voltage distortion. The level of the distortion is considered high and the central controller decides that the α-element must operate with sinusoidal input current.

The sinusoidal input current is achieved if the IBBS and/or DG operate as active filter. Both of them can supply the non-active current for the PCC1 and PCC2. However, in order to avoid the circulation of distorted current in the feeders within the α-element, the DG is responsible to supply the non-active current for the nonlinear load connected at PCC1 while the IBBS to the nonlinear load connected at PCC2. Therefore, the requirement 2 objective can be expressed in mathematical form as presented in (6.30).

$$\begin{aligned} & i_{grid}(t) \to i_{a\_load1}(t) + i_{a\_load2}(t) \\ & \text{as } i_{DG}(t) \to i_{r\_load1}(t) + i_{v\_load1}(t) \\ & \text{and } i_{IBBS}(t) \to i_{r\_load2}(t) + i_{v\_load2}(t) \end{aligned} \tag{6.30}$$

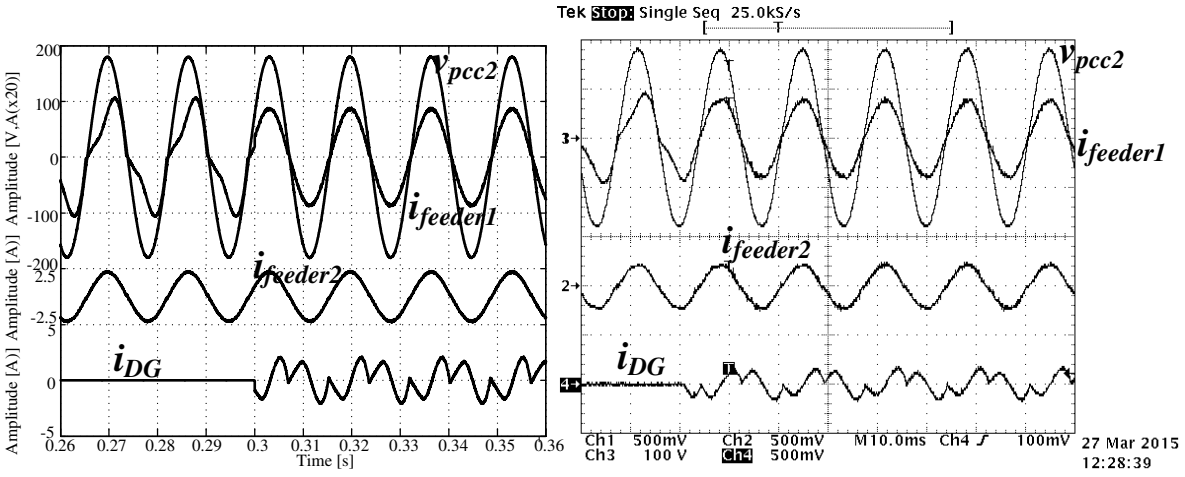
Figure 6:34 presents initial results for fulfillment of requirement 2. The IBBS turns on at the trigger position and the feeder 2 current becomes sinusoidal. The feeder 1 current has its distortion reduced.



(a) (b)

Figure 6:34 - Initial results for fulfillment of requirement 2. (a) Simulation and (b) Experimental Ch1, Ch2, Ch4: 0.1V/A).

Figure 6:35 presents final results for fulfillment of requirement 2. The feeder 1 current reaches a sinusoidal waveform by the moment the DG turns on. In the end, both the feeder 1 and 2 currents are sinusoidal and in-phase related to the PCC1 and PCC2 (not shown) voltages, respectively. The requirement 2 is fulfilled.



(a) (b)

Figure 6:35 – Final results for fulfillment of requirement 2. (a) Simulation and (b) Experimental Ch1, Ch2, Ch4: 0.1V/A).

iii) Requirement 3: Injection of active power into the grid with unit power factor.

The central controller demands from the α-element the reception of an amount of active power within acceptable levels of quality. The system operator may desire active power when the load demand is higher than the power production. Without any ad hoc solution, load curtailment would probably happen.

The requirement 2 objective can be expressed in mathematical form as presented in (6.31), assuming that the input voltage is free of distortions.

$$i_{grid}(t) \rightarrow -i_{power}(t) = \frac{P_{ref}}{\|v_{BUS}\|} \sin\left(\theta + \pi/2\right) \tag{6.31}$$

where i_{power} is the current supplied to the grid and P_{ref} is the power reference power informed by the central control. The minus signal is to indicate that the grid current is in counter-phase related to the BUS voltage

The DG and the IBBS must feed the load, inject the demanded power and compensate the power quality at the element input terminals. The local controller decides that the IBBS 2 supplies active power and operate as active filter simultaneous while the DG operates only as active filter.

The DG current is given by (6.32).

$$i_{DG}(t) = i_{r\_load1}(t) + i_{v\_load1}(t) \tag{6.32}$$

The IBBS current is given by (6.33).

$$i_{IBBS}(t) = i_{a\_load1}(t) + i_{load2}(t) + i_{power}(t) \tag{6.33}$$

Figure 6:36 presents the PCC1 voltage and the feeder 1 and 2 currents in a long time scale. Initially, the waveforms of the feeder 1 and 2 currents are those presented in Figure 6:35. The feeder 2 reaches first the zero current, indicating that the IBBS is injecting active power in a certain rate. As the time goes on, the amount of injected power is enough to feed the load at PCC2 and also to invert the flux of feeder 2. The feeder 1 is still draining power from the grid due to the load connected at PCC1. The IBBS continues injecting power. At the end, the load 2 is fully supplied and the grid receives power with unit power factor. The requirement 3 is fulfilled.

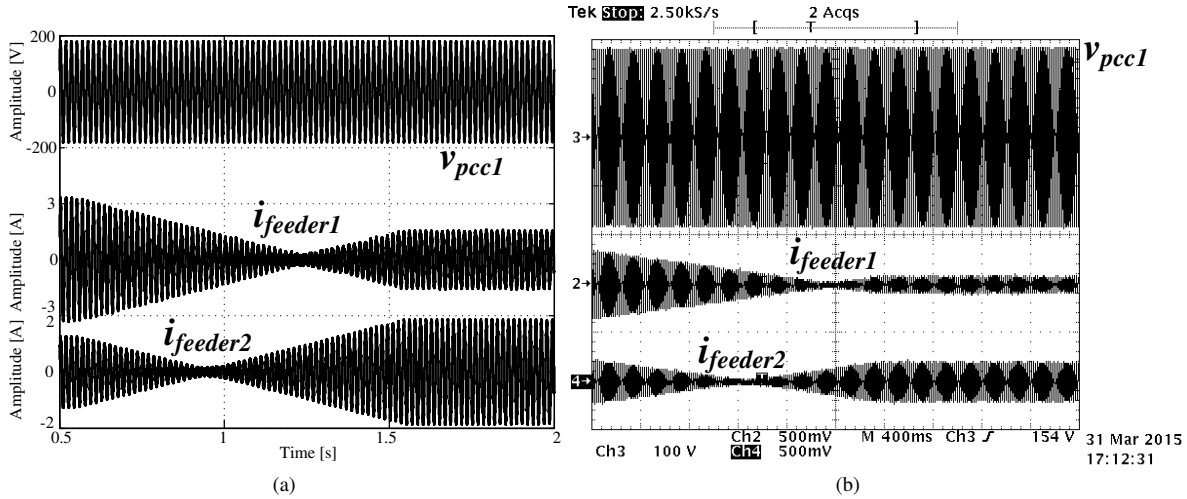
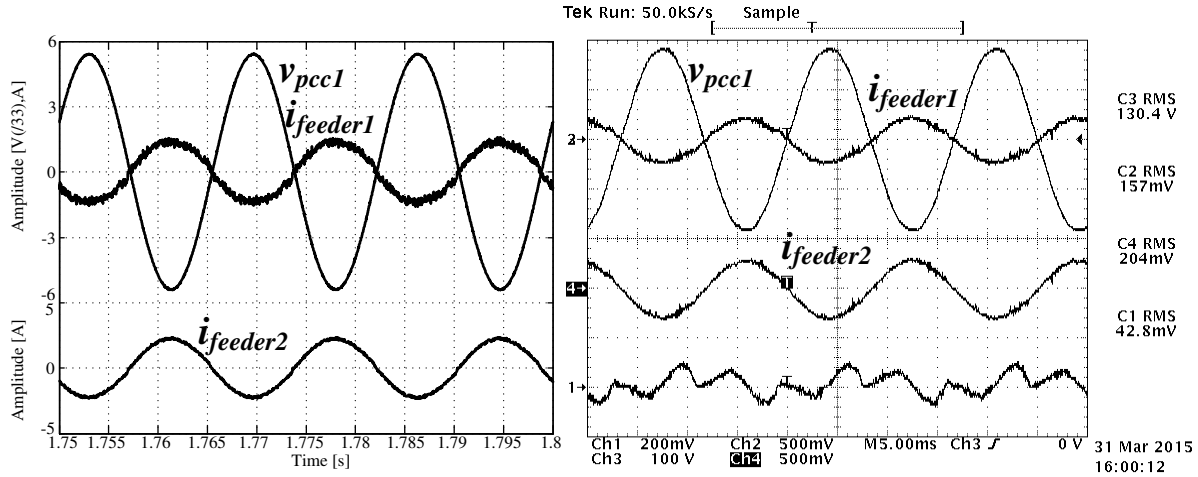


Figure 6:36 - PCC1 voltage and the feeder 1 and 2 currents in a long time scale. (a) Simulation and (b) Experimental Ch1, Ch2, Ch4: 0.1V/A).

Figure 6:37 presents the steady-state results after the fulfillment of requirement 3. Both feeder 1 and 2 currents are sinusoidal and 180 degree phase-shifted related to the PCC1 voltage. Therefore, the grid receives from the α-element active power and the PCCs are kept within acceptable power quality levels.



(a) (b)

Figure 6:37 - Steady-state results after the fulfillment of requirement 3. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch4: 0.1V/A).

6.12 Isolated operation

The proposed IBBS has the ability to operate in isolated smart micro-grid. Isolated grids are characterized by the absence of a stiff generator. One of the generators must supply a controlled voltage, regulated in frequency and amplitude. Other generators shall not temper these quantities. Isolated grids differ from islanded grids in the fact that first is permanently energized by its DG while the second is primarily energized by their DG only in occurrence of fault in the stiff generator. Figure 6:38 presents the IBBS connected to an isolated smart micro-grid. The grid is composed by one PCC, one nonlinear load and one DG. There is only local controller, even though central controller is also applicable. The IBBS is responsible to supply the controlled voltage while the DG is controlled in current mode. The IBBS output current is not controlled. For the sake of simplicity, the primary source of the DG is considered free of energy shortage.

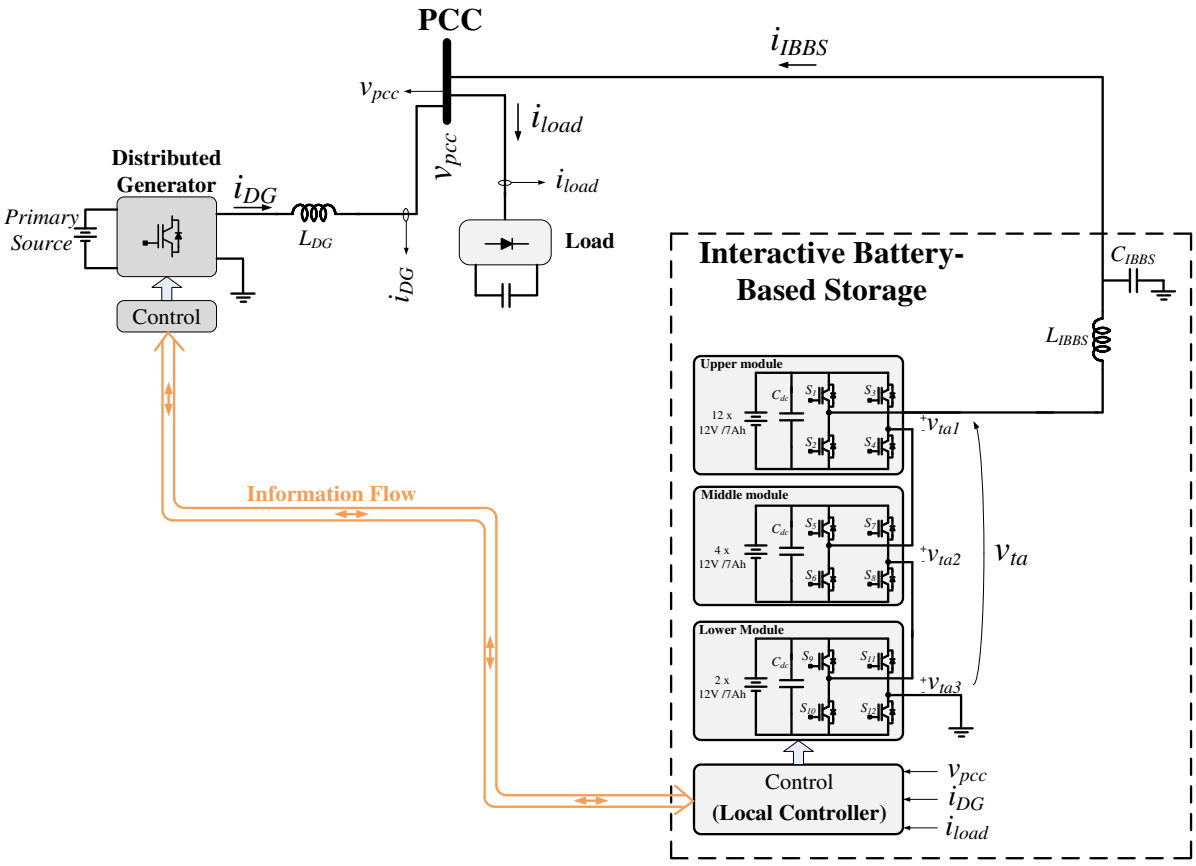


Figure 6:38 - The IBBS connected to an isolated smart micro-grid.

The IBBS controls the isolated grid by keeping the PCC voltage steadily controlled. The PCC voltage is controlled by means of the control presented in Section 6.3.3. Figure 6:39 presents the decision-taker algorithm performed by the local controller. The IBBS computes the DG output power and verify its quantity. If the available power is enough to feed the load, the IBBS orders to the DG to do that. In this case, the DG current reference is the load current. If the available power is not enough, the IBBS verifies if active filter action is required. The verification of necessity of active filtering action is performed through an overload occurrence. In such condition the PCC voltage may suffer distortion due to the voltage drop across the IBBS output filter. If the active filtering action is necessary, the DG is set to operate as active filter. Its current reference is the load current subtracted by the active current, obtained through the CPT. If the active filtering action is not necessary, the IBBS feeds the load and the DG reference current is set to be null.

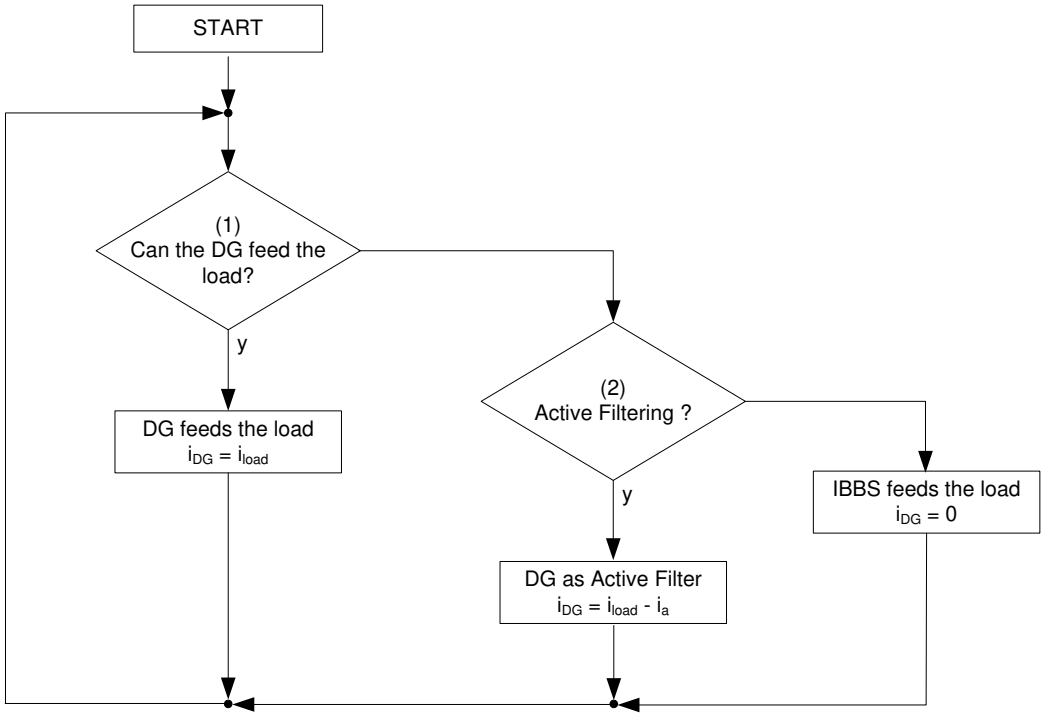
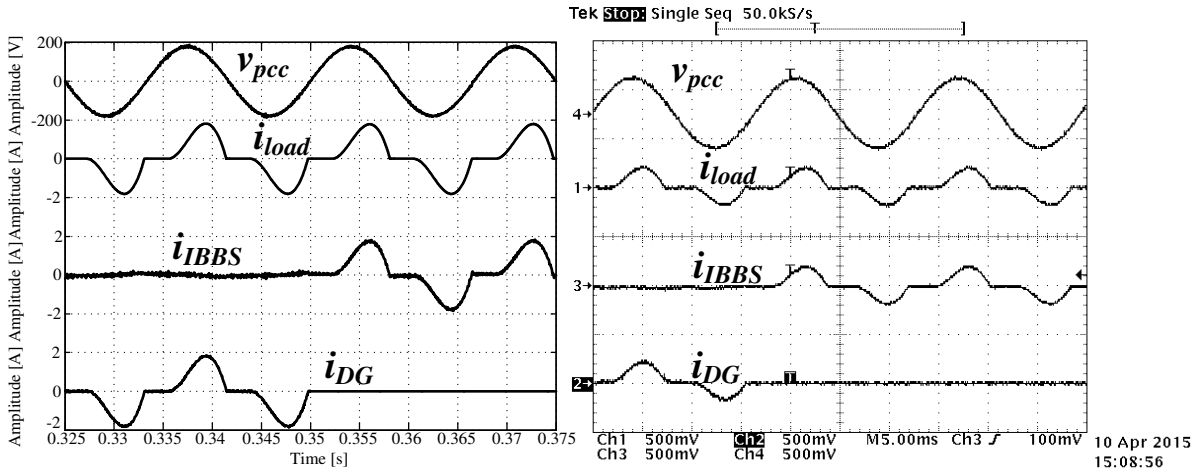


Figure 6:39 - Decision-taker algorithm performed by the local controller.

Figure 6:40 presents results for changing the answer in inquiry (1) from YES to NO. Initially, the DG is feeding the load current load and the IBBS current is null. Later, the IBBS supplies the load and the DG current is cancelled. The load current and the PCC voltage are kept unchanged.



(a) (b)

Figure 6:40 - Results for changing the answer in inquiry (1) from YES to NO. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch3: 0.1V/A; Ch4: 0.5V/V).

Figure 6:41 presents results for changing the answer in inquiry (1) from NO to YES. Initially the IBBS is feeding the load current while the DG current is null. Later, the DG supplies the load current and the IBBS current is cancelled.

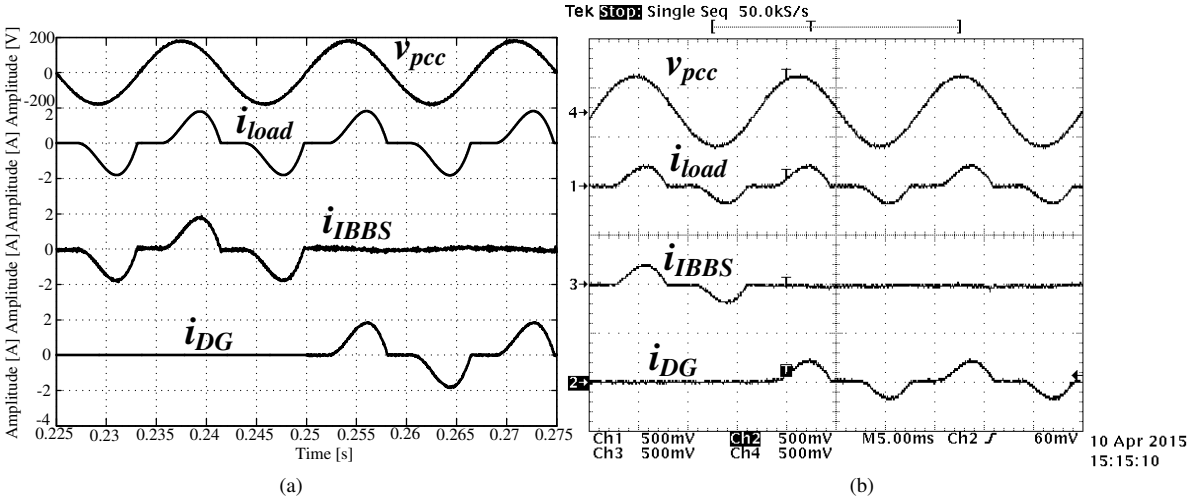


Figure 6:41 - Results for changing the answer in inquiry (1) from NO to YES. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch3: 0.1V/A; Ch4: 0.5V/V).

Figure 6:42 presents results for the DG operating as active filter. The DG current is distorted while the IBBS current is sinusoidal and in-phase related to the PCC.

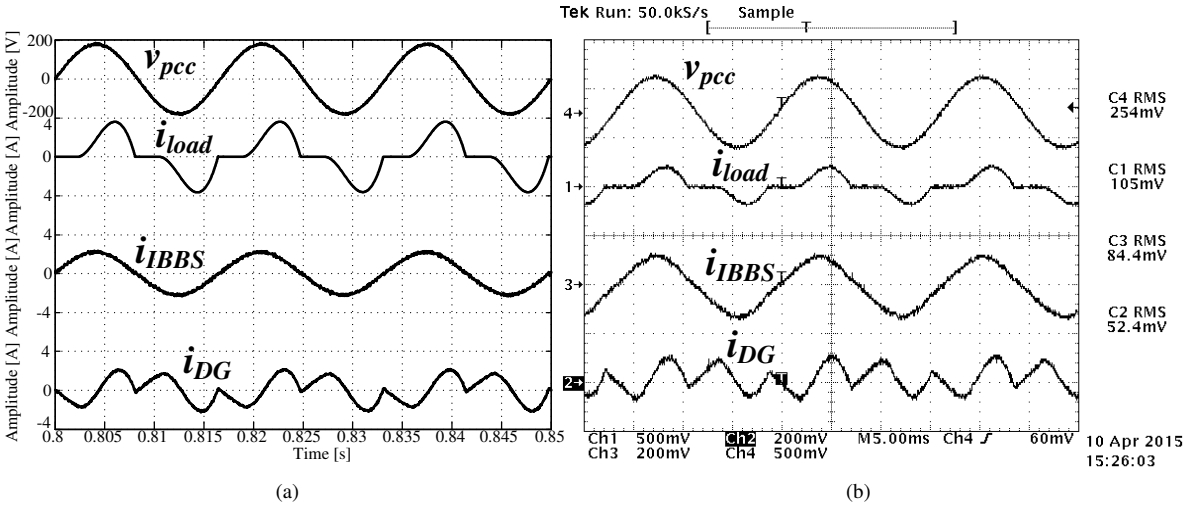


Figure 6:42 - Results for the DG operating as active filter. (a) Simulation and (b) Experimental (Ch1, Ch2, Ch3: 0.1V/A; Ch4: 0.5V/V).

6.13 Smart micro-grid prototype

Figure 6:43 presents the smart micro-grid prototype built to verify the proposed IBBS. Its details are presented in Appendix G.

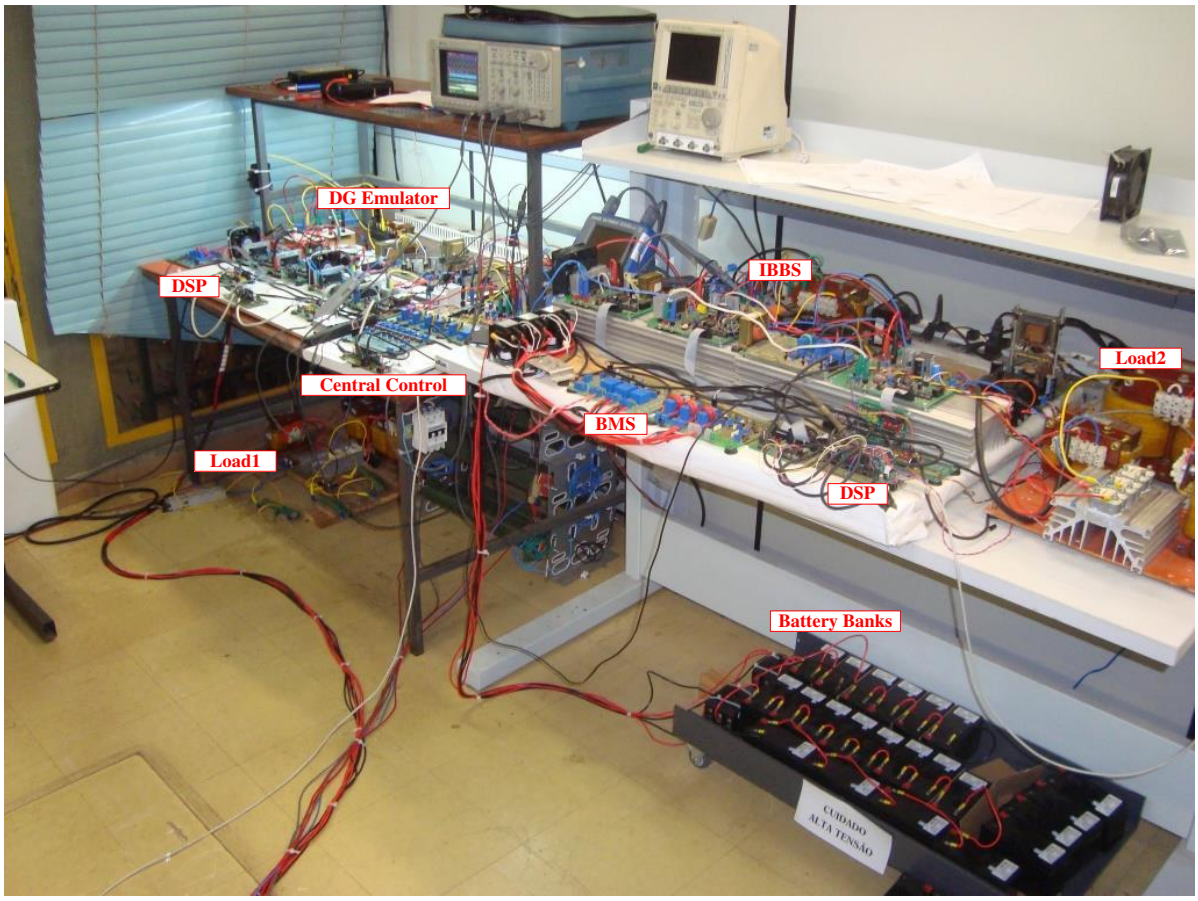


Figure 6:43 - Smart micro-grid prototype built to verify the proposed IBBS.

6.14 Extension to three-phase system

The proposed IBBS may be extended to three-phase system. However, some features for three-phase system may be included. One of them is the load balance compensation. This section presents how this feature is performed on the IBBS. For better visualization, the IBBS is set to operate simultaneously as active filter [77].

Figure 6:44 presents the IBBS connected to a three-phase system. The system is composed by the main generation and by single- and three-phase loads. The configuration of the loads makes the grid current unbalanced.

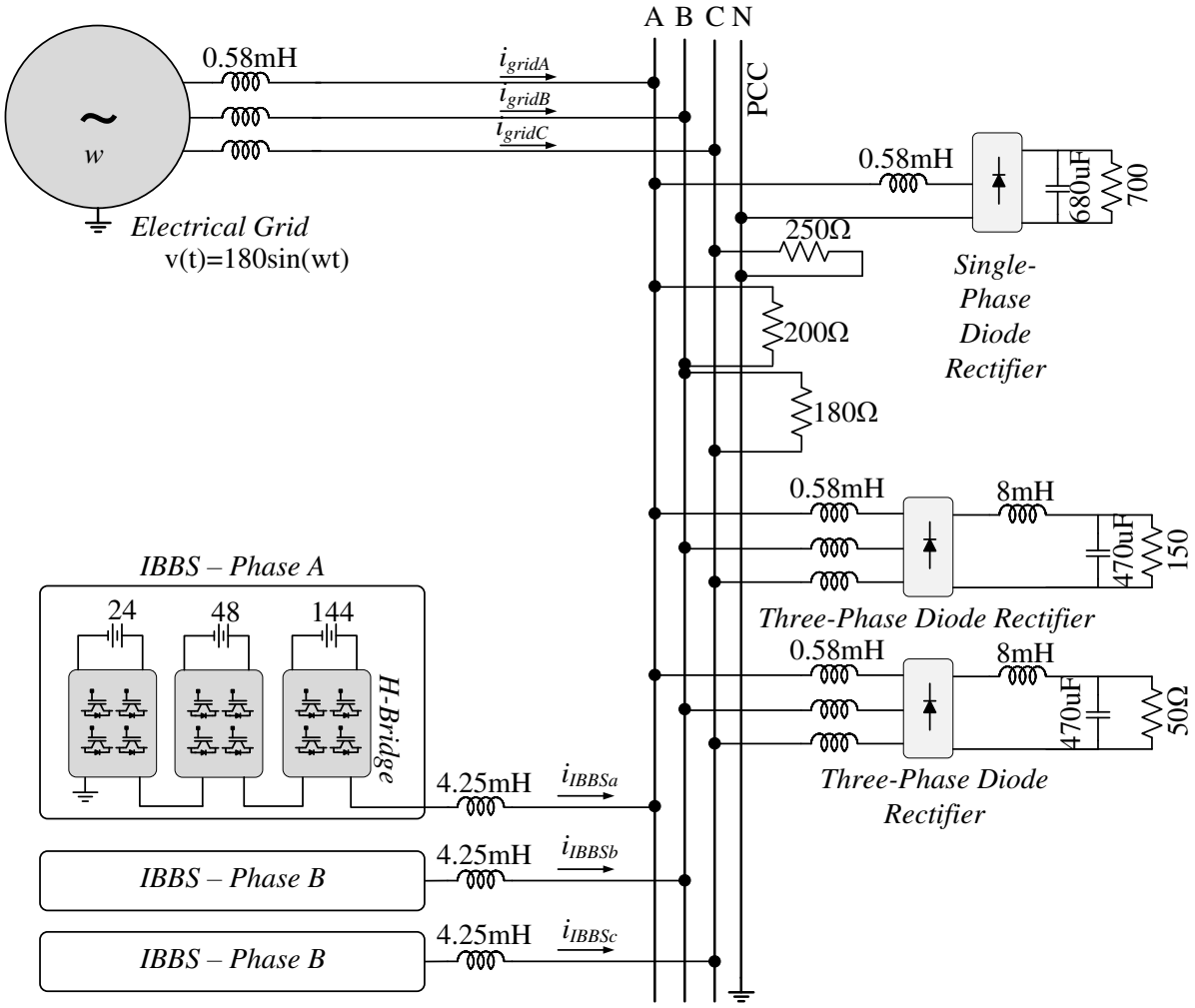


Figure 6:44- The IBBS connected to a three-phase system.

In order to obtain the IBBS current reference for unbalance compensation, the CPT is used [77].

The three-phase active current is given by (6.34).

$$i_{a(a,b,c)} = \frac{\left\langle v_{(a,b,c)}, i_{(a,b,c)} \right\rangle}{\left\| v_{(a,b,c)} \right\|^2} v_{(a,b,c)} \tag{6.34}$$

The three-phase reactive current is given by (6.35).

$$i_{r(a,b,c)} = \frac{\left\langle \hat{v}_{(a,b,c)}, i_{(a,b,c)} \right\rangle}{\left\| v_{(a,b,c)} \right\|^2} \hat{v}_{(a,b,c)} \tag{6.35}$$

The three-phase void current is given by (6.36).

$$i_{v(a,b,c)} = i_{(a,b,c)} - i_{a(a,b,c)} - i_{r(a,b,c)} \tag{6.36}$$

The three-phase active balanced current is given by (6.37).

$$i_{abal(a,b,c)} = \frac{\left\langle v_a i_a \right\rangle + \left\langle v_b i_b \right\rangle + \left\langle v_c i_c \right\rangle}{\left\| v_a \right\|^2 + \left\| v_b \right\|^2 + \left\| v_c \right\|^2} v_{(a,b,c)} \tag{6.37}$$

The three-phase reactive balanced current is given by (6.38).

$$i_{rbal(a,b,c)} = \frac{\langle \hat{v}_a i_a \rangle + \langle \hat{v}_b i_b \rangle + \langle \hat{v}_c i_c \rangle}{\|\hat{v}_a\|^2 + \|\hat{v}_b\|^2 + \|\hat{v}_c\|^2} \hat{v}_{(a,b,c)} \tag{6.38}$$

The unbalance compensation current is given by (6.39).

$$i_{ba(a,b,c)} = i_{a(a,b,c)} - i_{abal(a,b,c)} + i_{r(a,b,c)} - i_{rbal(a,b,c)} \tag{6.39}$$

For unbalance compensation, it is sufficient to add to the IBBS current reference the equation (6.39).

Figure 6:45 presents simulation results for the PCC voltage and the grid current for load unbalance compensation. Initially, the IBBS is turned off. The grid current is the sum of the load current. It is highly distorted and unbalanced. At t = 0.25s the IBBS turns-on. The IBBS initially is operating as active filter without unbalance compensation. The grid current is sinusoidal and in-phase to the PCC voltage. The grid current presents different amplitude for each phase. At t = 0.3 s, the IBBS begins to compensate the unbalance. The grid current becomes balanced.

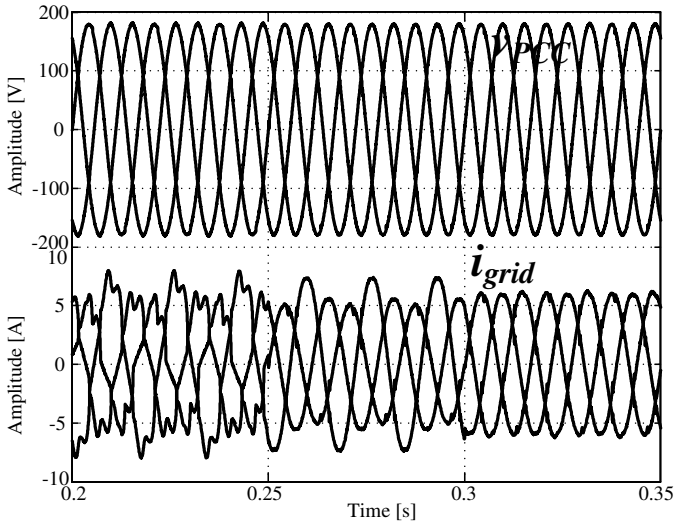


Figure 6:45 – Simulation results for the PCC voltage and the IBBS current for load unbalance compensation.

7 CONCLUSIONS

7.1 General Conclusions

This thesis presented the study and development of multilevel inverters for intelligent distribution system. The symmetrical and asymmetrical topologies were studied. Concepts about the structure, the modulation, the power distribution across the modules, the output filter, the current and voltage controller, among others, were presented. Simulation and experimental were presented in order to verify the studies.

The SCMI topology presented a linear distribution of the processed power across the modules. This feature makes the SCMI topology an attractive choice in applications covering non-active power handling, such as STATCOMs and active filters. The control techniques from the classical H-bridge converter are easily expanded to SCMI.

The ACMI topology presented a nonlinear distribution of the processed power across the modules. Additionally, a regenerative process can occur depending on the modulation index. This feature makes the ACMI topology technically unfeasible for a variety of applications. However, this thesis showed some possibilities to apply the ACMI topology in BBS system connected to low distribution voltage without the need of changing the physical structure.

The features found in both topologies were compared side-by-side in a three module configuration. Applications dealing with storage applied in medium voltage are more prone to be made by the SCMI topology. The main reasons are the modularity and the possibility to keep the storage working even under occurrence of fault. The ACMI topology is suited for applications in low voltage, where the efficiency and the emission of electromagnetic radiation is the main concern. The processing of the major part of the total power in 60 Hz and a reduced output filter are reasons to justify their usage. Residential storages and compensators for avionic systems are example of applications aiming the abovementioned concerns.

A proposal of an IBBS system was presented. The interaction made the BBS to operate coordinately to local and centralized controllers and to perform ancillary functions. Moreover, the IBBS system in conjunction to another interactive distributor power element resulted in a synergist operation of the grid. Concepts about smart-grids were also presented in order to clarify how the interaction contributes to the smart-grid realization.

The proposal was verified through a BBS built in an ACMI, but it is equally applied to any other BBS topology. A variety of scenarios was evaluated, such as the IBBS

performing ancillary functions, communicating to a central controller, compensating the intermittent behavior of a wind based DG and supporting a starting process of a squirrel-cage induction motor. Simulation and experimental results showed the efficacy of the proposed IBBS.

The studies of multilevel topologies and the proposed IBBS presented in this thesis contribute to the smart-grid realization. Interactive storage is a promising technology and will play an important role in smart-grids. A variety of algorithms may be aggregate to the IBBS, considering relevant aspects like price of energy, weather changes and political concerns. Additionally, the ICT allows the communication to central and local controllers, enhancing the reliability, the stability, the uninterrupted supply capability of smart-grids.

7.2 Suggestions for future work

The research project presented in this thesis can be expanded. This section presents some suggestions for future work.

The batteries should be better considered in the IBBS project. The SOC and SOH were the only parameters used and they were estimated in a simplified manner. The suggestion is to build a more sophisticated BMS, able to get accurate values and to manage the incoming power in the batteries from the grid.

The literature lacks of a methodology to control the DC-link voltages in the ACMI topology. The suggestion is to develop a methodology to control such voltage, independently of the existent load and without using parallel resistors. Moreover, the implementation of a bidirectional high-frequency module to replace the lower is also suggested.

Another suggestion is to employ more functions into the IBBS, such as load peak shaving, voltage regulation and islanding mode capability. Additionally, there is a necessity to deeper evaluate how the central and local controller take decision. In section 8.11, the local controller took decision randomly.

Final suggestions are to adapt the IBBS to operate in ring grids and to build a parallel DC grid. The DC grid would be connected to the presented smart micro-grid through a DC-AC converter. Then, power can be transferred through the grids in order to achieve an optimized operation of whole system.

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APPENDIX A - MULTILEVEL TOPOLOGIES

Besides the SCMI and ACMI, there are other multilevel topologies with a broad field of application. This appendix briefly presents some of these topologies.

A.1 Diode-Clamped

Figure A:1 presents the Diode-Clamped topology with three levels at the output voltage [111]–[114]. This topology arose from the conventional two level inverters, where the addition of clamped diodes and transistors makes the output voltage to have more levels. There is only one DC source and it is equally divided into two capacitors. Its common point is defined as the neutral. The output voltage can present three values, related to neutral. They are: +Vc/2, 0 and –Vc/2. Each transistor and diode must hold one half of the VDC voltage.

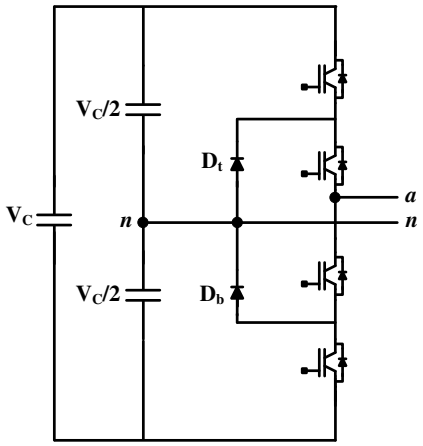

Figure A:1 - Diode-Clamped topology with three levels at the output voltage.

By properly adding more diodes and transistors, the five-level topology is achieved [115], [116]. Figure A:2 present the diode-clamped topology with five levels. The Vdc voltage is equally divided into four capacitors. Each transistor must hold one fourth of the Vdc voltage while there are diodes which hold one fourth, two fourth and three fourth of the Vdc voltage. The diodes D3 and D4, and D2 and D5, can be replaced by two and three series diodes, respectively. Then, each diode holds one fourth of the Vdc voltage.

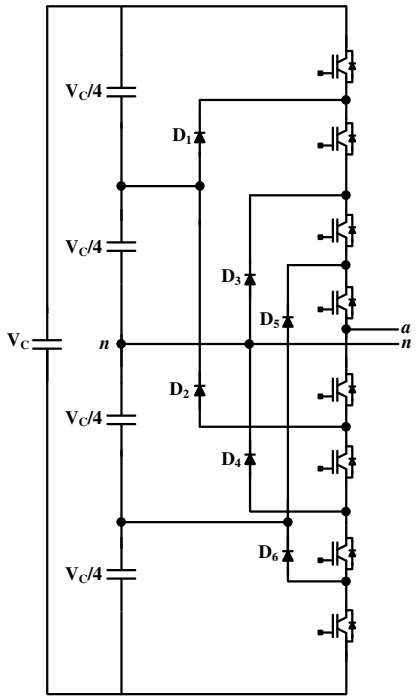

Figure A:2 - Diode-clamped topology with five levels.

Disadvantages of the diode-clamped topology are the complexity of implementation, the voltage unbalance found on the capacitors [112],[117] and problems associated to the diode recovery current [118].

A.2 Pyramidal Diode-Clamped

Other topologies based on the diode-clamped were proposed in the literature in order to enhance the original performance. One of them is the pyramidal diode-clamped topology [119],[120]. Figure A:3 presents the pyramidal diode-clamped topology with seven levels. The difference between this topology and the previous one is the location of the clamped diodes. Each transistor and diode is under one-sixth of the VDC voltage. Therefore, the diodes and transistors are equally sized in voltage.

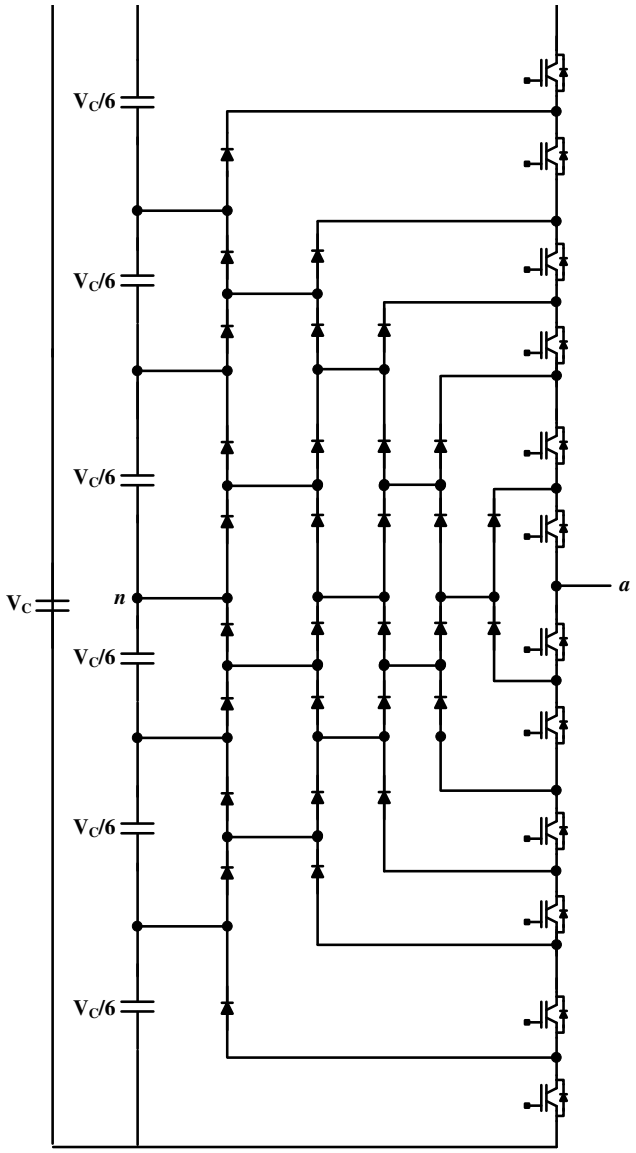

Figure A:3 - Pyramidal diode-clamped topology with seven levels.

A.3 Flying capacitor

Figure A:4 presents the flying capacitor topology with three levels [121], [122]. The VDC voltage is equally divided into two capacitors. The Capacitor C1 is responsible to clamp the voltage. Each transistor must hold one half of the VDC voltage. An advantage of the flying capacitor topology over the diode-clamped is the fact that the voltage across the transistor is directly clamped, avoiding occurrence of overvoltage.

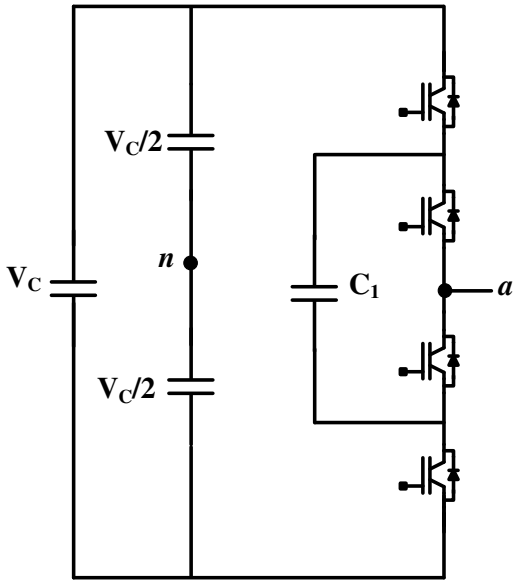

Figure A:4 - Flying capacitor topology with three levels.

Figure A:5**Error! Reference source not found.** presents the flying capacitor topology with five levels. The VDC is still divided into two equal parts.

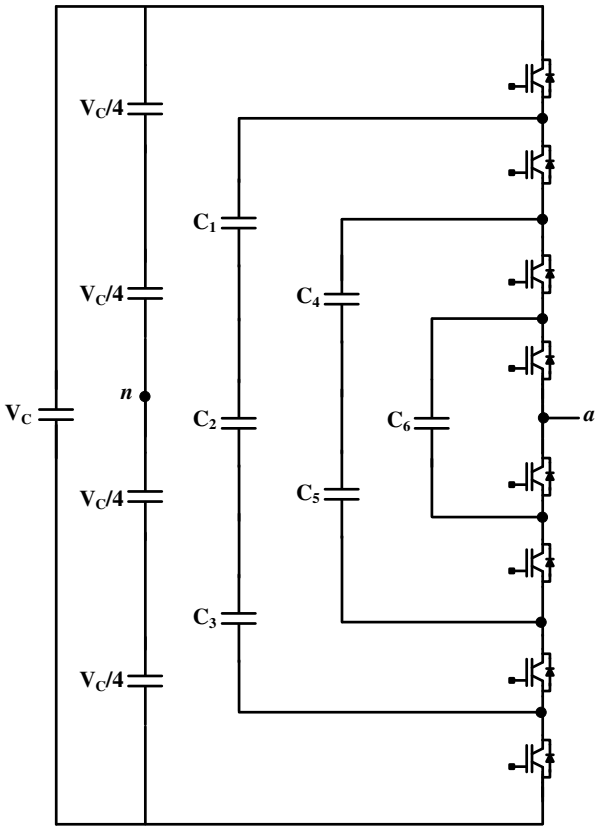

Figure A:5 - Flying capacitor topology with five levels.

A disadvantage of the flying capacitor topology is the necessity of a robust control strategy to keep the clamped capacitor voltages stable at the set-point. Moreover, the start-up process requires the implementation of a pre-load technique in order to avoid overcurrent.

A.4 Modular

The Modular Multilevel Topology (MMT) is a cascaded structure with several cells [123]–[126]. Figure A:6 presents the MMT with *n* cells. Each cell is composed by an H-bridge converter. Other topologies could be used within the cells.

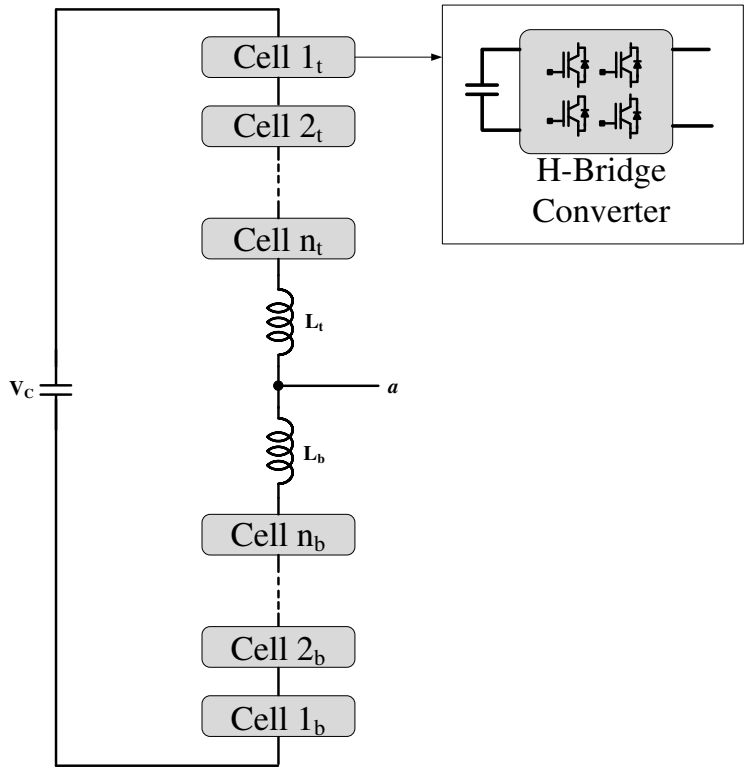

Figure A:6 - Modular multilevel topology with *n* cells.

The main advantages of MMT are the use of only one DC source and the modularity. Capacitor voltage control and circulating current are drawbacks of this topology [127], [128].

A.5 Hybrid topologies

Hybrid topologies can be achieved by combining classical converter topologies [129]–[133]. Figure A:7 presents a hybrid multilevel inverter made by the combination of the flying capacitor topology and the symmetrical cascaded.

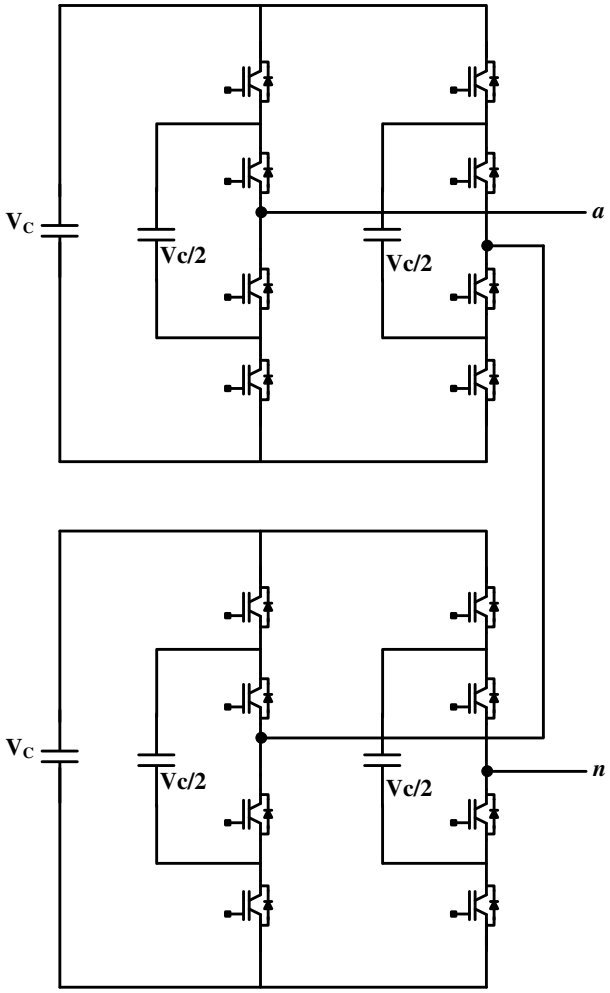

Figure A:7- Hybrid multilevel inverter made by the combination of the flying capacitor and the symmetrical cascaded.

Figure A:8 presents the three-phase hybrid multilevel inverter made by a three-phase diode-clamped topology and the symmetrical cascaded [134].

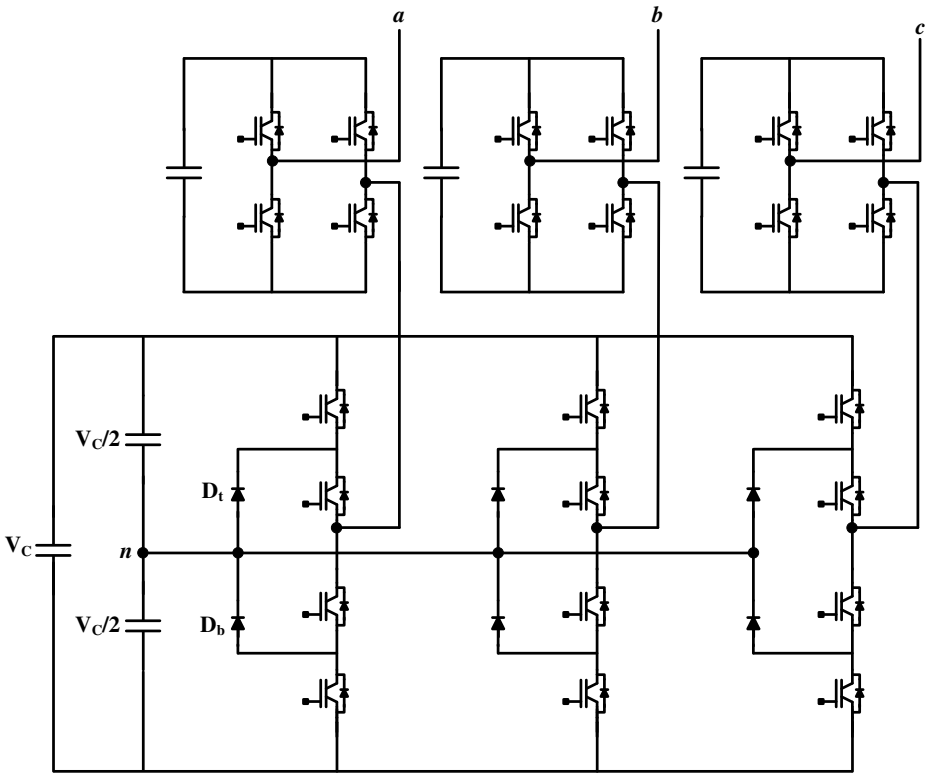

Figure A:8 - Three-phase hybrid multilevel inverter made by a three-phase diode-clamped and the symmetrical cascaded.

APPENDIX B - STORAGES

The use of renewable energy for distributed generators is increasing considerably nowadays. Reports have demonstrated that generators based on renewables will represent a meaningful percentage of the total world energy production, with a prediction of around 80% by 2050 in United States [135]. Technologies involved with renewables are also expected to have potential growth in order to beneficiate all the electric system. One of them, and one of the most indispensable for supporting the intermittent behavior of renewable energy, is storage systems.

There are several manners to store energy. Some examples are batteries, compressed air, flywheel, capacitor, supercapacitor and pumped hydro [136]–[140]. The criteria to choose the storage technology usually are lifetime, life-cycle, power and energy density, self-discharging rates, environmental impact, efficiency and cost.

Pumped hydro system are by far the most widely used, with more than 127,000 MW installed worldwide. Compressed air energy storage installations are the next largest, followed by Sodium-Sulphur batteries. All remaining energy storage resources worldwide total less than 85 MW combined. Figure B:1 presents the worldwide installed storage capacity for electrical energy, by the end of 2010.

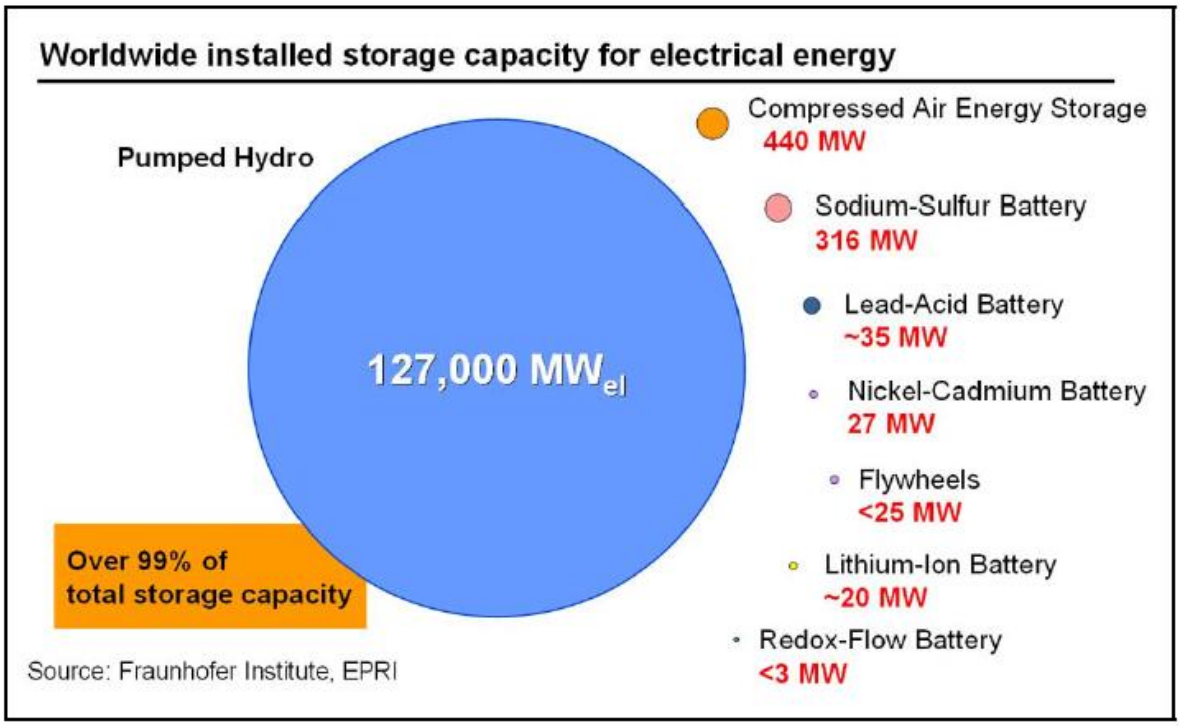

Figure B:1 - Worldwide installed storage capacity for electrical energy [141].

Storage applications may be divided into two groups: power and energy. Storage for power applications has relative high power density and can supply power for long timescale, for instance, some hours. Pumped hydro and batteries are some example of power storage. They are suited for bulk systems. On the other hand, storage for energy applications has low power density and they have higher time response compared to the previous. Supercapacitors are an example of energy storage. Figure B:2 presents the characteristics of various energy storage technology options in terms of system power rating along the duration of discharge time.

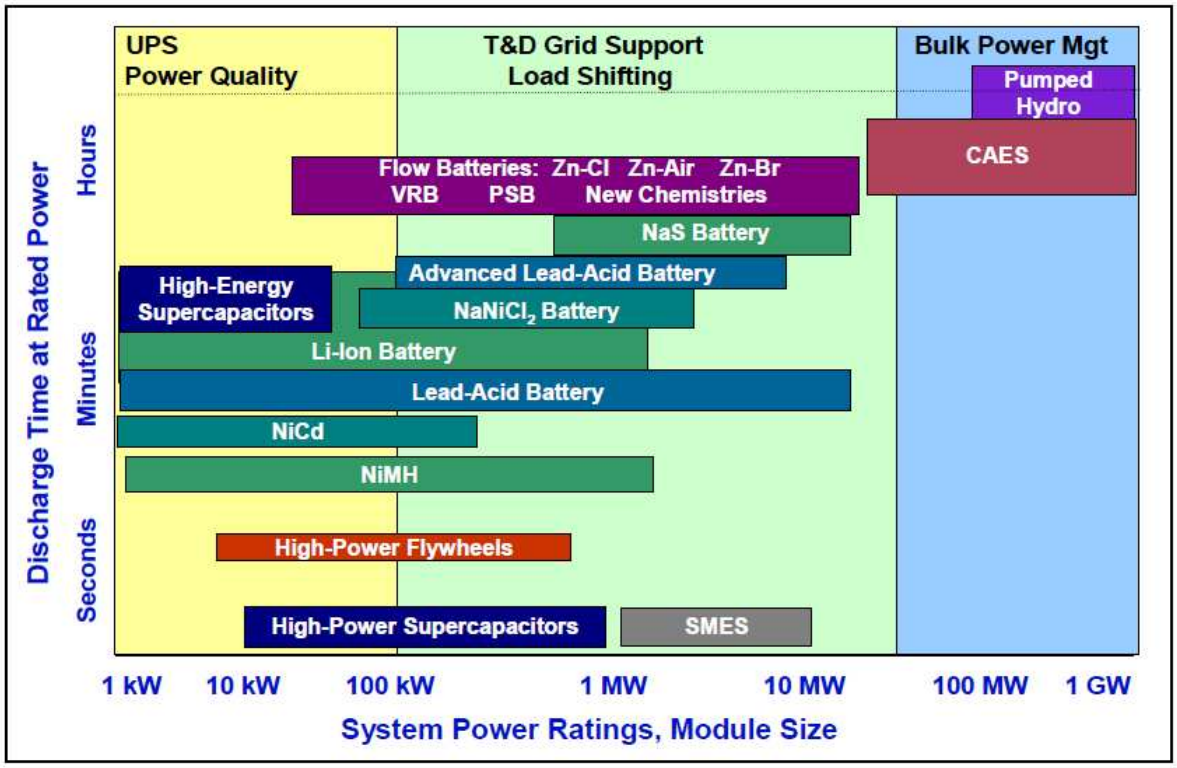

Figure B:2 - Characteristics of various energy storage technology options in terms of system power rating along the duration of discharge time [141].

Some technologies found in B:2 are presented as follow.

B.1 Pumped Hydro

Pumped Hydro Storage stores potential energy from height difference in water levels. They are different form a conventional hydroelectric power plant because they have the ability to pump water from the lower reservoir to the upper. Pumped hydro storage represents approximately 3% of the total world installed power capacity and 97% of total storage capacity [142].

Some features of pumped hydro storage are efficiency around 65 to 85%, large power capacity (100 – 1,000 MW), large storage capacity (1 – 24 hours), long life (30 – 60

years), low cycle cost, high capital cost and project lead time around ten years. Pumped hydro storage causes environmental damages by flooding and they are not attractive for renewable applications due to its low time response.

B.2 Compressed air (CAES)

Compressed air storage systems usually use an existing underground site, like rock cavern and abandoned mines, to storage gas [143]–[146]. Some features of compressed air storage are large energy storage capacity (2 – 50 hours), efficiency around 60 – 80%, lower capital cost compared to pumped hydro, cause little environmental impact and have low energy density. But the major drawback of compressed air storage is to find favorable locations for new facilities.

B.3 Battery

Batteries have the ability to store energy through a reversible chemical reaction. The most common chemistry technologies found in batteries are: lead-acid, nickel-cadmium, sodium-Sulphur, lithium-ion and zinc-bromine. Brief description of each one is given as follow.

B.3.1 Lead-acid

Lead-acid batteries have been used for more than 130 years [147]. Lead acid batteries have high reliability, low cost, strong surge capability, efficiency around 65 to 80 %. They are attractive for UPS, power quality devices and for spinning reverse applications. However, they have short life (500 – 1,000 cycles), require regular maintenance, they are poor for energy management purpose, have low energy density, have poor performance at cold temperatures and emit explosive gas and acid fumes [87], [148]–[150].

B.3.2 Nickel-Cadmium

Nickel-cadmium batteries are attractive for UPS and generator-starting applications [151], [152]. However, the sales of these batteries declined for the period of 1995 to 2003, motivated mainly by the increasing environmental controls for toxic cadmium. Nickel-cadmium batteries have high energy density and long life (2000 – 2500 cycles). They have high cost and suffer from memory effect. If they are not fully discharged before being recharged, the battery starts losing is capacity [153], [154].

B.3.3 Sodium-sulphur

Sodium-Sulphur batteries are the most promising technology for variable renewable energy sources, such as wind and solar power. In the past decades, installations based on sodium-sulphur grew exponentially from 10 MW in 1998 to 305 MW at the end of 2008 [6].

Sodium-sulphur batteries can be cycled 2500 times, have high power density, have general capacity around 1MW and have efficiency around 75 – 90%. Additionally, they are environmentally benign and 99% of the overall weight of the battery material can be recycled [155], [156]. The drawbacks of sodium-sulphur batteries are the high capital cost the necessity to keep the internal temperature around 350 °C.

B.3.4 Lithium-ion

Lithium-ion batteries were commercialized by Sony in 1991 [6]. Rapidly, the demand for these batteries has grown drastically in several markets. This is due to the many desirable characteristics these batteries have, as efficiency around 95%, long life cycle (3000) and high energy and power densities [157]–[162]. Such features have made the lithium-ion batteries the best choice for portable electronics applications. The main hurdles of theses batteries are the high cost, making them unattractive for installation in bulk system. They need also circuitry for safety and protection.

B.3.5 Zinc-Bromine

Zinc-bromine batteries are a special type of technology, called flow batteries. The battery stores at least one of its liquid electrolytes in an external storage tank that flows through the reactor to store/create electricity. As a result, the energy storage can be independent of the power capacity, depth-of-discharge can be ignored and self-discharged is negligible. Moreover, zinc-bromine batteries have response time in milliseconds scale, low cost, efficiency around 75%, life of around 2000 cycles and 3 to 4 hour charging time.

Several battery storages are currently working worldwide. Table B.0:1 presents some battery storage systems installed in the world.

Table B.0:1 - Some battery storage systems installed in the world.

Battery Energy Storage System	Location	Capacity	Battery	Application	Year
BEWAG AG [163]	Berlin, Germany	17MW / 14MWh	Lead Acid	Spinning reverse, frequency control	1986
Kansai Electric Power Co., Inc [164]	Tatsumi, Japan	1 MW / 4 MWh	Lead Acid	Multipurpose demonstration	1986
South Carolina Edison (SCE) [165]	Chino, CA, USA	10 MW / 40 MWh	Lead Acid	Multipurpose demonstration	1988
Puerto Rico Electric Power Authority (PREPA) [166]	San Juan, PR, USA	20 MW / 14 MWh	Lead Acid	Spinning reverse, frequency control, voltage regulation	1994
GNB Technologies [167]	Vernon, CA, USA	5 MW / 2.5 MWh	Lead Acid	UPS, peak shaving	1995
Golden Valley Electric Association (GVEA) [168]	AK, USA	40 MW / 14 MWh	Nickel Cadmium	Spinning reverse, frequency control, voltage regulation	2003
Tokyo Electric Power Co., Inc (TEPCO) [169]	Hitachi, Japan	8 MW / 58 MWh	Sodium Sulphur	Load Leveling	2004
EaglePitcher Technology	KS, USA	60 MWh	Lithium-ion	Frequency regulation, grid stabilization	2009

B.4 Flywheels

A flywheel is a mass that stores energy according to its change in rotational velocity [170], [171]. It is also a promising technology mainly due to its long life (15 – 20

years), long cycle life (10,000 to 100,000) and efficiency around 95%. The main drawback of flywheels is the high capital cost.

Although flywheels are not yet widespread in the electrical sector, they are slowly penetrating the market, mostly for UPS, power conditioning, pulse power and with renewable source technology applications [172], [173].

B.5 Capacitor and supercapacitors

Capacitor and supercapacitors store energy by accumulating positive and negative charges. They can be charged substantially faster than conventional batteries and can be cycled over 100,000 times. However, they have low energy density. They are suited for fast cycling applications [174]–[178].

Capacitors accumulate charges on parallel plates separated by a dielectric. They last approximately 5 years, and have 60 to 70% of cycle efficiency. In power system, they are typically used for power factor correction and voltage regulation.

Supercapacitors usually store energy by means of an electrolyte solution between two solid conductors. They have a durability of 8 to 10 years, efficiency around 95%, have deep discharge and overcharge capability and high energy dissipation rate (5 – 40%).

APPENDIX C - DETAILS ABOUT THE SIMULATION OF THE SCMI

This appendix presents details about the simulation of the SCMI. The simulation file is freely available on https://sites.google.com/site/busarellosmartgrid/home.

Figure C:1 presents the circuits for the grid, the PCC and the load. The PCC is the point where the SCMI is connected.

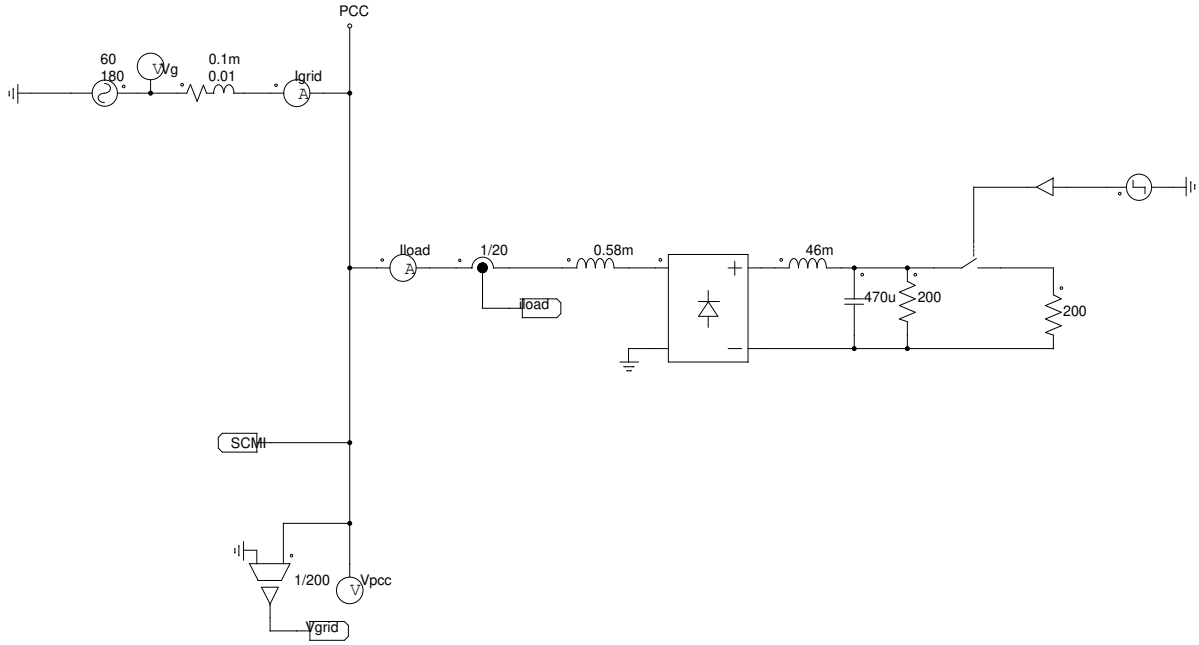

Figure C:1 - Circuits for the grid, the PCC and the load.

Figure C:2 presents the circuit for SCMI.

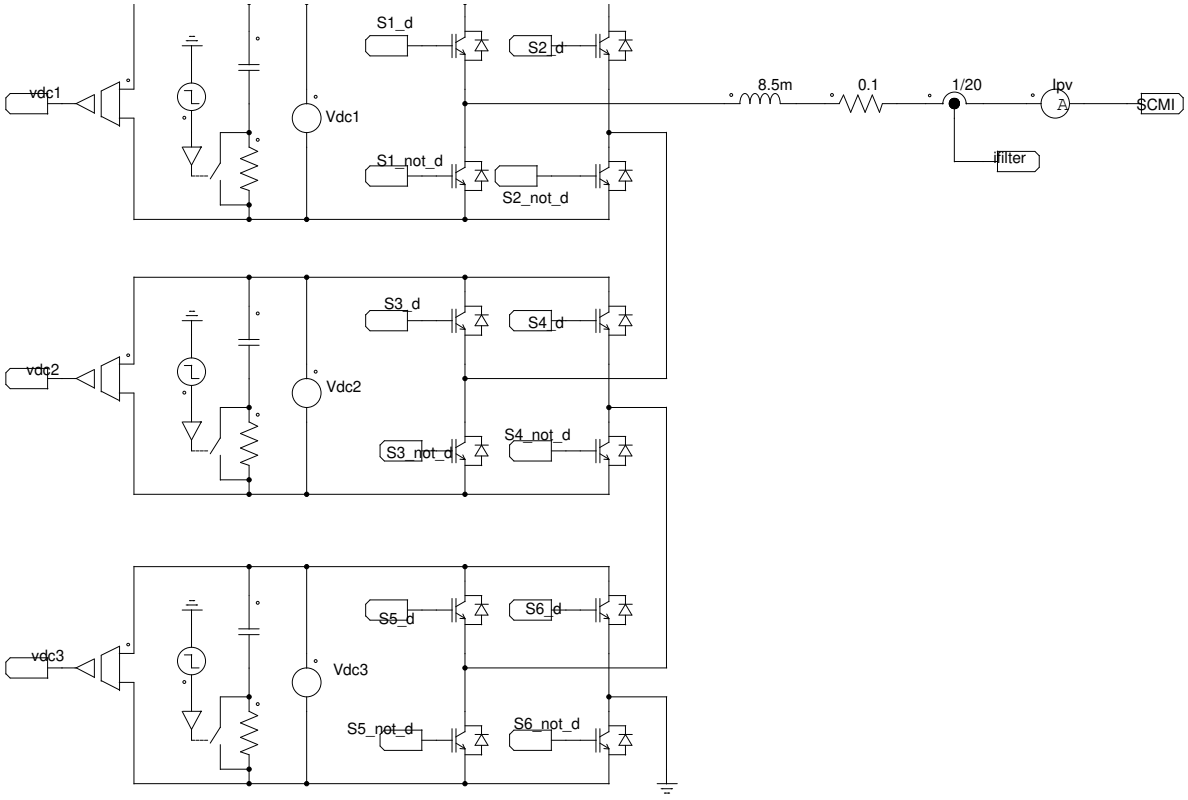

Figure C:2 - Circuit for the SCMI.

Figure C:3 presents the circuits for ADC converter and the PLL.

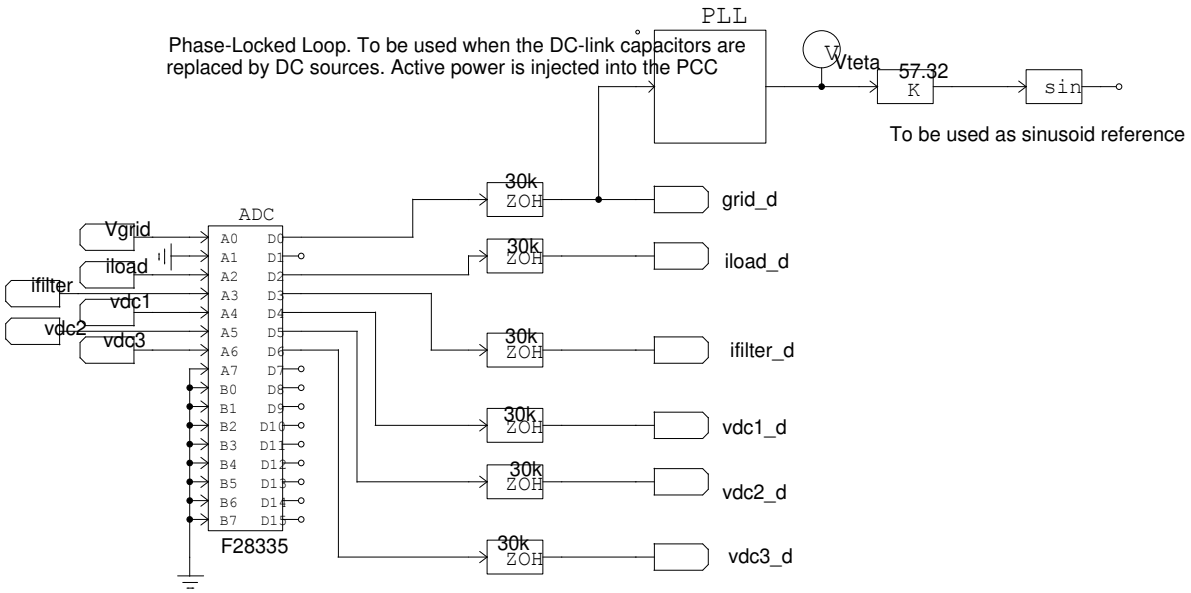

Figure C:3 - Circuits for ADC converter and the PLL.

Figure C:4 presents the circuits for the CPT used in the SCMI.

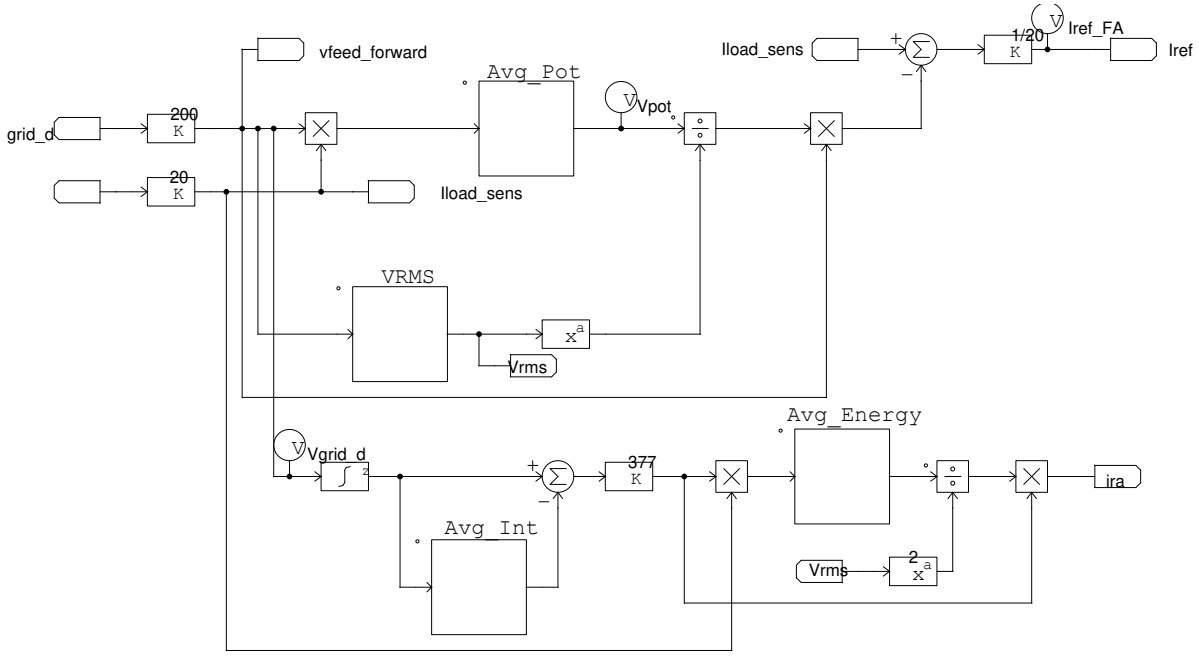

Figure C:4 - Circuits for the CPT used in the SCMI.

Figure C:5 presents the circuits for the current controller.

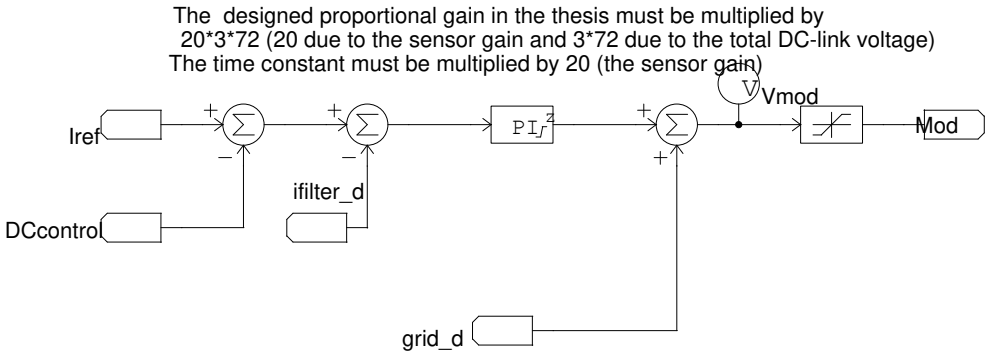

Figure C:5 - Circuits for the current controller.

Figure C:6 presents the circuits for the DC-link control.

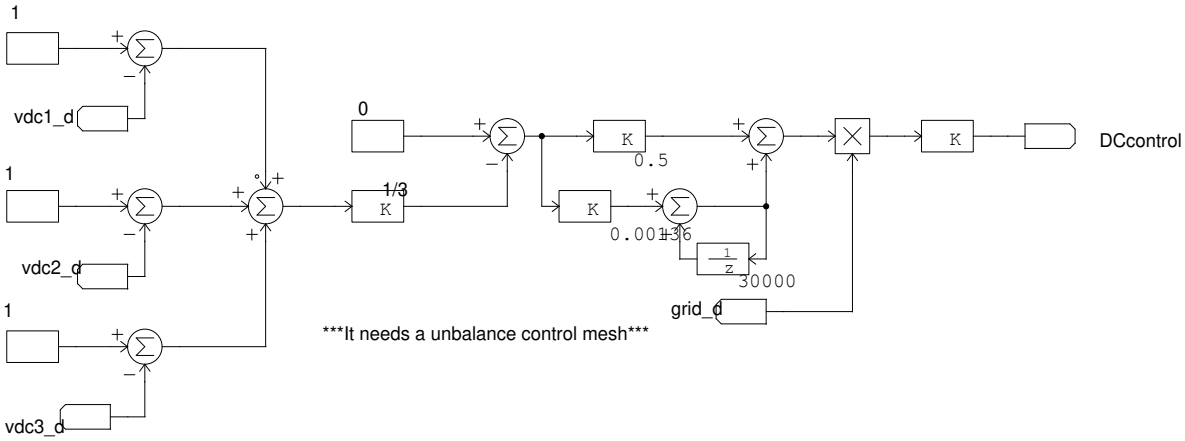

Figure C:6 - Circuits for the DC-link control.

Figure C:7 presents the circuits carriers and the PWM generators.

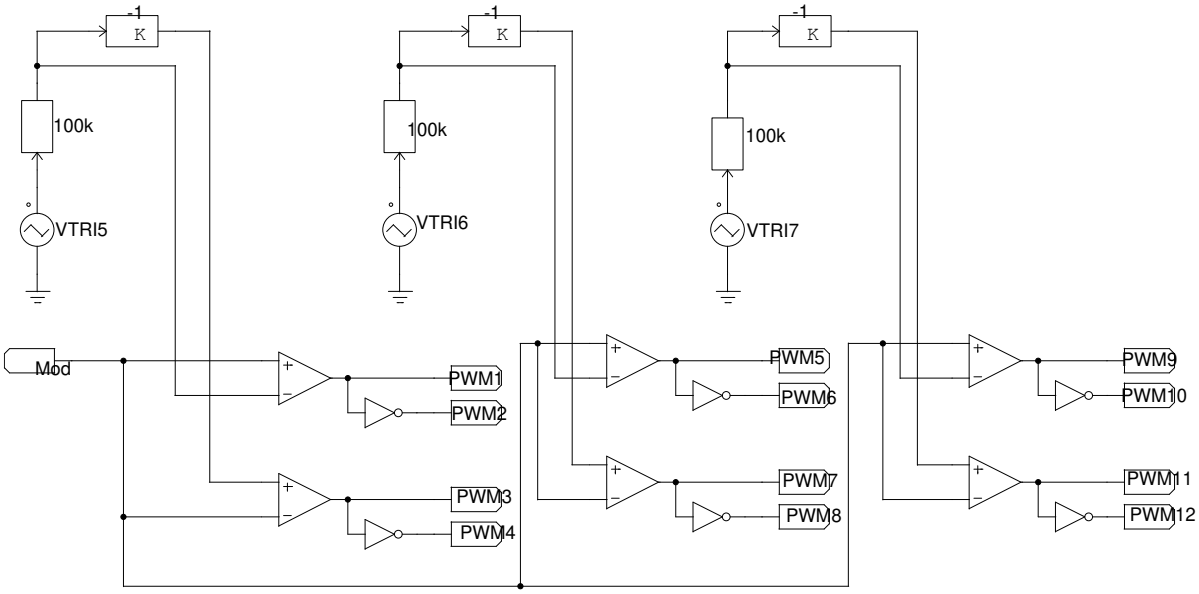

Figure C:7 - Circuits carriers and the PWM generators.

Figure C:8 presents the circuits for the digital outputs.

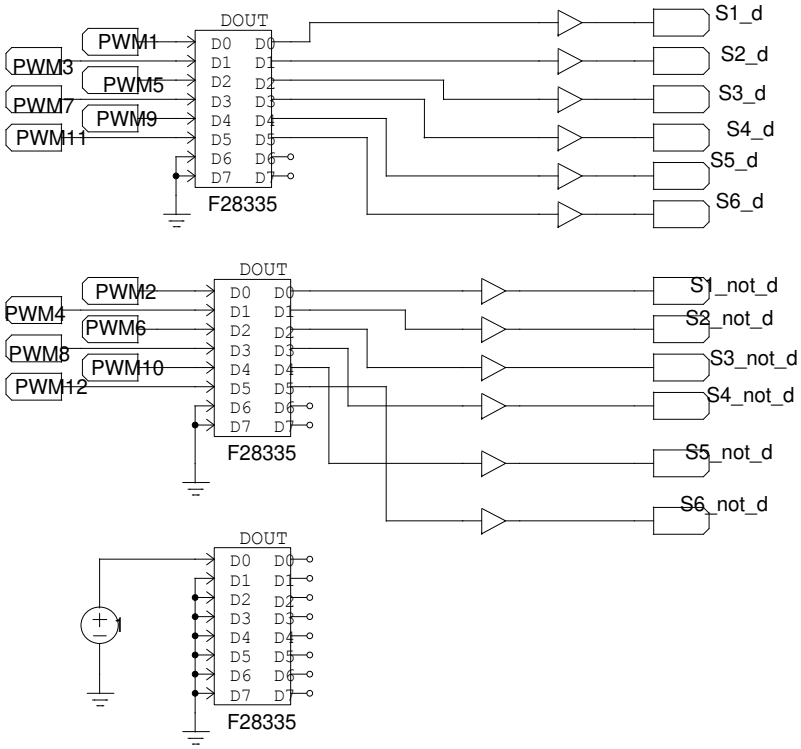

Figure C:8 - Circuits for the digital outputs.

APPENDIX D - HOW THE EFFECT OF A DISTURBANCE CAN BE MINIMIZED IN A CLOSED-LOOP SYSTEM

Equation (3.25) has a term associated to the load current which is considered a disturbance. The effect of a disturbance can be minimized by an appropriate methodology. This appendix present how and a disturbance can be minimized in a closed-loop system. Figure D.1 presents a generic closed-loop system with disturbance. *G(s)* is the system plant, *H(s)* is the feedback transfer function and *D(s)* is the disturbance.

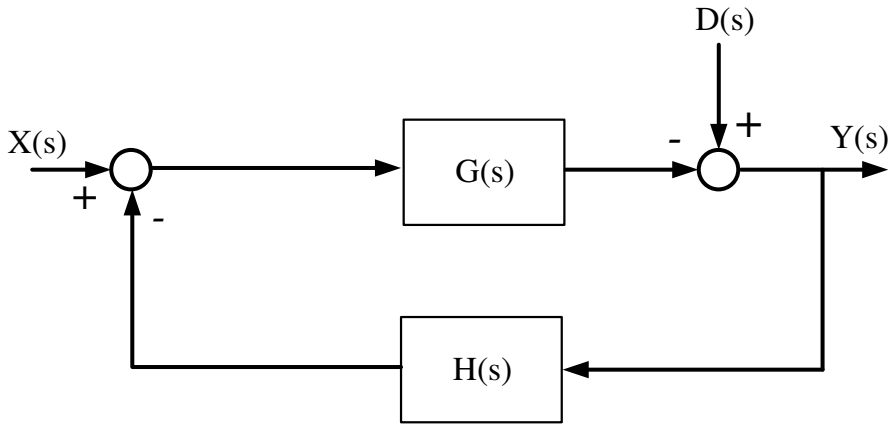

Figure D.1 - Generic closed-loop system with disturbance.

The product of the system plant by the feedback transfer function is given by (D.1).

$$T(s) = G(s)H(s) \tag{D.1}$$

By applying the superposition technique to the generic system, the output signal is given by (D.2).

$$Y(s) = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} X(s) + \frac{1}{1+T(s)} D(s) \tag{D.2}$$

The effect of the disturbance can be minimized by increasing the gain at *T(s)*. Equation (D.3) illustrates how the increase of the gain of *T(s)* minimizes the disturbance. With high gain, the denominator of the term associated to the disturbance tends to infinite. Consequently, the effect of the disturbance is minimized.

$$\frac{1}{1+T(s)} \approx \begin{cases} \frac{1}{T(s)}; & 0 \quad \text{for } |T(s)| \gg 1 \\ 1 & \text{for } |T(s)| = 1 \end{cases} \tag{D.3}$$

The action of increasing the gain in *T(s)* also benefits the term associated to the input. Equation (D.4) illustrates how the term associated to the input is beneficiated by the increase of the gain.

$$\frac{T(s)}{1+T(s)} \approx \begin{cases} 1 & \text{for } |T(s)| \gg 1 \\ T(s) & \text{for } |T(s)| = 1 \end{cases} \tag{D.4}$$

Therefore, high gain at *T(s)* tends the closed-loop system to present unitary gain. Consequently, the steady-state error tends to be null. The gain of *T(s)* can be increased by increasing the proportional gain of the controller associated to the system plant.

APPENDIX E - DETAILS ABOUT THE SIMULATION OF THE ACMI

This appendix presents details about the simulation of the ACMI. The simulation file is freely available on https://sites.google.com/site/busarellosmartgrid/home.

Figure E:1 presents the circuits for the grid, the PCC and the load.

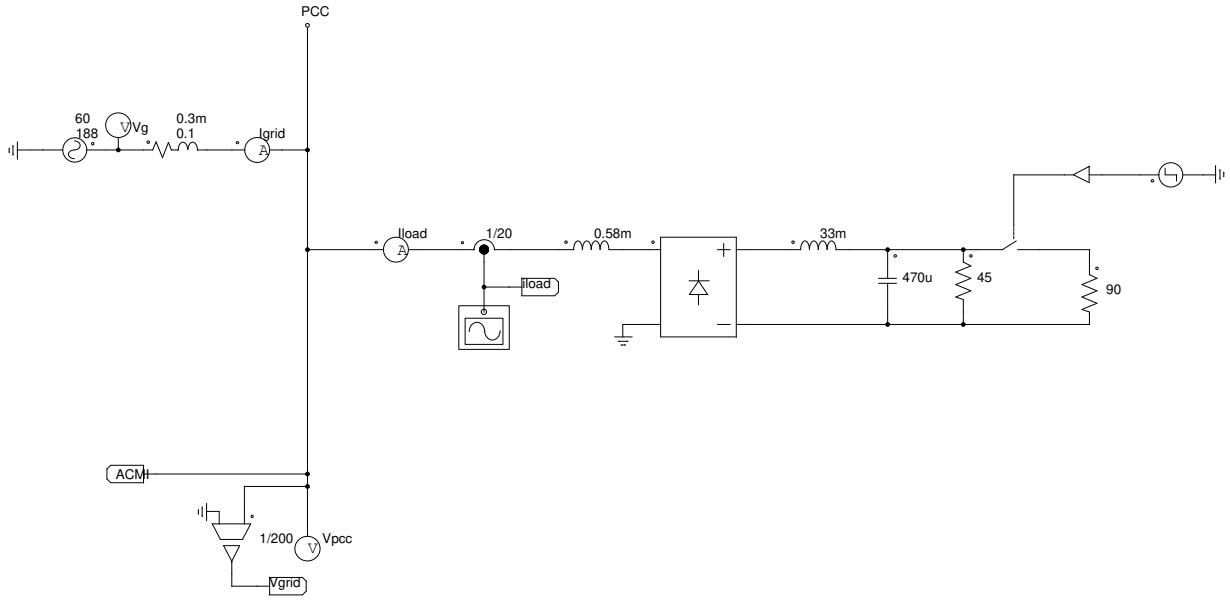

Figure E:1 - Circuits for the grid, the PCC and the load.

Figure E:2 presents the circuit for the ACMI.

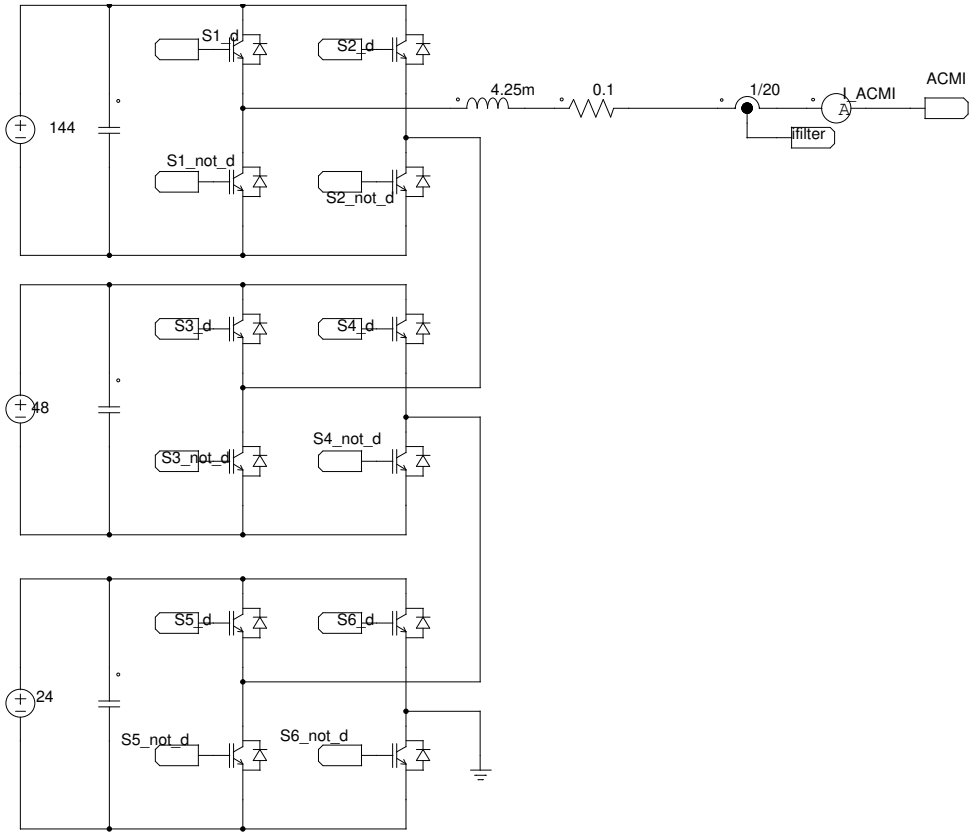

Figure E:2 - Circuit for the ACMI.

Figure E.3 presents the circuits for the ADC converter, the PLL and the CPT.

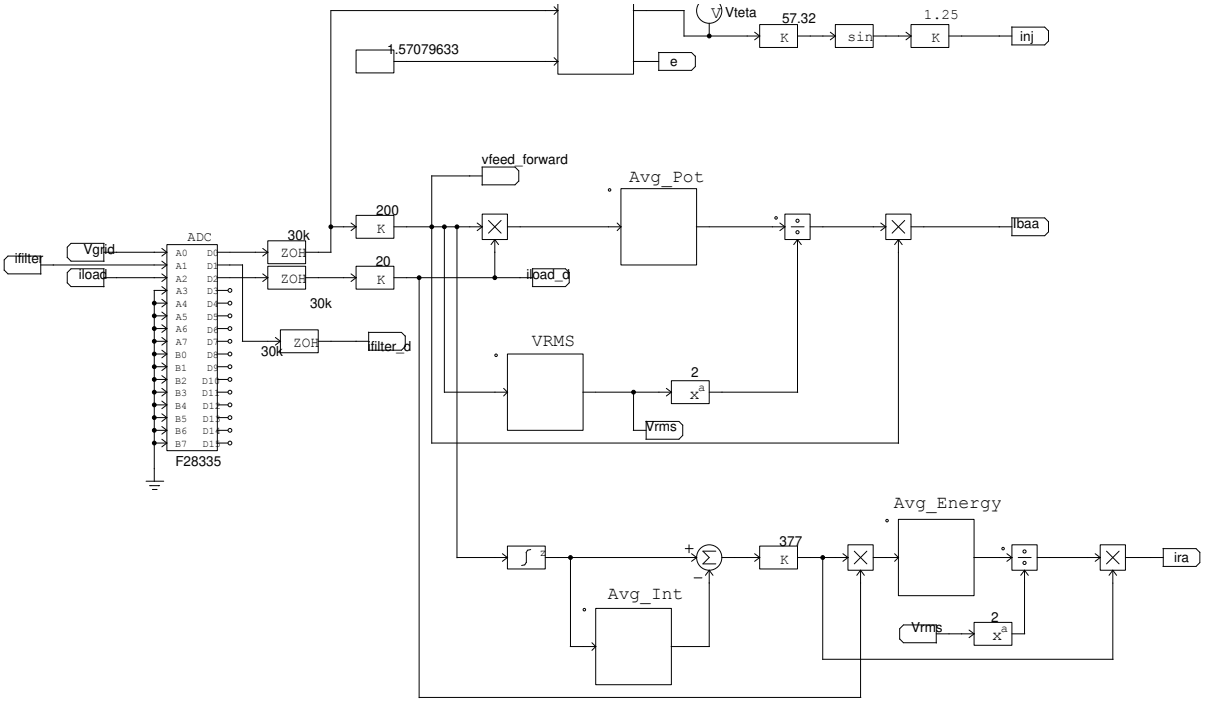

Figure E:3 - The circuits for ADC converter, the PLL and the CPT.

Figure E:4 presents the circuits for the current controller.

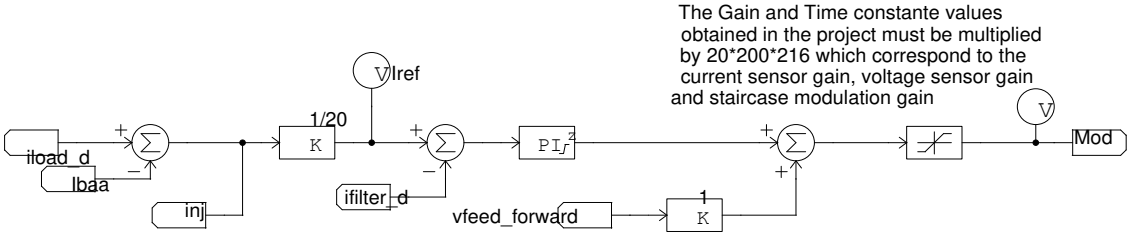

Figure E:4 – Circuits for the current controller.

Figure E:5 presents the circuits for the staircase modulation.

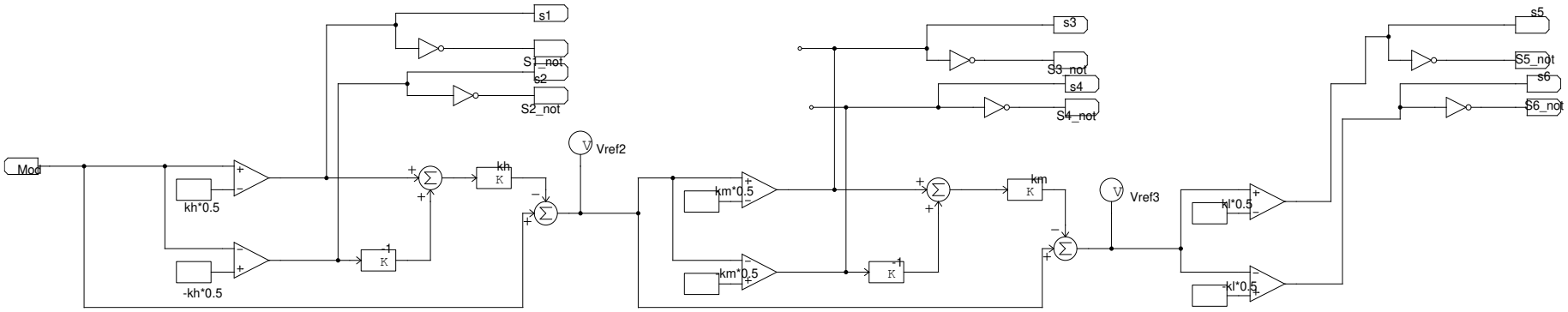
Mod
kh*0.5
-kh*0.5
kh
K
-1
K
s1
S1_not
s2
S2_not
Vref2
km*0.5
-km*0.5
km
K
-1
K
s3
S3_not
s4
S4_not
Vref3
kl*0.5
-kl*0.5
s5
S5_not
s6
S6_not

Figure E:5 – Circuits for the staircase modulation.

Figure E:6 presents the circuits for the digital outputs.

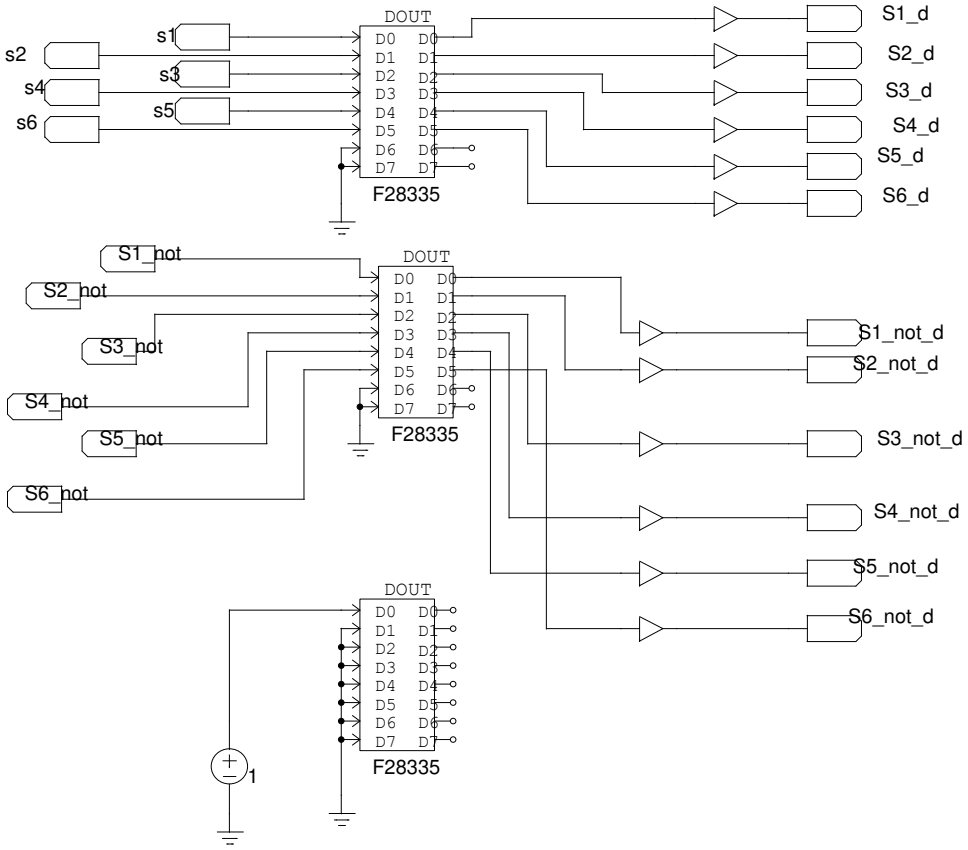

Figure E:6 – Circuits for the digital outputs.

APPENDIX F – DETAILS ABOUT THE SIMULATION OF THE SMART MICRO-GRID

This appendix presents details about the simulation of the micro smart grid simulation and prototype. The simulation file is freely available on https://sites.google.com/site/busarellosmartgrid/home.

Figure F:1 presents the circuits for the grid, the PCCs and the loads.

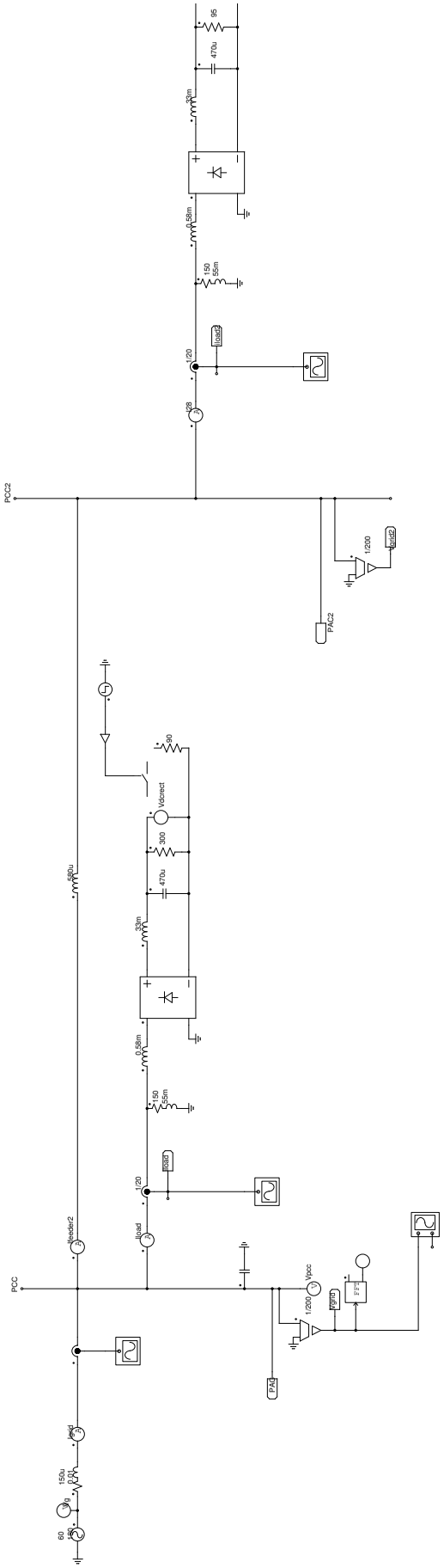

Figure G:1 - Circuits for the grid, the PCCs, the feeders and the loads.

APPENDIX G – DETAISL ABOUT THE MICRO SMART GRID PROTOTYPE

This appendix present details about the micro smart grid prototype. A complete schematic of the micro smart grid prototype is freely available on https://sites.google.com/site/busarellosmartgrid/home.

Figure G:1 presents the schematic for the central control. The schematic for each component is also available on the referred website.

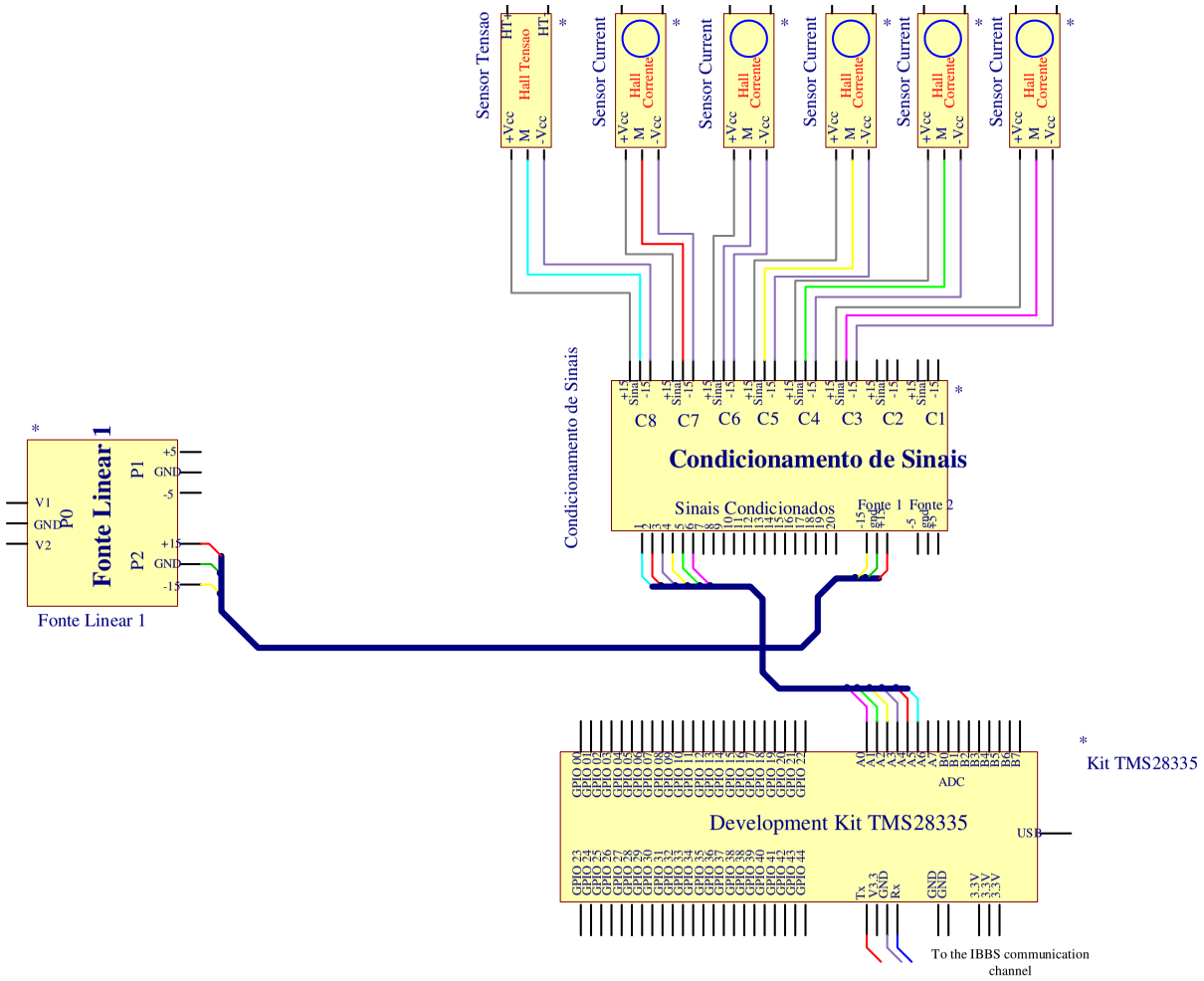

Figure G:1 - Schematic for the central control.

APPENDIX H – PUBLICATIONS

This appendix presents the publications along the doctorate course. The list shows the publications until the moment this of thesis was written.

H.1 Papers published in journals

CURI BUSARELLO, T.D;. ANTENOR POMILIO, J. “Bidirectional Multilevel Shunt Compensator with Simultaneous Functionalities based on the Conservative Power Theory” IET Journal of Generation, Transmission and Distribuiton, 2014, (A1).

MARCELO GODOY SIMÕES, TIAGO DAVI CURI BUSARELLO, ABDULLAH SAAD BUBSHAIT, FARNAZ HARICHI, JOSÉ ANTENOR POMILIO AND FREDE BLAABJERG; “Interactive Smart Battery Storage for PV and Wind Energy System Management Control Based on the Conservative Power Theory”. International Journal of Control, 2014 (A1).

H.2 Chapter in book

TIAGO DAVI CURI BUSARELLO AND MARCELO GODOY SIMÕES. “Distributed Generation and Microgrids” in Power Electronic Converters and Systems: Frontiers and Applications by Andrzej M. Trzynadlowski. IET. ISBN: 978-1-84919-826-4.

H.3 Papers published in conferences

CURI BUSARELLO, T.D.; ANTENOR POMILIO; “Synergistic operation of distributed compensators based on the conservative power theory”. Submitted on April 30th to the Power Electronics Brazilian Conference (COBEP).

Mortezaei, Ali; Simoes, M.Godoy; Busarello, Tiago Davi Curi, "A multi task microgrid inverter based instantaneous Power Theory in islanded and grid-connected modes," in Power & Energy Society General Meeting, 2015 IEEE , vol., no., pp.1-5, 26-30 July 2015.

Busarello, Tiago Davi Curi; Pomilio, Jose Antenor; Bubshait, Abdullah Saad; Simoes, Marcelo Godoy, "Staircase modulation based battery storage system with Asymmetric Cascaded H-Bridge Multivel Inverter," in Power & Energy Society General Meeting, 2015 IEEE , vol., no., pp.1-5, 26-30 July 2015.

BUSARELLO, TIAGO. D. C, ABDULLAH SAAD BUBSHAIT, MARCELO GODOY SIMÕES, JOSÉ ANTENOR POMILIO. “Staircase Modulation Based Battery Storage System with Asymmetric Cascaded H-Bridge Multivel Inverter”. 2015 IEEE PES General Meeting.

ALI MORTEZAEI, M. GODOY SIMÕES, BUSARELLO, TIAGO. D.. “A Multi Task Microgrid Inverter Based Instantaneous Power Theory in Islanded and Grid-Connected Modes” 2015 IEEE PES General Meeting.

BUSARELLO, TIAGO. D. C. ; SIMÕES, M .G. ; “Power Quality Enhancement by means of Shunt Compensators based on the Conservative Power Theory”. 2015 Clemson University Power Systems Conference (PSC).

CURI BUSARELLO, T.D.; ANTENOR POMILIO, J. Bidirectional Multilevel Shunt Compensator with Simultaneous Functionalities Based on the Conservative Power Theory. In: 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014), 2014, Manchester. 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014). p. 1.11.04.

BUSARELLO, TIAGO. D. C. ; MORALES, H. ; POMILIO, J. A. . An Intelligent Battery-based Energy Storage System Based on Multilevel Inverter and the Conservative Power Theory. In: PCIM South America 2014 - International Conference and Exhibition for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2014, São Paulo. Proc. of PCIM South America 2014. Frankfurt:: Mesago PCIM GmbH, 2014. p. 174-181.

MOREIRA, A. C. ; BRANDAO, D. I. ; BUSARELLO, TIAGO DAVI CURI ; POMILIO, J. A. ; SILVA, L. C. P. ; PAREDES, H. K. M. . Impactos técnicos decorrentes da conexão de geradores fotovoltaicos com injeção de reativos em redes residenciais. In: Simpósio Brasileiro de Sistemas Elétricos, 2014, Foz do Iguaçú. Anais do V SBSE 2014, 2014.

H.4 Papers submitted to periodicals

CURI BUSARELLO, T.D.; ANTENOR POMILIO; SIMÕES, M .G. “Passive Filter Aided by Shunt Compensators based on the Conservative Power Theory”. Submitted on July 21st to the IEEE IAS Transaction on Renewable and Sustainable Energy Conversion Systems (RES) Committee.