UNIVERSIDADE ESTADUAL DE CAMPINAS
Faculdade de Engenharia Elétrica e de Computação

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FinFET Prototype Fabrication Using Alternative Methods

Fabricação de Protótipos de FinFETs Usando Métodos Alternativos

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Dissertação apresentada à Faculdade de Engenharia Elétrica e de Computação da Universidade Estadual de Campinas como parte dos requisitos exigidos para a obtenção do título de Mestra em Engenharia Elétrica, na área de Eletrônica, Microelectrônica e Optoeletrônica.

Supervisor: Prof. Dr. Leandro Tiago Manera

Co-supervisor: Prof. Dr. José Alexandre Diniz

Este exemplar corresponde à versão final da tese defendida pela aluna Alessandra Leonhardt, e orientada pelo Prof. Dr. Leandro Tiago Manera

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Campinas

2016

Agência(s) de fomento e nº(s) de processo(s): CNPq, 161893/2015-5

Ficha catalográfica
Universidade Estadual de Campinas
Biblioteca da Área de Engenharia e Arquitetura
Elizangela Aparecida dos Santos Souza - CRB 8/8098

L553f

Leonhardt, Alessandra, 1990-
FinFET prototype fabrication using alternative methods / Alessandra Leonhardt. – Campinas, SP : [s.n.], 2016.

Orientador: Leandro Tiago Manera.
Coorientador: José Alexandre Diniz.
Dissertação (mestrado) – Universidade Estadual de Campinas, Faculdade de Engenharia Elétrica e de Computação.

1. Transistores de efeito de campo. 2. Feixes de íons focalizados. 3. Microeletrônica. I. Manera, Leandro Tiago,1977-. II. Diniz, José Alexandre,1964-. III. Universidade Estadual de Campinas. Faculdade de Engenharia Elétrica e de Computação. IV. Título.

Informações para Biblioteca Digital

Título em outro idioma: Fabricação de protótipos de FinFETs usando métodos alternativos
Palavras-chave em inglês:
Field effect transistors
Focused ion beam
Microelectronics
Área de concentração: Eletrônica, Microeletrônica e Optoeletrônica
Titulação: Mestra em Engenharia Elétrica
Banca examinadora:
Leandro Tiago Manera [Orientador]
Stefan Jozef Emma Alfons De Gendt
Jacobus Willibrordus Swart
Data de defesa: 12-07-2016
Programa de Pós-Graduação: Engenharia Elétrica

COMISSÃO JULGADORA - DISSERTAÇÃO DE MESTRADO

Candidata: Alessandra Leonhardt RA: 162634

Data da Defesa: 12 de Julho de 2016

Título da Tese: FinFET Prototype Fabrication Using Alternative Methods (Fabricação de Protótipos de FinFETs Usando Métodos Alternativos)

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A ata de defesa, com as respectivas assinaturas dos membros da Comissão Julgadora, encontra-se no processo de vida acadêmica do aluno.

We choose to go to the moon. We choose to go to the moon in this decade and do the other things, not because they are easy, but because they are hard, because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone, and one which we intend to win.

[Address at Rice University, September 12 1962]
John F. Kennedy

Study hard what interests you the most in the most undisciplined, irreverent and original manner possible.

[Letter to J. M. Szabados, November 30, 1965]
Richard Feynman

Agradecimentos

Em primeiro lugar, gostaria de agradecer ao meu orientador, Leandro Tiago Manera, pelo apoio e confiança. Cuja motivação e entusiasmo foram essenciais no curso da pesquisa. Agradeço ao meu co-orientador, José Alexandre Diniz, pelas discussões muito prolíficas que ajudaram a dar forma a esse trabalho.

Agradeço ao CNPq pelo apoio financeiro e pelas políticas de incentivo à pesquisa, ao desenvolvimento e à inovação do governo brasileiro, que ainda não sendo ideais, já nos permitem mais do que haveria, se fosse de outra forma.

Aos grandes amigos e excelentes pesquisadores Lucas Petersen Barbosa Lima e Marcos Puyidinger dos Santos, que me ensinaram boa parte do que sei hoje e que me apoiaram sempre, e que acima de tudo me cobram sempre um trabalho sério. Que me ajudaram a sonhar mais alto e a buscar mais longe.

Agradeço aos meus amigos Jeckson Souza, Arthur Rauter, Gennaro Rodrigues, Luis Henrique Reinicke e Marcelo Brandalero, que tinham sempre uma piada guardada para os dias escuros e cuja amizade é muito valiosa.

Aos funcionários e colegas do CCSNano e do LPD/IFGW que me ajudaram em muitos momentos e me desafiaram a ser uma pessoa melhor em outros.

À minha esposa, Flávia Filippin, que foi sempre o mais importante suporte e incentivo em todos os momentos. Que é a motivação de todo o trabalho, de todo o esforço e empenho, e a razão de buscar ser sempre melhor do que se é.

Agradeço aos meus pais e irmãs, que possibilitaram minha caminhada, que torceram a cada conquista e que estenderam a mão a cada tropeço.

Abstract

This work explores alternative methods for FinFET prototype fabrication. Different fin definition methods (Al hard mask FIB milling and Ga^+ FIB lithography) are explored, aiming for flexibility in defining the number of fins, as well as fin height. Alternative gate stacks are applied in the fabricated FinFETs, with two different dielectric materials (SiON and TiAlON) and two different methods for TiN gate electrode formation. The detailed fabrication process is provided and discussed, with special attention to difficulties and challenges faced. Fabrication steps are carefully evaluated, presenting details and parameters such as that the process could be replicated. Morphological and electrical characterizations are performed on the fabricated FinFETs. With the Ga^+ FIB lithography method, working FinFETs with nine parallel fins are fabricated, with fin width down to 87nm. Electrical parameters are extracted, such as V_{TH}, subthreshold slope, leakage current, low field mobility, R_{SD}, gate electrode work function, EOT, and others. Working FinFETs with sub-100nm fin width are presented, with subthreshold slope of 120mV/dec and low field mobility of $372cm^2/v.s$, results that show an improvement on previous works, but still leave room for optimizations. Discussions are performed, explaining the meaning of the extracted parameters, and ways to improve the results. The different gate stacks are evaluated regarding their parameter stability and leakage current density. An EOT of 3.6nm is achieved for the SiON dielectric, with leakage current density between $177\mu A/cm^2$ and $0.61mA/cm^2$. Important developments have been made towards process integration and novel prototype fabrication methods. Future works include silicon-dielectric interface improvements and a self aligned process to achieve increased transconductance and gate-to-channel coupling, and reduce the series resistance.

Keywords: FinFET; MOSFET; Nanotechnology; Prototype Fabrication; Focused Ion Beam; Metal Gate.

Resumo

Este trabalho explora métodos alternativos para fabricação de protótipos de FinFETs. Diferentes métodos de definição de *fin* (fresagem de máscara de Al por feixe de íon focalizado e litografia por feixe focalizado de íons de gálio) são explorados, buscando flexibilidade na definição do número de *fins*, bem como a altura dos *fins*. Diferentes estruturas de porta são aplicados nos FinFETs fabricados, com dois materiais dielétricos diferentes (SiON e TiAlON) e dois métodos diferentes para a formação de TiN como eletrodo de porta. O processo de fabricação detalhado é fornecida e discutido, com especial atenção às dificuldades e desafios enfrentados. Etapas de fabricação são cuidadosamente avaliadas, apresentando detalhes e parâmetros de forma que o processo possa ser replicado. Caracterizações morfológicas e elétricas são realizadas nos FinFETs fabricadas. Com a litografia por feixe focalizado de íons de gálio, FinFETs com nove *fins* em paralelo são fabricados, com largura de *fin* até 87nm e comportamento elétrico de transistor. Parâmetros elétricos são extraídos, tais como V_{TH}, inclinação de sublimiar, corrente de fuga, mobilidade de portadores, R_{SD}, função trabalho do eletrodo de porta, EOT, e outros. FinFETs com largura fin abaixo de 100nm são apresentados, com inclinação de sublimiar de 120 mV/dec e moblidade de portadores de 372 cm^2/V.s, resultados que mostram uma melhoria em relação a trabalhos anteriores, mas ainda deixam espaço para otimizações. Discussões são realizadas, explicando o significado dos parâmetros extraídos, e formas de melhorar os resultados. As diferentes estruturas de porta são avaliados quanto à estabilidade dos parâmetros e densidade de corrente de fuga. Um EOT de 3.6nm é alcançado para o dieléctrico SiON, com densidade de corrente de fuga entre 177µA/cm^2 e 0.61mA/cm^2. Desenvolvimentos importantes são feitos no sentido da integração de processos e inovaçoes em termos de métodos de fabricação de protótipos. Trabalhos futuros incluem melhorias na interface de silício-dielétrico e um processo de fabricação auto alinhado para alcançar uma maior transcondutância e acoplamento entre porta e canal, e reduzir a resistência série.

Palavras-chaves:FinFET; MOSFET; Nanotecnologia; Fabricação de Protótipos; Feixe de Íons Focalizado; Eletrodo Metálico de Porta.

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μ_0 low field mobility.

ALD atomic layer deposition.

CMOS complementary metal oxide semiconductor.

CMP chemical mechanical polishing.

CVD chemical vapour deposition.

DI deionized.

DIBL drain induced barrier lowering.

e-beam electron beam.

EBL electron beam lithography.

ECR electron cyclotron resonance.

EDS energy dispersive X-ray spectroscopy.

EOT equivalent oxide thickness.

EUVL extreme ultraviolet lithography.

FIB focused ion beam.

FinFET fin field effect transistor.

HF hydrofluoric acid.

IC integrated circuit.

ICP inductively coupled plasma.

L_{met} metallurgical channel length.

LDD lightly doped drain/source.

MEMS micro electro-mechanical systems.

MIF metal ion free.

MOSFET metal oxide semiconductor field effect transistor.

R_{OUT} output resistance.

R_{SD} source and drain series resistance.

RIE reactive ion etch.

RTA rapid thermal annealing.

SEM scanning electron microscope.

SIMS secondary ion mass spectrometry.

SiON silicon oxynitride.

SOI silicon-on-insulator.

STI shallow trench isolation.

TEM transmission electron microscope.

TiAlON titanium-aluminium oxynitride.

V_{FB} flat band voltage.

V_{th} threshold voltage.

VLSI very large system integration.

W_{fin} fin width.

WF work function.

Contents

1 Introduction

1.1 Planar and 3D MOSFETs

The metal oxide semiconductor field effect transistor (MOSFET) can be considered one of the greatest inventions of the 20th century and has revolutionized the field of electronic devices and systems. For the last five decades the transistor has become steadily smaller, following the observation made by Gordon Moore (MOORE, 1965; GARGINI, 2015). However, it is a constant challenge for process engineers to reduce its dimensions, which ranges from incremental improvements and slight tricks to whole new materials and novel processes. Figure 1 presents the evolution of Intel technology from the 0.5µm technology node to the 14nm node, in regards to the several aspects that comprise the complete integrated circuit (IC) fabrication. It can be seen that to achieve modern transistors with gate lengths of few nanometres, steady efforts in all aspects had to be made. The transistor architecture change towards Tri-Gate, also known as fin field effect transistor (FinFET), has been commercially introduced in 2011, and current research is focused on further improvements still – such as replacing the silicon channel for a material with higher carrier mobility. It is important to note that although some developments are ground-breaking – such as the introduction of high-κ dielectric and metal gate – they are not final. For the scaling to continue, new developments have to be introduced every node and new paradigms are researched, which could solve one problem or another (COLLAERT et al., 2015).

The main focus of this Master thesis are the transistor architecture, gate oxide and gate electrode aspects. Beyond 32nm, short channel effects degrade the electrical behaviour of planar MOSFETs, and a 3D channel becomes essential. It provides superior gate-to-channel coupling, lessening effects such as drain induced barrier lowering (DIBL) and enabling excellent device subthreshold characteristics (SUBRAMANIAN et al., 2006; COLINGE et al., 2008). The adopted solution was the FinFET (HUANG et al., 1999; HISAMOTO et al., 2000), a tri- or double-gate semiconductor device with self-aligned source and drain regions and gates aligned to each other, and planar complementary metal oxide semiconductor (CMOS)-compatible process flow. A schematic of a planar MOSFET, fabricated in bulk silicon, and of a 3D FinFET, fabricated on silicon-on-insulator (SOI) substrate, is presented in Figure 2[1]. One can see that a completely new direction related to transistor fabrication was taken when the 3D FinFET was first introduced. What was a mostly planar process – in the front end of the line, at least – now becomes three-dimensional, and has to solve issues related to this device three dimensionality – step

[1] All figures whose source has not been mentioned are of own elaboration.

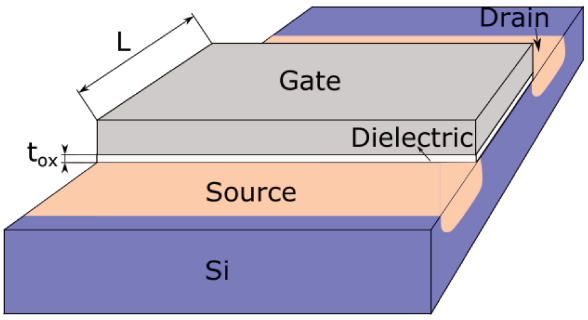
Evolution of Intel Technology

Process	P852	P854	P856	P858	PX60	P1262	P1264	P1266	P1268	P1270	P1272
Year	1993	1995	1997	1999	2001	2003	2005	2007	2009	2011	2014
Node	0.5µ	0.35µ	0.25µ	0.18µ	0.13µ	90nm	65nm	45nm	32nm	22nm	14nm
Metal	Al	→	→	→	Cu	→	→	→	→	→	→
Interlevel Dielectric	SiO2	→	→	SiOF	→	CDO	→	→	→	→	Air Gap
Transistor Architecture	Planar	→	→	→	→	→	→	→	→	Tri-Gate	→
Gate Oxide	SiO2	→	→	→	→	→	SiON	High-K	→	→	→
Gate Electrode	Poly	→	→	→	→	→	→	Metal	→	→	→
Channel	Si	→	→	→	→	Strained Si	→	→	→	→	→
Lithography	365nm	248nm	→	→	→	193nm	→	Double Pattern	i193nm	→	→
Wafer Size	200mm	→	→	→	200mm/ 300mm	300mm	→	→	→	→	→

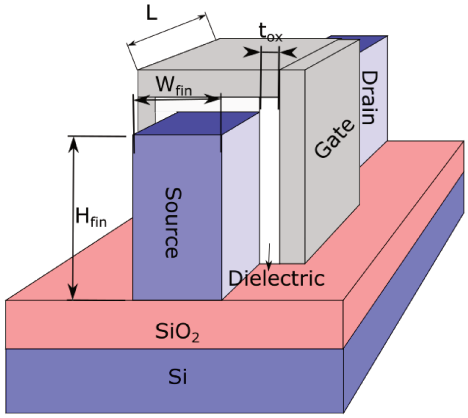
Source: Intel, IC Insights

Figure 1 – Evolution of different aspects of Intel integrated circuit fabrication. From (IC INSIGHTS, 2015).

coverage during material deposition and careful sidewall etching, to name a couple.



(a) Planar Bulk MOSFET



(b) 3D SOI FinFET

Figure 2 – Three dimensional schematic of a planar bulk MOSFET and a SOI FinFET.

1.2 Transistor Operation

The main principle of MOSFET operation is to apply a bias on the gate electrode that creates an inversion layer on the semiconductor substrate, where a source to drain current flows. In this section the transistor physical and electrical operation will be briefly explained in the context of the works presented in Grove (1967), Tsividis (2003) and Sze and Ng (2006).

When varying the gate bias, two regions are clearly discernible: the subthreshold region (Figure 3a), where the channel is still beginning to form, and the inversion region (Figure 3b), where the channel is fully formed and the transistor is conducting.

If the gate bias is set to a value above the threshold voltage, varying the drain voltage takes the transistor from the linear region (Figure 3b), where an increase in V_{DS} results in a linear increase in I_{DS}, to the saturation region (Figure 3c), where the channel is pinched off and the current is constant for further increases in V_{DS}.

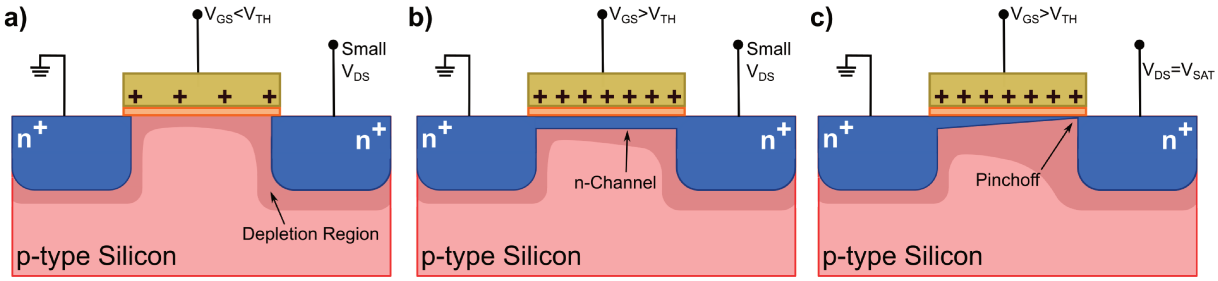


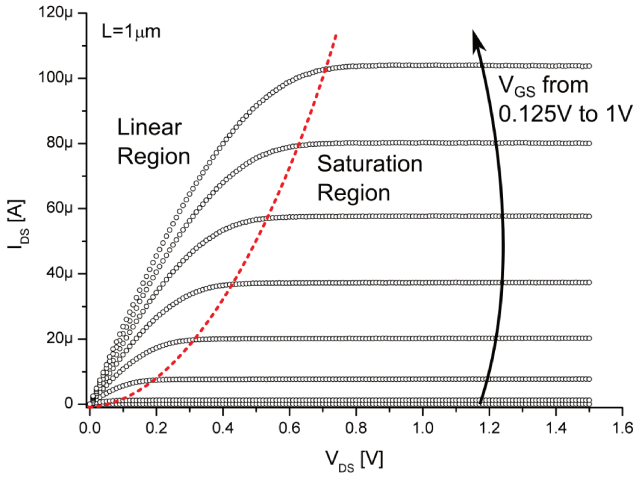
Figure 3 – Illustration of the operation of the MOS transistor in the subthreshold region (a), linear region (b) and saturation region (c).

The physical operation translates in current response for a given condition of source, drain and gate bias. In Figure 4 the typical transistor behaviour is presented through the characteristic I_{DS} measurements of FinFET fabricated at IMEC with gate length of 1µm and 10nm fin width (FERREIRA, 2012; LEONHARDT, 2014). Throughout this work similar curves – for the FinFETs fabricated and measured in this thesis – will be presented and analysed.

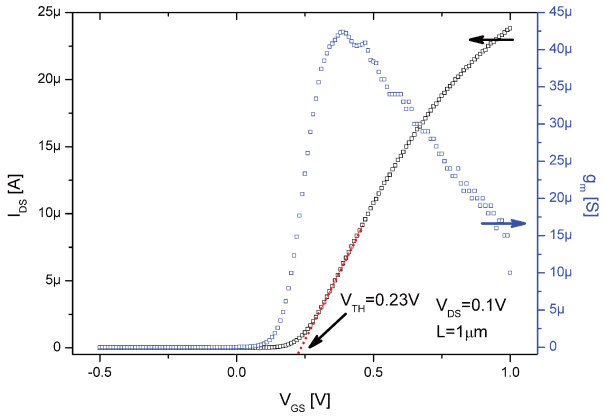
Figure 4a shows the I_{DS}xV_{DS} curve of the MOS transistor. For a given V_{GS}, increasing V_{DS} takes the transistor from the linear region, where the drain current increases linearly with V_{DS}, to the saturation region, where I_{DS} is ideally constant. On the onset of saturation, V_{DS} is equal to V_{GS} minus V_{TH}. Increasing the gate bias value takes the transistor back to the linear region, what gives rise to the quadratic curve that divides the linear and saturation regions.

The current response with the variation of V_{GS} is analysed in Figure 4b and Figure 4c, for a small V_{DS}, showing the above threshold and subthreshold characteristics, respectively. When increasing V_{GS}, the transistor passes from an off state, with small current, to an on state, where I_{DS} increases almost linearly with every increase in V_{GS}, as shown in Figure 4b. The voltage where the transistor start conducting, roughly (SUN et al., 1986; TAUR, 2000; SCHRODER, 2006), is called the threshold voltage (V_{th}). The transconductance, presented in the right hand axis, is defined as $\frac{dI_{DS}}{dV_{GS}}$, and represents how much current the transistor delivers for an increase in V_{GS}.

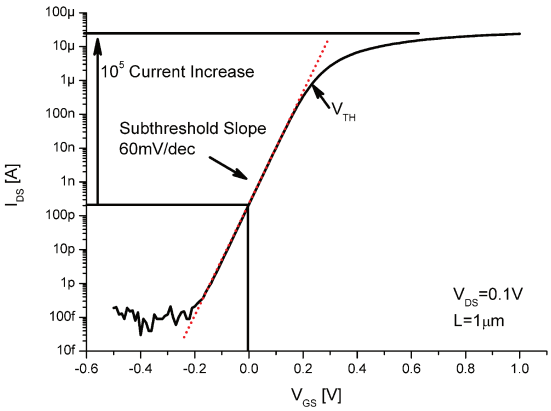
Below V_{th} the current is not zero, however. Figure 4c presents the same I_{DS}xV_{GS} discussed previously, but in logarithmic scale, such as to better evaluate the exponential



(a) Drain current response when increasing the drain bias, for different values of gate bias.



(b) Drain current response and device transconductance when increasing the gate bias, for a small drain voltage.



(c) Drain current response in the subthreshold region, showing the exponential current increase.

Figure 4 – MOSFET typical electrical response presented using FinFETs with 1µm gate length and 10nm fin width.

current increase in the subthreshold region. An increase in V_{GS} from negative values to the threshold voltage induces a sharp increase in I_{DS}, dominated by the diffusion current. Two important transistor figures of merit can be extracted from this graph, the subthreshold slope and the I_{ON}/I_{OFF} ratio. The first indicates how much V_{GS} needs to increase to induce a tenfold increase in I_{DS}, and is defined as

$$S \simeq \frac{kT}{q} ln\left(10\frac{C_{ox}+C_D+C_{it}}{C_{ox}}\right) \tag{1.1}$$

where C_D is the depletion capacitance, C_{it} the interface trap capacitance and C_{ox} the gate oxide capacitance. The minimal theoretical limit is 59.6 mV/decade at T=300K, where $S = \frac{kT}{q} ln(10)$, where the capacitance terms C_{it} and C_D approach zero (SZE; NG, 2006). The I_{ON}/I_{OFF} ratio indicates how much the drain current increases from the transistor off

state at zero gate bias to the on state at high V_{GS}. In the transistor presented in Figure 4c, the subthreshold slope is 60mV/dec, what is called ideal, and the I_{ON}/I_{OFF} ratio is 10^5, the current increases five orders of magnitude from the off state to the on state.

1.3 FinFET Fabrication Overview and Related Challenges

FinFET fabrication flow on SOI substrates can be divided in four simplified steps: fin patterning, gate stack formation, source and drain implant, and contacts and interconnect deposition, presented schematically in Figure 5.

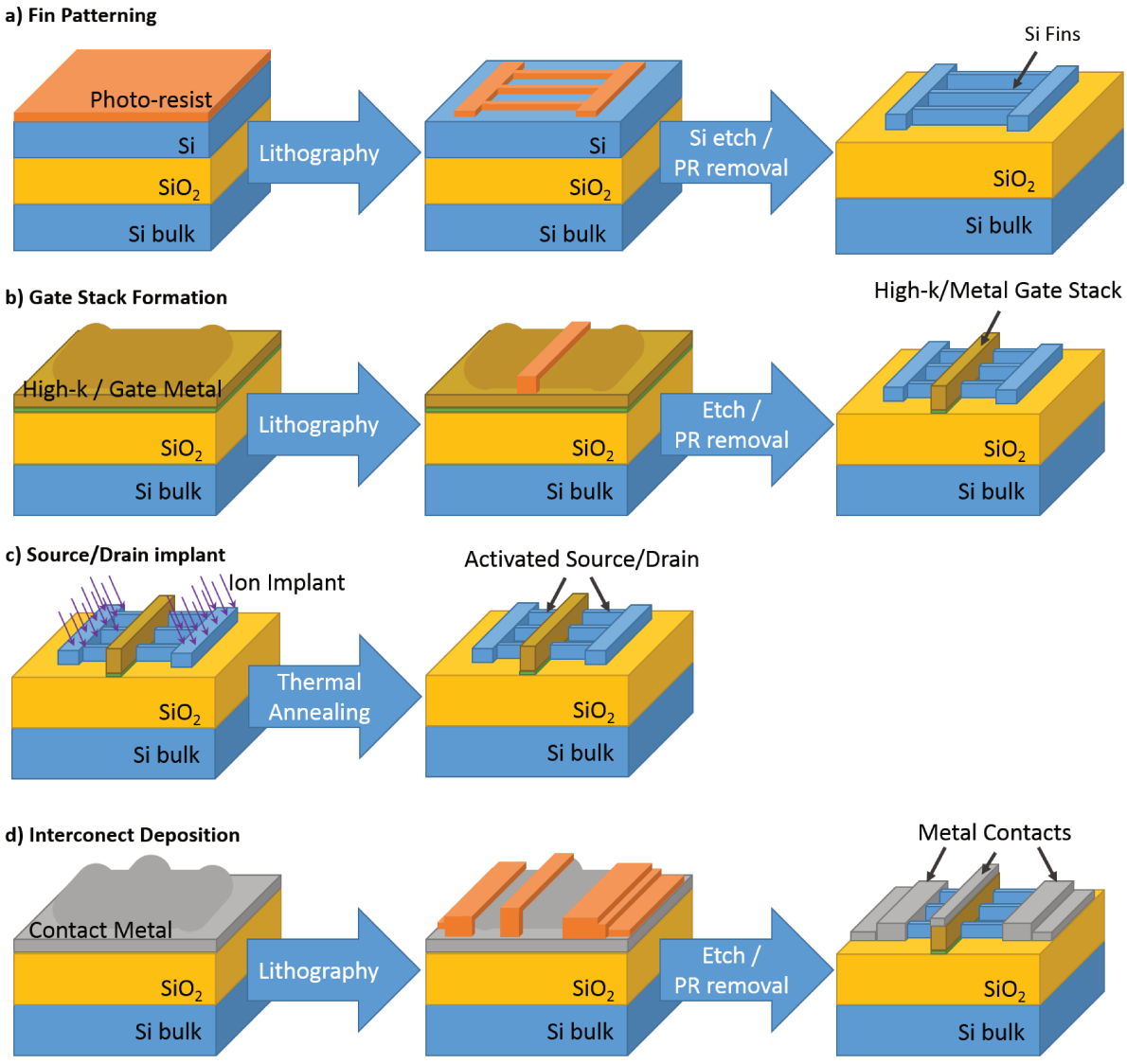


Figure 5 – Simplified schematic of the FinFET fabrication flow, presenting the fin patterning (a), gate stack formation (b), source and drain implant (c) and interconnect deposition (d)

Fin patterning (Figure 5a) consist in the definition of the active area, the fins and source/drain pads, using a lithographic method that achieves small enough dimensions.

The silicon layer is then etched and the photo-resist or other masking material is removed, leaving the silicon fins exposed for the next step. Gate stack formation (Figure 5b) can be achieved by high-κ dielectric deposition, followed by gate metal deposition, which is then lithographically defined and etched. Again, the lithographic method used, along with the etching techniques, has to be able to produce gate lengths of sub-50nm or less. Source and drain implantation (Figure 5c), along with thermal annealing, creates the source and drain junctions, by incorporation and activation of impurity atoms in the silicon lattice. The final gate stack, with the correct materials, can be formed either before – known as gate first scheme – of after – gate last scheme – source and drain implantations, according to process design decisions (FRANK, 2011; VELOSO et al., 2011). Contact and interconnect deposition (Figure 5d) is usually the last step of device fabrication, where the contact metal is deposited, patterned and etched. Contact deposition allows the device to be accessed to be tested or connected to other devices, creating a circuit.

The presented fabrication steps are obviously simplified, since modern CMOS fabrication involves additional steps such as gate sidewall spacer formation, silicides, complex gate stacks, engineered junction profiles and others (CHAU et al., 2007; HARELAND et al., 2013). Also, FinFETs fabricated on bulk silicon substrates require further additional steps, such as ion implants to avoid junction punchthrough and creation of shallow trench isolation (STI) (LINDERT; CEA, 2006).

Although FinFETs present simplified fabrication steps, compared to other multiple gate transistor designs –such as planar and vertical double-gate transistors (NOWAK et al., 2004)–, several challenges arise from the channel three dimensionality. The challenges are mainly related to sidewall smoothness after etching, ion implantation and uniform fin doping, conformal metal gate deposition and layout usage (KAWASAKI et al., 2009).

One of the most important structural parameter in a FinFET device – which is not present in planar MOSFETs – is the fin width (W_{fin}). A very thin fin is desired, to ensure volume inversion, improve the electrical response and reduce short channel effects (DAL et al., 2007). Volume inversion is when the current flows in the center of the fins, not on the surface, reducing the mobility scattering effects and resulting in enhanced transistor performance, as first suggested by Balestra et al. (1987). It is only achieved, however, in fins thinner than 10nm (COLINGE et al., 2008), which imposes serious fabrication challenges not only to achieve this dimension, but to ensure uniformity and low roughness. Besides thin fins, multiple fin FinFET are also desired. Multiple fins improve FinFET electrical characteristics, for two important reasons: first, it provides better layout usage, and a wider channel for the same device, increasing the transistor drive current; second, it averages the fin characteristics, reducing random morphological variations that may compromise single fin transistors (SHANG et al., 2006). The fin definition is thus the first FinFET fabrication challenge, and special attention is required on the sidewall roughness,

which increases mobility scattering and degrades the device performance (CHOI et al., 2002a). Another issue is to guarantee that the metal gate fully envelops the fin, with proper step coverage and uniform thickness (JURCZAK et al., 2009).

Regarding fin doping, two main issues can be discussed: channel doping and source and drain doping. While planar MOSFETs require complex doping profiles to succesfully suppress short channel effects, the supperior gate-to-channel coupling provided by FinFET devices allows the reduction of the channel doping (KING, 2005). An undoped channel provides higher carrier field effect mobility, increasing the transistor drive current. Random discrete doping variability is also significantly suppressed, when reducing the channel doping (WANG et al., 2011). For FinFETs with undoped channel, the threshold voltage (V_{th}) is controlled mainly by the gate electrode work function. Work function variations become thus the main source of V_{th} variations between transistors in a circuit (MATSUKAWA et al., 2009).

The challenge of FinFET source and drain doping is related to uniformity and silicon amorphisation. An uniform doping of FinFET source and drain is more difficult to obtain due to fin shadowing, where one fin acts as a mask for the ion implant of the other (KAWASAKI et al., 2008). Also, the very thin silicon layer is prone to complete fin amorphisation during source and drain ion implant, which leads to problematic recrystallization during high temperature anneal. Boundary defects and possibly polycrystalline fins can result from complete amorphisation, contributing to increase the source and drain series resistance (R_{SD}) (DUFFY et al., 2007; COLLAERT et al., 2008). One way of preventing full amorphisation is to perform epitaxial regrowth of the thin fins – thus increasing the size of the silicon layer – before source and drain ion implantation, which also reduces significantly the source and drain series resistance (R_{SD}) (BASKER et al., 2010).

1.4 Objectives and Motivation

MOSFET prototype fabrication is an important part of the development cycle of new technologies and a basis for important discoveries in materials and devices. Transistor prototypes are mainly used to evaluate new materials and fabrication alternatives that can be integrated in the main process flow if successful. New materials or deposition methods for a given material should be assessed both regarding their morphological and electrical parameters. Due to its constraints on step coverage, sidewall roughness and work function stability, FinFET devices present themselves as excellent mediums for electrical characterisation of novel gate stack materials, for example. The fin has to be completely covered by both the dielectric and gate electrode, or else the device will not function properly. As such, the deposition method has to guarantee conformality, which can be assessed electrically using FinFET prototypes. Furthermore, a dielectric film which induces

a high density of charged interface states degrades the transistor carrier mobility and the subthreshold slope, parameters extracted from the electrical measurements. In summary, the evaluation of a given material or deposition method, in semiconductor research, has to go beyond morphological assessments, and as the industry has moved towards 3D devices, so are research labs required to.

This work is an effort to bring FinFET prototypes as a feasible testing tool for future developments in the Center for Semiconductor Components and Nanotechnologies (CCS Nano). When performing experimental research, one faces several challenges and drawbacks. This work is focused at critically analysing the issues and identifying their sources, in order to solve some and propose improvements and useful advice for future works related to prototype fabrication. Special attention is given to in depth evaluation of the results, both structural – such as cross sections with magnification close to the scanning electron microscope (SEM) resolution limit – and electrical – with careful parameter extraction and result discussion.

To fabricate the FinFET prototypes, results from other works, both from CCS Nano and elsewhere, have been put together, investigated and optimized to a certain degree. An effort towards process integration has been made, since the best results should be applied to new studies in order to achieve progress. Nonetheless, part of this work consists of new developments and new methods, since past solutions were not able to solve the issues raised in this research.

Prototype fabrication and transistor scaling depends on a full toolbox of methods, materials and equipments that are continually evolving, as was seen in Figure 1. With this thesis one more technique is expected to be added to the FinFET prototyping toolbox: the multiple fin definition using Ga^+ focused ion beam (FIB) lithography. This technique allows fast device prototyping using the focused ion beam (FIB), when compared to the most common technique of substrate milling using the same equipment. The flexibility regarding number of fins and fin width provided by Ga^+ FIB lithography is valuable for prototype fabrication, since it allows FinFETs with different fin characteristics to be fabricated side by side. In addition, transistor scaling is full of examples of techniques and tricks that were used for reasons beyond their original purpose. Spacer technology is an interesting case, first used in the gate sidewalls, allowing the fabrication of high performance lightly doped drain/source (LDD) MOSFETs (TSANG et al., 1982), was later used for sub-20nm line patterning and fin definition (DEGROOTE et al., 2007; XU et al., 2013), then called self-aligned double-patterning or spacer lithography. Likewise, techniques designed for FinFET prototyping could potentially be used for vertically integrated nanowire FETs or other applications even.

1.5 Thesis Structure

The schematic structure of the thesis is presented on Figure 6. The first block indicates the introduction, where the motivations, and basic knowledge of transistor operation and FinFET fabrication is presented. The work then follows to the specific fabrication steps, with in depth details on fin definition and gate stack formation alternatives.

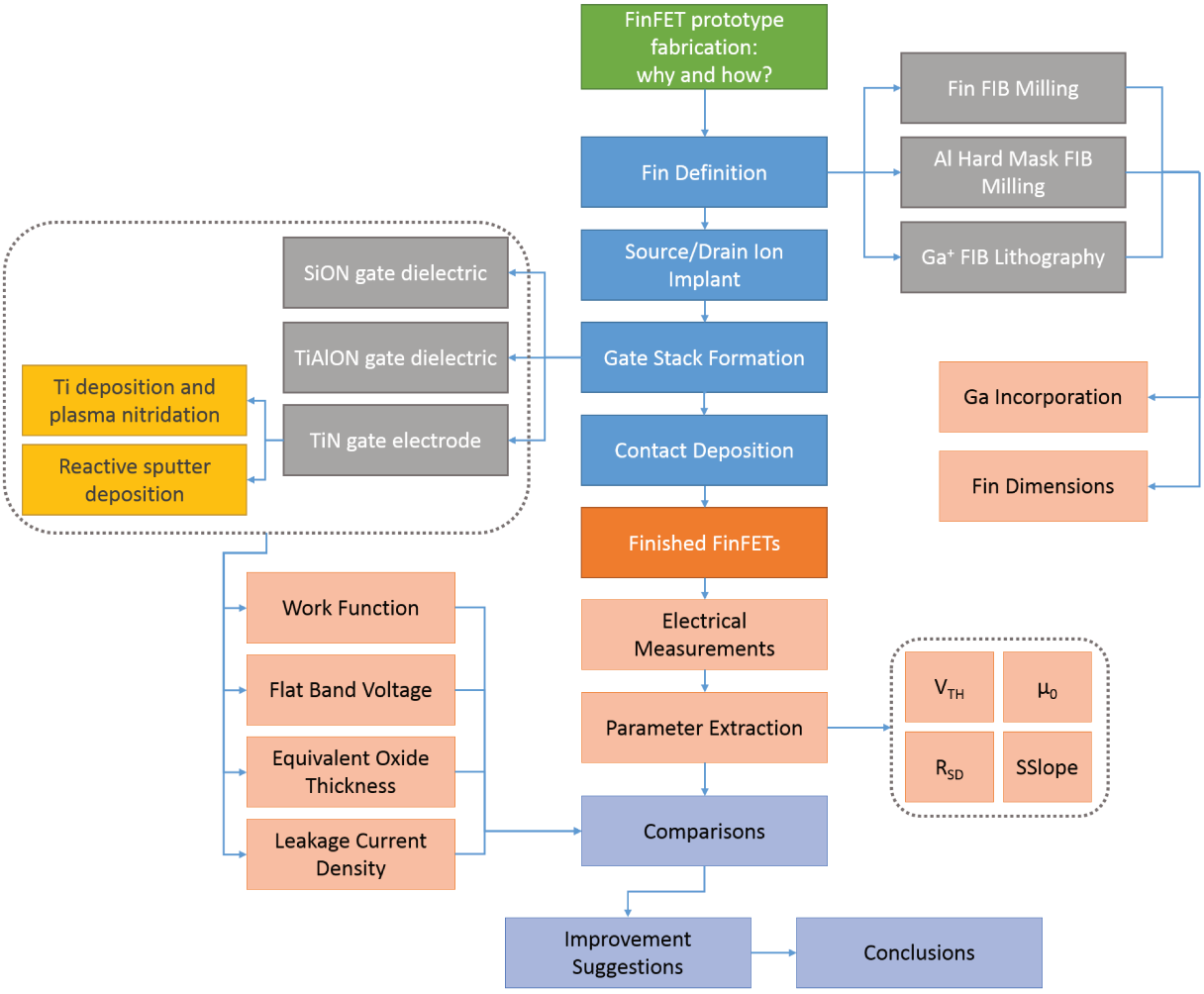


Figure 6 – Schematic organization of the work and how this thesis will present it.

In this work three fin definition methods are studied: Fin FIB Milling, Al hard mask FIB milling and Ga^+ FIB lithography, with special attention to the latter two. Those methods are described in Section 2.1, along with other lithographic alternatives for FinFET fin definition. In the experimental procedure their parameters and initial results are presented. The fin definition methods are evaluated regarding the process induced gallium incorporation and obtained fin dimensions, in Chapter 4, in the morphological characterisations.

Different FinFET gate stack alternatives are also explored, including two dielectrics – SiON and TiAlON – and two different methods for TiN formation – e-beam titanium deposition followed by plasma surface treatment, and reactive sputter deposi-

tion. These materials and methods are discussed in the context of analogous results and applications, and gate stack alternatives used in modern CMOS by either the industry or other research institutes. The experimental formation of the different gate stacks in the fabricated FinFET prototypes and control capacitors is presented in Chapter 3, and the extracted parameters, results and comparisons are discussed in Section 4.2.

Following the FinFET fabrication, presented in the experimental procedure in Chapter 3, a complete device is obtained. Electrical characterisations is then performed and discussed along with its extracted parameters, such as R_{SD}, V_{th} and mobility, for example. The discussions and comparisons are tied with gate stack comparisons and lead to the conclusions. Improvement suggestions are made, based on the extracted parameters, electrical characterisations and evaluations of problems during prototype fabrication. It is not expected that this thesis solves all issues related to process integration and prototype fabrication, but that it provides useful advice for future improved devices. The final conclusions are thus drawn based on the fabrication experience and results achieved.

2 FinFET Fabrication Processes

Several fabrication steps are necessary for modern IC fabrication. In this section some of these fabrication steps will be covered, focusing on the key process for FinFET fabrication in special. The techniques employed in this work will be described in detail.

2.1 Fin Definition Methods

The vertical FinFET body – the fin – can be obtained using a variety of different techniques. The main issue is to define sub-100nm lines using the available lithographic equipment and methods. This section focuses on briefly outlining common lithography techniques for fin definition and discussing their advantages and difficulties.

2.1.1 Electron Beam Lithography

Electron beam lithography (EBL) is the method of choice for initial prototype fabrication, not only FinFETs, but other proof-of-concept devices and techniques as well. The first FinFETs fabricated employed e-beam lithography for fin definition and source and drain pads (HUANG et al., 1999; HISAMOTO et al., 2000).

Flexibility in pattern generation, since lithography is performed by direct writing, which eliminates the need of physical masks. Very fine lines below 10 nm can be achieved using e-beam lithography (GRIGORESCU et al., 2007; MANFRINATO et al., 2013). Electron forward scattering and backscattering leads to beam spread when electrons interact with the e-resist and even pattern size variations (CONSTANCIAS et al., 2013). This increases pattern roughness and results in line edge roughness which compromise smaller features (VIEU et al., 2000). For FinFET fabrication, it results in fins with uneven width, wich in turn degrades the output characteristics of the transistors. To reduce the effects of scattering upon the resist, that result in line width roughness and line edge roughness, very thin resists are employed. This, in turn, compromise future sample processing, since thicker resist layers are often needed for lift off and etch steps. Another option, is to separately adjust the exposure dose for each feature, accounting for proximity effects in order to properly define the featues with minimal roughness (TSENG et al., 2003).

While electron beam lithography is very attractive for prototyping, mask and mold fabrication, and research and development (James Watt Nnanofabrication Centre, 2014), the low throughput makes this technique undesirable for high scale manufacturing. To address this issue, multiple beam tools are being developed to increase processing speeds

(CHANG et al., 2001), with different approaches being evaluated, such as the micro-column multiple e-beam (DU et al., 2016) and the reflective electron beam lithography (REBL) (MCCORD et al., 2012). While these systems are still in the development phase, interesting opportunities are expected for multiple beam systems in critical lithography steps (LIN, 2012).

2.1.2 193nm Immersion Lithography

Big manufactures and research institutes use multi million dollars 193nm immersion lithography along with ashing and reactive ion etch (RIE) optimizations for fin definition. Some examples of fabricated FinFETs using this technique are demonstrated by IBM (KEDZIERSKI et al., 2003), IMEC (DAL et al., 2007), Intel (KAVALIEROS et al., 2006; AUTH, 2012; NATARAJAN et al., 2014) and TSMC (WU et al., 2010a). While the reported technology is 193nm immersion lithography, other methods are also frequently employed for the fin definition and other structures as well, such as double lithography double etch (LELE) and self aligned double patterning (MAENHOUDT et al., 2008) – herein called spacer lithography.

One way to obtain smaller structures using the same laser source is to replace the medium between the lenses and the wafer. When switching from air to a higher refraction index fluid, the system numerical apperture is increased, and thus the resolution and focal depth (SMITH et al., 2004b). Using water as an immersion fluid reduces the effective wavelength of 193nm radiation by 30% (SANDERS, 2010). Immersion lithography enables the patterning of sub-45nm features (SMITH et al., 2004a) and even sub-10nm when applied in conjunction with other techniques such as multiple patterning (OWA et al., 2014) and directed self assemby (JEONG et al., 2013).

Challenges remain, however, when immersion lithography is employed. The fluid has to be extremely homogeneous, free of bubbles and particles, that damage the final pattern (LIN, 2006). Moreover, scaling using 193nm immersion lithography can only achieve certain dimensions and remain viable. Beyond the 14nm technology node, extreme ultraviolet lithography (EUVL) provide important reduction of process complexity – and cost (RONSE et al., 2012).

2.1.3 Spacer Lithography

Spacer lithography is often used for fin definition, since it provides reduction of the minimum features obtained by optical lithography (JUNG et al., 2006). Most nostably, FinFETs have been fabricated using spacer lithography and RIE for the silicon etch step (CHOI et al., 2001; CHOI et al., 2002b; DEGROOTE et al., 2007; KIM et al., 2013), and also using TMAH wet etch for highly anisotropic silicon etching (LIU et al., 2003;

JOVANOVI et al., 2010).

Spacer lithography, also called sidewall image transfer (STI) or self aligned double patterning (SADP) has been applied in NAND flash (BENCHER et al., 2008), due to the simple layouts, but also in SRAM fabrication (BASKER et al., 2010) and back end of the line (BENCHER et al., 2011). Beyond expanding the resolution limit, spacer lithography also reduces line width roughness.

The generic spacer fabrication flow is presented in Figure 7. A mandrel of sacrificial material is lithographycally defined. The mask layer is deposited by chemical vapour deposition (CVD) and subsequently plasma etched to leave thin spacers on the side of the sacrificial layer. This is then selectively removed, usually by wet etching, to leave the free-standing spacers. The final fins are obtained by etchin the silicon, using the spacers as etch masks, and then removing the spacers. We can see that the pattern density is doubled (one mandrel becomes two fins) and the final fin width is controlled solely by the thickness of the deposited film that forms the spacers. Since deposition thickness is more easily controlled than optical lithography line edge roughness, the resulting patterns present lower width variations. Structures with 15nm half pitch presenting line width roughness as low as 1.5nm and line edge roughness of 2.5nm have been reported for self assembled double patterning after process optimizations (XU et al., 2013).

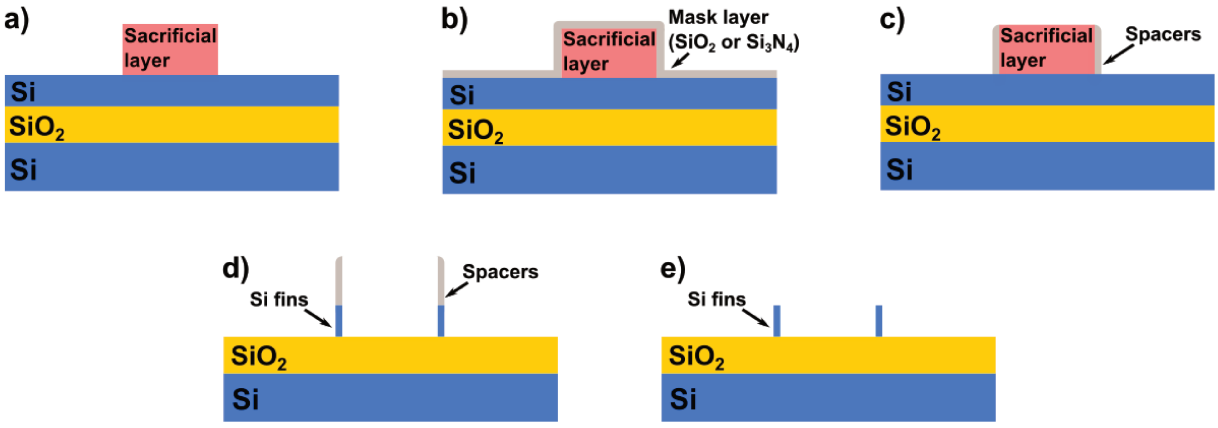


Figure 7 – Schematic process for fin definition through spacer lithography

2.1.4 Focused Ion Beam Techniques

Ion beam approaches for nanopatterning have gathered considerable attention in the last few years, with improved controllability and versatility (BAGLIN, 2012). When comparing to electron beam lithography, considerable advantages are observed due to the reduced lateral scattering, since ions are several order of magnitude heavier than electrons. Low line width roughness and line edge roughness are reported for ion beam lithography, especially when employing low mass ions such as helium (WINSTON et al., 2009; SCHOLDER et al., 2013; LUO et al., 2016).

Ion beam techniques for nanopatterning and nanofabrication are especially interesting due to its flexibility. By tailoring parameters such as ion mass and acceleration energy, a wide range of applications can be addressed(WATT et al., 2005). Focused ion beam for device fabrication has two main approaches: milling and lithography.

2.1.4.1 FIB Fin Milling

Heavy ions such as Gallium are specially suited for patterned material sputtering, also known as milling. Several works have been performed using milling and ion-assisted material deposition for 3D transistor fabrication (POTT; IONESCU, 2006; LIMA et al., 2013; SANTOS et al., 2013; LIMA et al., 2015). Three dimensional fins can be obtained by defining and etching the transistor active region using conventional lithography and subsequently using the focused ion beam to remove the silicon on the channel until only a thin fin is left. Figure 8 schematically presents this process. An aluminium thin layer is used as the etching hard mask and left on the sample during the milling step to allow better contrast.

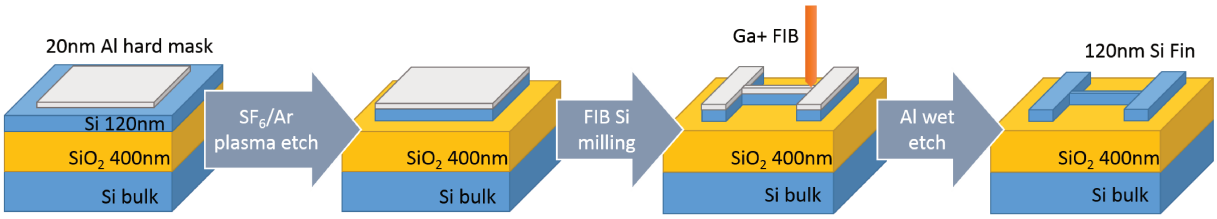


Figure 8 – Schematic process for FIB fin milling

This method presents some disadvantages, however. First, a single beam FIB system is inherently serial, which is, the transistors are fabricated one at a time. This limits the maximum number of devices that can be fabricated, due to time (and thus cost) constraints. Second, to obtain fins with sub-100nm width, very low beam currents have to be used. Lower beam currents result in lower sputtering yield, and thus the milling process requires very long time. Third, the focused Ga^+ beam, when interacting with the sample, not only sputter surface atoms, but also implant ions from the beam itself (VOLKERT et al., 2007). When using silicon substrates, this implanted gallium alters the doping levels, since Ga is an acceptor ion in silicon. Focused ion beam systems using hellium ions solve this last issue, and significant results have already been presented (WINSTON et al., 2009; SCHOLDER et al., 2013; LUO et al., 2016). In this work however, a Ga ion beam is used, which is relevant both for the Ga^+ FIB Lithography method and for the discussion regarding Ga incorporation in the samples.

2.1.4.2 Al Hard Mask FIB Milling

In order to solve some of this issues, a new technique for fin definition using Ga^+ FIB milling is proposed in this work, where only a shallow milling is performed to remove

the aluminium hard mask on top of the transistor channel, leaving only a thin strip that becomes the fin after RIE. Since the milling depth is reduced, lower processing times are required to produce the same device, when comparing to the fin milling technique. The lower processing time also relates to lower Ga^+ implanted dose in the sample. The schematic process is presented in Figure 9.

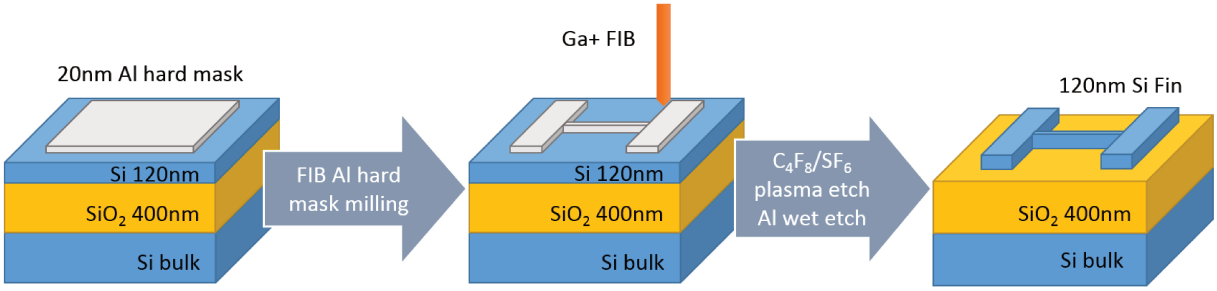


Figure 9 – Schematic process for FIB Aluminium hard mask milling

Although promising, this method assumes that the silicon just beneath the milled aluminium layer etches at the same rate – or near – as the bare silicon elsewhere on the sample. This was experimentally determined in this thesis as not being true, and in fact, Ga^+ ion irradiation of silicon can lead to nanopillars as tall as 800nm when using fluorinated plasma etch chemistries such as C_4F_8/SF_6 or SF_6/Ar (HENRY et al., 2010). This etch masking, in turn, can be used for the fin definition itself, and is the last method discussed.

2.1.4.3 Ga^+ FIB Lithography

Ga^+ ion irradiation os silicon can be adopted as a maskless and resistless lithography method for nanoscale multiple fin definition. While this technique has already been employed for micro electro-mechanical systems (MEMS) (CHEKUROV et al., 2010), in this work it is used for FinFET prototype fabrication for the first time. The Ga^+ FIB lithography relies on the formation of a thin non-volatile mask on the silicon regions irradiated by the Ga^+ ions, when exposed to a fluorinated plasma such as SF_6 and Ar. The time required for the multiple fin definition by combining the Ga^+ FIB lithography and SF_6/Ar plasma etch techniques, is drastically reduced when compared to the traditional Ga^+ FIB milling.

The multiple fins are defined using surface modification through Ga+ shallow implant on silicon. Using a 30KeV focused ion beam, a 20nm layer of silicon is incorporated with Ga ions (VOLKERT et al., 2007). This incorporation is associated with material sputtering, and thus we call the process of patterned Ga implantation FIB shallow cuts. Figure 10 presents the schematic for the multiple fin definition. The Ga incorporated in the sample, in fluorinated plasma such as SF_6/Ar, creates a thin GaF_x non-volatile mask that protects the fins from etching (HENRY, 2010; HENRY et al., 2010).

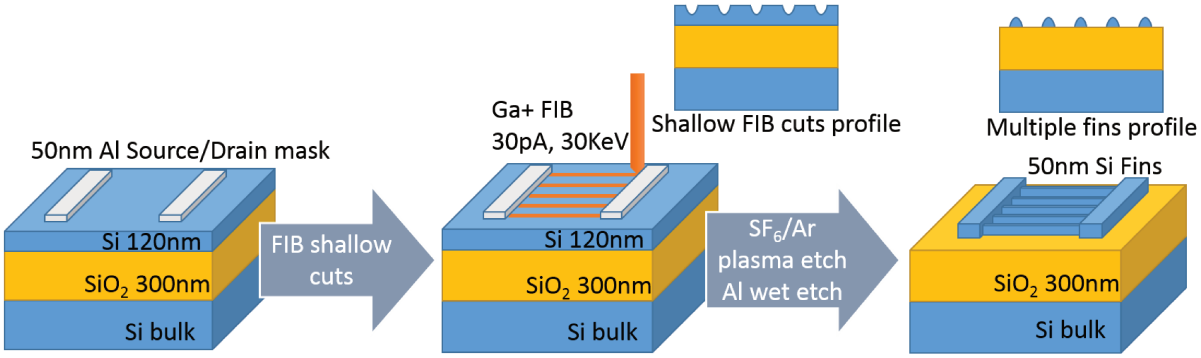


Figure 10 – Schematic process for Ga^+ FIB lithography

When compared to other fin definition methods using the focused ion beam, the Ga^+ FIB lithography offers significant advantages. While the fabrication of a single fin using the Al hard mask milling process requires approximately 10 minutes, only 40 seconds are necessary to define nine parallel fins using ion beam lithography. It is still a serial process but the much reduced processing time allows increasing the number of fabricated FinFETs. The device gallium incorporation is also drastically reduced, as will be later discussed. An important disadvantage of the proposed method is the material sputtering related to the Ga^+ incorporation, which requires a thicker silicon layer than the desired fin height. It is shown, however, that the fin height can be controlled with adequate accuracy based on the FIB cut depth and silicon layer thickness.

2.2 Thin Film Deposition

Thin film deposition is an essential step of modern IC fabrication flow. A large variety of thin films is necessary to fabricate transistors nowadays, either metals, semiconductors or insulators. Deposited films have to follow strict requirements, such as uniform and controllable thickness and composition, low density of defects and imperfections, excellent adhesion, conformal step coverage and suitable electrical characteristics (WOLF; TAUBER, 1986). Several techniques are used for thin film deposition, owing to their advantages in different aspects needed in IC fabrication. This section will outline the main methods used for thin film formation and focus of the techniques employed in this work.

2.2.1 Atomic Layer Deposition

Although atomic layer deposition (ALD) was introduced in (SUNTOLA; ANTSON, 1977), the widespread adoption occurred when film conformality and precise thickness control became strict requirements. The transition from SiO_2 gate dielectrics to high-κ materials – that will be discussed in the next section – much increased ALD importance in the microelectronics industry (MISTRY et al., 2007). The FinFET design

has also been readily implemented partly due to the excellent conformal films provided by ALD (AUTH, 2012; JOHNSON et al., 2014). Furthermore, the main disadvantage ALD presents – the low deposition rate – has become less important as required film thickness have decreased and thickness control has in turn gained importance (LESKEL; RITALA, 2002).

The ALD process consists of sequential alternating pulses of vapour phase chemical precursors that react with the substrate. These individual gas-surface reactions are called "half-reactions" and appropriately make up only part of the materials synthesis. During each half-reaction, the precursor is inserted in the chamber reacts with to the substrate surface in a self-limiting manner, saturating the exposed surface and leaving no more than one monolayer. The first half reaction is purged and and the next chemical species are inserted, which react to the adsorbed monolayer and create a single layer of the desired material. ALD processes are performed at relatively low temperatures (<350°C), and the temperature range where the growth is saturated is called the "ALD temperature window" and depends on the utilized precursos (JOHNSON et al., 2014). Due to the self limiting nature, the films are highly uniform, conformal and continuous. Since each cycle deposits a single material layer, excellent thickness control is achieved (GEORGE, 2010). Several precursor gases have been developed to deposit a wide range of materials, including gate oxides, transition-metal nitrides for gate electrodes and metals for interconnections such as copper and ruthenium and even semiconductor materials (LESKEL; RITALA, 2003; GUO et al., 2015; MINJAUW et al., 2015; AHADI; CADIEN, 2016; SCHWARTZBERG; OLYNICK, 2015).

One of the limitations of ALD is related to film contamination arising from the non-reacted precursors incorporated in the film(LESKEL; RITALA, 2003; KIM, 2003; WU et al., 2010b), which can be controlled by changing the process temperature and improving the purge steps. Also, the materials that can be deposited are dependent on the available precursors. Furthermore, ALD depends on the chemisorption of the first pulse of precursors to the substrate surface, and for this active sites need to exist in this surface (PUURUNEN, 2005). For some chemistries employed, certain substrates require an additional step of surface preparation, prior to material deposition (POMAREDE et al., 2003).

2.2.2 Metal Evaporation

While evaporation has been phased out in the semiconductor industry, it still retains a degree of importance for research purposes (NISHI; DOERING, 2000). Evaporation tools are either thermal, with a tungsten filament heating the source material, or based on an electron beam (e-beam) as a heating source. In both cases the material to be deposited is heated above its boiling point and evaporates. When the vapour reaches the

sample it condenses and forms a continuous thin film. Electron beam evaporators reach higher temperatures, which allows the deposition of a wider range of materials. Furthermore, the source material is only melted in a small spot, where the electron beam is focused, reducing the contamination from the crucible that holds the material. Evaporation is performed at ultra high vacuum, which improves film purity and reduces gas phase scattering. Deposition of alloys is challenging, since different metals have different vapour pressures and thus their evaporation rate is also distinct. A multiple e-beam system can be used for this purpose, with adjusted beam energy to match the deposition rate of different materials (PLUMMER, 2009). The main disadvantage of e-beam evaporation is the poor step coverage, leading to non-conformal films. Perfect step coverage is specially important for 3D transistor fabrication, where the gate dielectric and gate electrode have to envelop the fin, in the case of FinFETs. Another serious concern regarding e-beam evaporation, is the radiation damage, originating from the highly excited electrons that arrive in the material being evaporated decaying back to the core levels (CAMPBELL, 2001). The x-rays can cause oxide traps that reduce MOSFET performance.

In this work e-beam evaporation is employed to deposit ultra thin films (few angstroms thick) of titanium and aluminium. The system reaches ultra high vacuum of 10^{-8}Torr, which allows high deposition rate control, low contamination in the films, and low substrate damage resulting from high energy atoms. The evaporated metallic films are subsequently treated modified by plasma treatments, that will be discussed in a following subsection, to become either different compounds or even dielectrics.

2.2.3 Sputter Deposition

Sputtering is a process in which ions are accelerated into a surface in order to remove atoms from that surface. Sputter deposition relies on the ejected atoms condensing on the desired substrate, forming a thin film. It is most widely used for metal deposition, but can also be employed for insulators (SIMON, 2012).

Argon is typically used as the bombardment species, which is accelerated to the target. Upon collision with the surface, atoms from the target ejected and travel with high kinetic energy to the substrate, condensing and forming the thin film. The impinging ions need sufficient energy – in the range of 50eV to 2KeV – in order to sputter target atoms, but at higher energies – 2KeV to 50KeV – the incident particle creates a cascade of collisions that breaks several atomic bonds and is not convenient for thin film deposition. Above 50KeV, ion implant is predominant and the sputter yield is significantly reduced (ROSSNAGEL, 2003).

The high kinetic energy of the sputtered atoms, when reaching the substrate surface is the main factor for the improvement in step coverage, when compared to evaporated films. The sputtered atoms have high surface mobility and can condense in smooth,

conformal and continuous films more easily than when evaporation is performed. The characteristic non-directionality of sputter deposition further improves film step coverage (ROSSNAGEL, 2003). Despite its advantadges, high energetic atoms can cause damage in thin films or sensible structures upon which the sputtered atoms are being deposited (LUJAN et al., 2002)

A magnetic field can be added parallel to the target, using permanent magnets, to confine secondary electrons in cycloidal orbits near the target surface. The probability of ionizing colizions is greatly increased, which results in a denser plasmas near the target (MCLEOD; HARTSOUGH, 1977; WAITS, 1978; SIMON, 2012). A schematic of a magnetron sputtering system is presented in Figure 11, using an aluminium target as an example. A denser plasma produces more ion collisions, and thus more target material is sputtered, increasing the deposition rate. With the increased plasma ionization provided by the magnetron arrangement, the plasma can be maintained at lower pressures, which in turns increases the mean free path of sputtered atoms (KELLY; ARNELL, 2000).

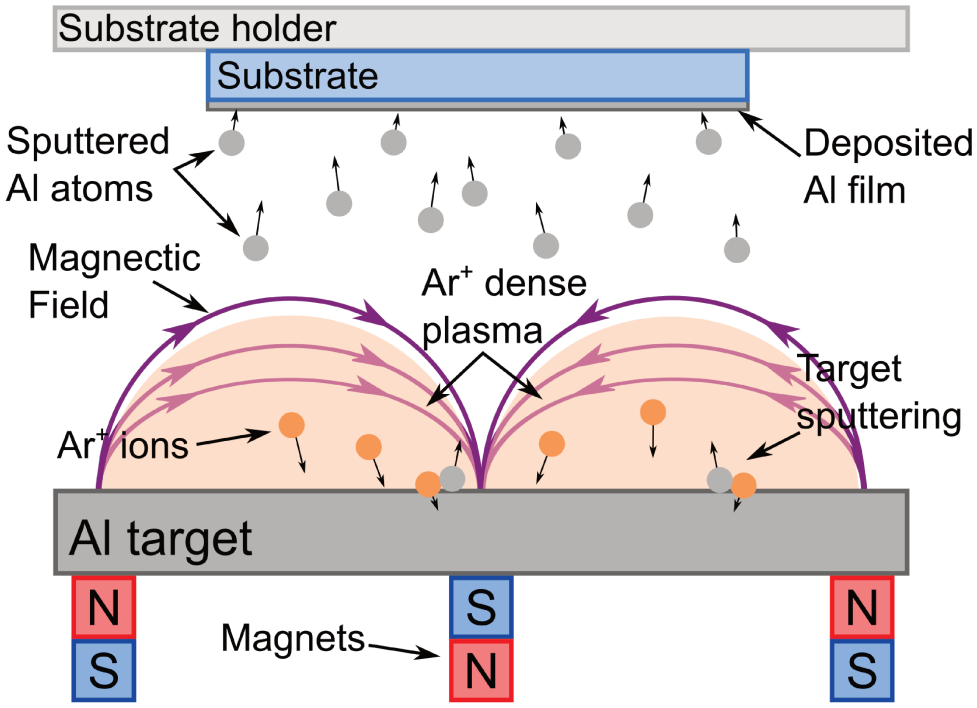


Figure 11 – Schematic of the magnetron sputtering system

Using the same material target, different compounds can be deposited if the reactive sputtering method is used. In this method, a pure metallic target is sputtered and the metal atoms are reacted with the appropriate gas at the sample surface – nitrogen or oxygen, for example – to form the desired compound – TiN, TaN, Al_2O_3, TiO_2 and others. Reactive sputtering has its own challenges, nonetheless. Maintaining high deposition rates while controlling compound stoichiometry is not achieved by simply increasing the reactant gas flow, since the formation of the compound in the metallic target – known as target poisoning – normally reduces the sputtering and deposition rate. Many interde-

pendent parameters can render the deposition process unstable, requiring carefull process monitoring (SAFI, 2000; SPROUL et al., 2005).

In this work, most of the metal are deposited by sputtering. Aluminium is used for hard masks, cap layers and contacts, and TiN is used as gate electrode of part of the fabricated transistors. TiN is deposited by the reactive sputtering process developed in the work presented in (LIMA, 2011).

2.2.4 Plasma Surface Treatment

Plasma surface treatment consists of subjecting a given material to a plasma with specific characteristics – low power, high density and high percentage of N_2, for example – in order to enhance certain characteristics of the material or even convert it to another compound. This technique is used for a variety of applications, from modification of industrial metal coatings, to modern CMOS dielectric formation and low temperature 2D semiconductor synthesis. An important advantage of plasma treatments, as opposed to thermal surface modifications relates to the thermal budget. The thermal budget is the total thermal energy the IC receives during fabrication. Lower thermal budget processes are needed in order to obtain shallow and abrupt junctions in modern CMOS transistors (KALAVADE; SARASWAT, 2000; SHARMA et al., 2014)

Heavy industries use plasma surface treatment to increase mechanical properties of metals such as stainless steel (LARISCH et al., 1999; MENTHE et al., 2000). It can be used to convert the surface of titanium substrates to titanium nitride (TiN and Ti_2N), which also increases its hardness and wear resistance (MURALEEDHARAN; MELETIS, 1992). Another use for plasma surface modification is to increase metal coating hydrophilicity, which improves subsequent paint adhesion (SHIN et al., 2007)

Plasma nitridation can be used to form a thin barrier layer above the gate dielectric that prevent diffusion of the polysilicon gate dopant to the oxide layer and semiconductor substrate (ARONOWITZ et al., 1998). In the late years of SiO_2 thickness scaling, the oxide reliability was increased by nitrogen incorporation, which could be achieved using plasma nitridation and subsequent annealing (HATTANGADY et al., 1996; NICOLLIAN et al., 2000). The next step, SiON as a gate dielectric for MOSFETs can be achieved by a variety of means. Notedly, using plasma surface treatment, silicon oxynitride can be obtained by plasma nitridation of SiO_2 (KRAFT et al., 1997; OKUNO; HATTANGADY, 2000), by nitridation of the silicon substrate with background O_2 (OKAMOTO et al., 1995), or by plasma oxynitridation of the silicon substrate (TOGO et al., 2000; TOGO et al., 2002; MANERA et al., 2004). Plasma-nitrided hafnium-silicate (HfSiON) has also been explored as an alternative high-κ dielectric, for its amorphous character even after thermal annealing (QUEVEDO-LOPEZ et al., 2005). Oxidation in Ar/O_2 plasma and nitridation in Ar/N_2 was used in (INUMIYA et al., 2003) to convert the deposited hafnium-silicate

in HfSiON.

Low temperature synthesis of 2D materials is interesting to enable flexible electronic circuits in sensible substrates. In the works presented in (MORRISH et al., 2014) and (O'BRIEN et al., 2014), sulphurisation for 60 minutes in H_2S and Ar plasma is used to convert dielectric WO_3 films in semiconducting WS_2. Thinner WO_3 films, from 2nm to 10nm, are more easily converted in WS_2, which can be explained because plasma treatment is predominantly a surface process rather than a bulk one.

In this work, plasma surface treatment of e-beam evaporated metals was used for TiN and TiAlON thin film formation following garcia (2014), Miyoshi (2008), Miyoshi (). Figure 12 shows schematically how both films are created. Furthermore, SiON for FinFET gate dielectric is grown by oxynitridation using an $Ar/O_2/N_2$ plasma following (OKAMOTO et al., 1995) and (MANERA et al., 2004).

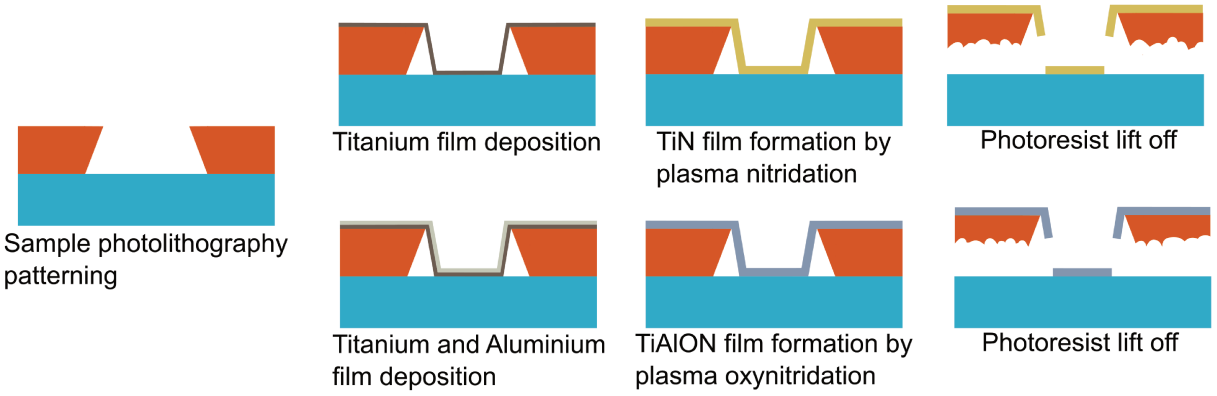


Figure 12 – Schematic of TiN and TiAlON thin film formation by PVD deposition and plasma surface treatment

An electron cyclotron resonance (ECR) plasma system relies on the resonance between the electron cyclotron frequency, due to the applied magnetic field, and the 2.45GHz microwave power source. This results in great effectiveness in plasma generation, due to the higher rate of ionizing electron collisions (CONRADS; SCHMIDT, 2000). Figure 13 presents the ECR plasma system used in this work, with the process chamber, magnetic coil, load capacitors and sample being processed indicated. The plasma is generated above the process chamber, in the region affected by the magnetic coil. ECR systems are specially suited for plasma surface treatment because of the low ion bombardment of the sample, since the plasma is created remotely and streams with low ion energy to the process chamber (ASMUSSEN, 1989). As the deposited metal films have only 1nm thickness, a heavy ion bombardment could lead to sputtering damage and defects in the thin films.

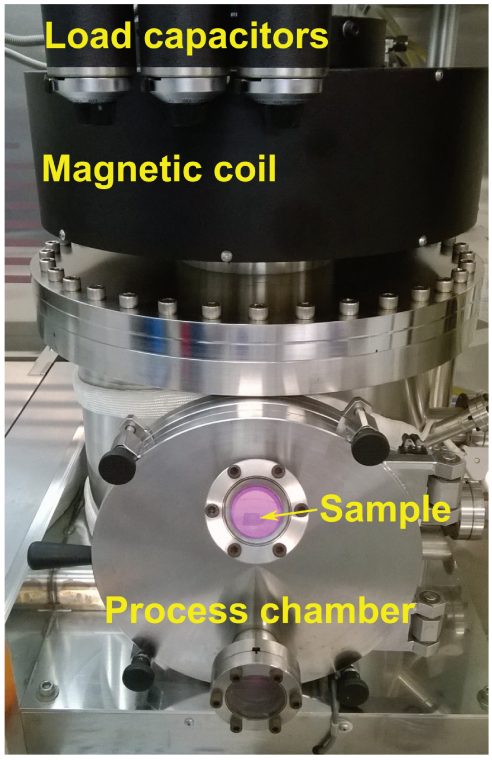


Figure 13 – ECR plasma system used, with its parts indicated

2.3 Gate Stack

MOSFET gate stack evolution is closely related to device scaling and the different technology nodes, pushing for higher capacitance from the oxide and lower resistance from the electrode (OSBURN; HUFF, 2002). In this section, the first part will follow the historical developments, indicate when changes have been made and briefly discuss future trends for the 10nm technology node and beyond. The second part will focus on materials used in this thesis and the reasoning behind those specific choices.

2.3.1 Industry Gate Stack Evolution

Figure 14 presents a simplified schematic of gate stack materials throughout the years and technology nodes. In the first years of the MOSFET technology, 100nm thermal SiO_2 was the typical dielectric, along with aluminium gate electrode (KHANG, 1963).

Ion implantation and polysilicon gate enabled the gate-first fabrication scheme, which provided increased performance and scaling capabilities (KERWIN et al., 1969; FAGGIN; KLEIN, 1970; DENNARD et al., 1974). The polysilicon/SiO_2/Si gave rise to the scaling golden age, where steady process improvements, oxide thickness reductions and lithography advances enabled the transistor to achieve gate lengths of 90nm in the end of 2002 (THOMPSON et al., 2002). From then on, further reducing the transistor dimensions have required important material and interface engineering. Replacing SiO_2

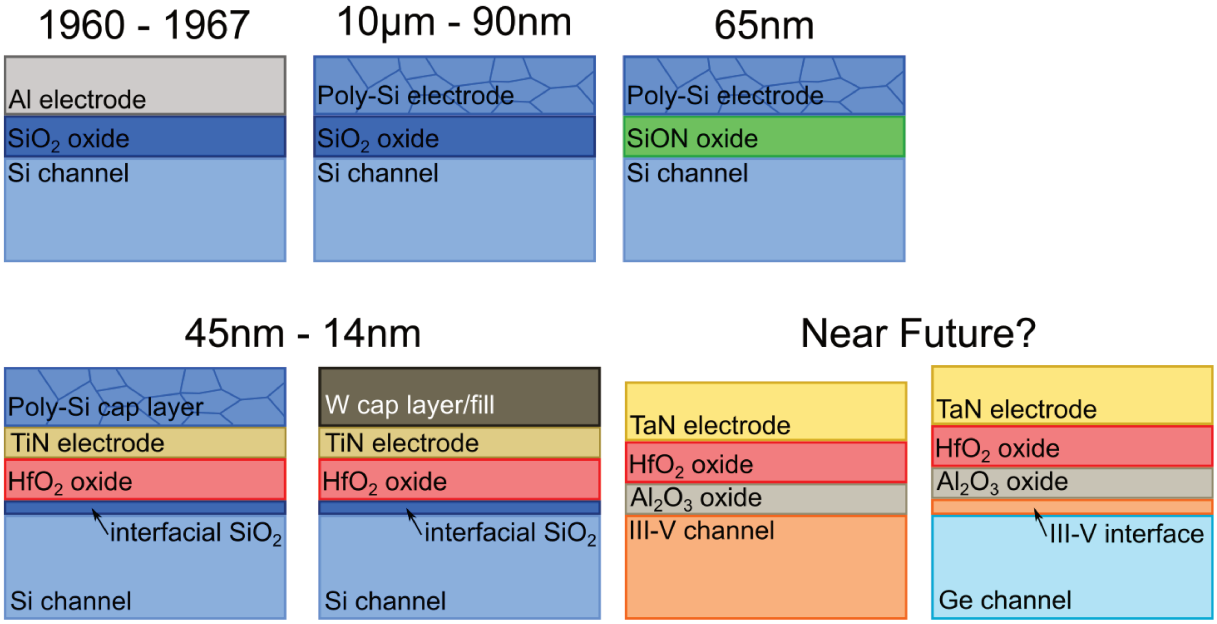


Figure 14 – Gate stack materials evolution throughout the years and technology nodes. A brief example of gate stack structure for future technology nodes is also outlined.

for SiON – along with other process optimizations – enabled the 65nm technology node, but no further, due to prohibitively high oxide leakage currents. Traditional transistor scaling requires oxide thickness reduction along with other dimensions, and at the 65nm node SiON oxide thickness was about 1nm, giving rise to high quantum mechanical tunneling currents (CHEN, 2006). The solution was to employ high-κ dielectric materials such as HfO_2, which allows increasing the physical layer thickness while maintaining its capacitance, and thus reducing the oxide tunnelling currents.

Some issues arise when changing the SiO_2 (or SiON) dielectric for a high-κ one. First, the thermal Si-SiO_2 interface presents very high quality, with low defect density. This is not the case for ALD of HfO_2 on silicon, however, that can have a high density of interface trap states and thus low silicon interface carrier mobility. To improve the silicon-dielectric interface, a thin layer of SiO_2 is used below the high-κ dielectric (CHENG et al., 1999). Other issues, related to the polysilicon gate electrode on top of the high-κ dielectric, is surface phonon scattering and Fermi level pinning. Surface phonon scattering contributes to carrier mobility degradation, and is enhanced when using such dielectrics. Mid-gap metal gate such as TiN successfully screen remote phonon electron interaction, improving the channel electron mobility (CHAU et al., 2004). Fermi level pinning, in turn, is caused by surface states in the metal oxide/polysilicon interface, and leads to transistor V_{th} shifts (HOBBS et al., 2004). Replacing the polysilicon for a metal electrode also solves this issue and enables accurate V_{th} modulation. Moreover, polysilicon remains a semiconductor material, even when highly doped. As such, a depletion layer is present, dependent on the applied bias, which increases the effective oxide thickness – now accounted as the

oxide thickness and the depletion layer width. For deeply scaled devices, the depletion width – between 0.4nm and 1nm – is comparable to the oxide thickness. Metal electrodes do not present depletion layers, and thus solve this issue also. TiN, and TaN to a certain degree, was chosen as the metal gate electrode due to its suitable – and also tunable – work function value and thermal stability (WU et al., 2010c; LIMA et al., 2012; LIMA et al., 2014). The HfO_2/TiN high-κ metal gate stack remain the materials of choice until the current 14nm transistor generation[1] (NATARAJAN et al., 2014), with either tungsten or poly silicon as the cap layer above the TiN electrode, depending on fabrication design decisions (FRANK, 2011).

Some discussion still exists regarding the gate stacks for the 10nm technology node and beyond. Interesting suggestions are to swap the silicon channel for either germanium or III-V compound semiconductors, with higher carrier mobilities. This change will force new materials in the gate stack, to allow adequate stability and reduce the density of interface defects. While both germanium and III-V compounds traditionally present lower quality semiconductor-dielectric interface than the Si-SiO_2, important improvements have been obtained recently. Atomic layer deposition (ALD) of dielectric materials has allowed decent quality gate stacks, and pre-deposition cleaning, interfacial layers, and post-deposition treatments are reported to provide lower interface state density (RIEL et al., 2014; TAKAGI et al., 2015). When III-V channels are considered, one option is to use a thin layer of Al_2O_3 beneath the HfO_2 to improve the interface (YADAV et al., 2015). One option, when using Ge as the channel, is to epitaxially grow a layer of InAlP to achieve high carrier mobilities by confining the electrons far from the high-κ/InAlP interface traps (YEO et al., 2015). Other options remain for future device scaling, from changing the gate stack materials to redesigning its concept entirely – think tunnel FETs and transistors fabricated solely from 2D materials (ROY et al., 2014; COLLAERT et al., 2015)

2.3.2 Alternative Gate Stacks for FinFET prototypes

The FinFETs fabricated in this work use TiN/SiON/Si gate stack for initial evaluations and TiN/TiAlON/Si as an alternative high-κ metal gate stack. Figure 15 presents the two different stacks studied. An aluminium cap layer is employed to reduce oxygen incorporation in the TiN layer, while maintaining low contact resistance.

SiON is used as a control stack, for its similarity to SiO_2, being a material that has already been used in a technology node and for its slightly higher dielectric constant, as well as the reduced thermal budget of growing SiON by ECR oxynitridation (TOGO et al., 2000; TOGO et al., 2002; MANERA et al., 2004). The works presented in (TOGO et

[1] The definition of current technology node here is relative to what is being manufactured. Research institutes are already concerned with 10nm, 7nm and 5nm nodes, for example.

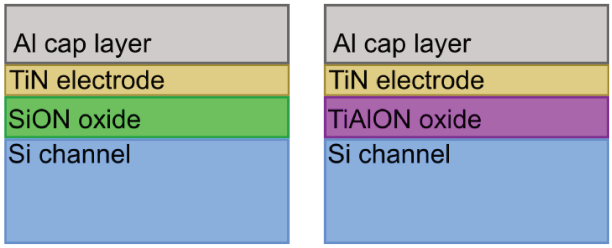


Figure 15 – Alternative gate stacks used in this thesis

al., 2000) and (TOGO et al., 2002) indicate that ultra-thin SiON dielectrics present two orders of magnitude less leakage currents than SiO_2 dielectrics with the same thickness. Both the oxide and transistor reliability are increased tenfold by replacing 1.5nm SiO_2 with 1.5nm SiON.

TiAlON was developed aiming to join the high dielectric constant of TiO_2, of 80, and the high band gap of Al_2O_3, of 8.8eV (ROBERTSON, 2006). It is best described elsewhere, from its development to the morphological and electrical characteristics (MIYOSHI, 2008; MIYOSHI et al., 2010; MIYOSHI et al., 2012). Future of nanoscale CMOS technology depends on further scaling EOT, which requires the replacement of HfO_2 (COLLAERT et al., 2015). One studied option is La_2O_3, not due to its dielectric constant, which is similar to Hf_2, but rather to the formation of La-silicate in the interface with silicon, instead of SiO_2 that is formed when using hafnium. This interfacial layer provides higher dielectric constant than SiO_2, and high electron mobility (KAWANAGO et al., 2012), but its thickness increases with annealing, increasing the total equivalent oxide thickness (EOT) (WONG et al., 2016). Other interfacial layers in conjunction with HfO_2 are also studied, with improved carrier mobility and sub-1nm EOT (LITTA et al., 2015). It is possible to see, thus, that even though HfO_2 has been widely used in the last technology nodes, research on replacement materials is still important. A higher-κ gate oxide is still desirable to further scale EOT while controlling gate leakage currents. Alternative dielectric materials, like TiAlON, are interesting candidates towards this objective, since dielectric constants as high as 1000 have been reported using laminated stacks of Al_2O_3 and TiO_2 (LI et al., 2011), and sub-0.5nm EOT has been achieved using TiAlO hybrid oxide (AUCIELLO et al., 2005). Previous results using TiAlON for planar transistors (MIYOSHI et al., 2010) and 3D capacitors (MIYOSHI et al., 2012) lead us to explore its performance as an alternative dielectric for FinFET devices.

3 Experimental Procedure

In this chapter the experimental procedure carried out for this research is explained in detail[1]. Process optimizations are described and preliminary results are presented when essential for the logical sequence. This is required since three sets of FinFET prototypes have been fabricated, and between each, tests and calibrations have been performed. Those experimental results support changes performed in the fabrication flow of the subsequent FinFET batch.

3.1 Aluminium Hard Mask Milled FinFETs

The process flow for this set of FinFETs is summarized in Figure 16.

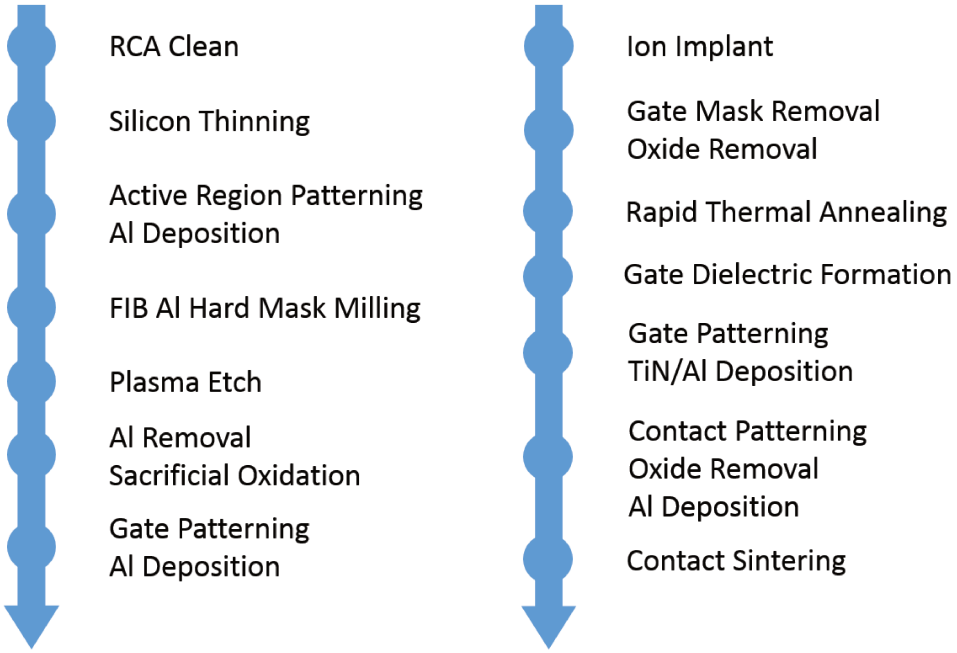
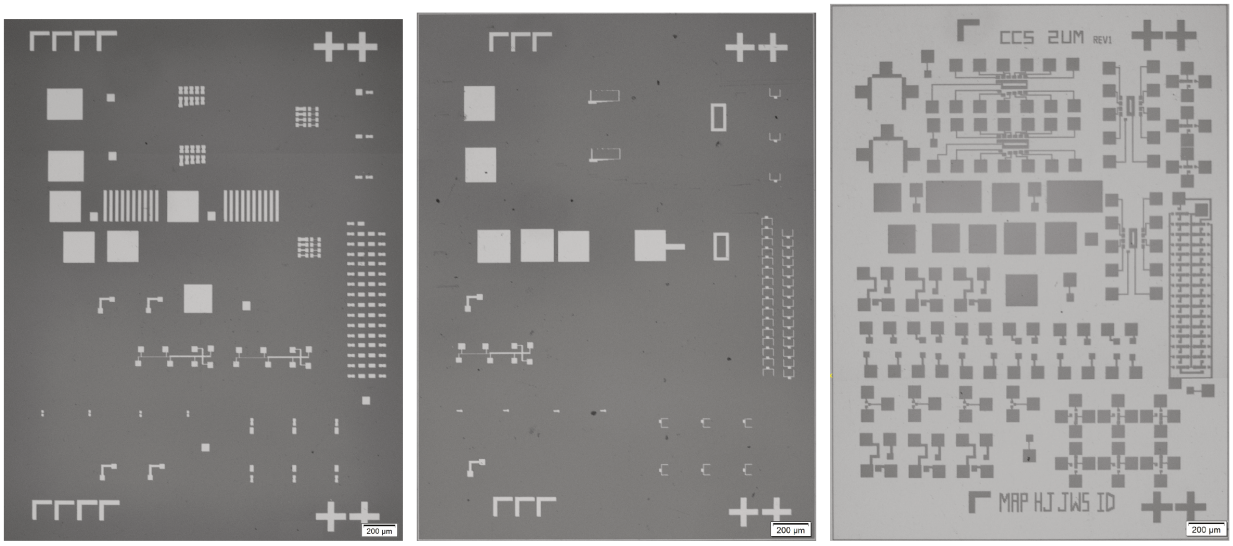


Figure 16 – Summarized process steps for FinFET fabrication

The fabrication process uses the set of photomasks presented in Figure 17 for all the lithography steps, while the fin definition is performed by FIB milling of the aluminium hard mask on the channel. The photomask set was originally fabricated in the work of Grados (2003), for a CMOS fabrication flow. The process steps for this batch of FinFETs is described in detail in the following pages.

The starting SOI substrate has 400nm buried oxide and 340nm silicon layer on top provided by the lab technicians. Since the desired fin height for the FinFETs is 100nm, ap-

[1] Most of the experimental part of this work has been performed at CCS Nano, with the help of staff and other students, for which we are thankful.



(a) Mask for the active area (b) Mask for the gate (c) Mask for the contact pads

Figure 17 – Set of photomasks used for the FinFET fabrication.

proximately 240nm of silicon should be etched before processing. This is achieved through oxidation of the silicon layer and wet etch of the SiO_2 in hydrofluoric acid (HF). The first step is to perform a complete RCA wafer clean process (KERN, 1990), following the steps on Table 1.

Table 1 – Complete RCA wafer clean process

Solution	**Temperature**	**Time**	**Comments**
H_2SO_4/H_2O_2 (4:1)	80°C	10 minutes	Organic residue removal.
HF/H_2O (1:10)	23°C	10 seconds	Dip to remove the SiO_2 created in the previous step.
$NH_4OH/H_2O_2/H_2O$ (1:1:5)	80°C	10 minutes	Organic and particle contamination removal.
$HCl/H_2O_2/H_2O$ (1:1:5)	80°C	10 minutes	Metallic contaminants removal, as well as fine polishing.

The wet oxidation step that follows is performed in a furnace at 1000°C and described in Table 2.

The wet oxidation provided an oxide with average thickness of 495nm, with 4.31% of standard deviation, according to ellipsometry measurements. 44% of the oxide thickness, or approximately 217nm, is consumed from the silicon layer. The removal of this oxide leaves the SOI wafers with a 123nm silicon layer on top of the buried oxide.

Following the silicon layer thinning, the active region is defined using the mask shown in Figure 31b, using the lithography steps presented in Table 3 for the lift off process. A thin film of 20nm of aluminium is sputtered on the wafer in order to create an etching hard mask.

Table 2 – Wet oxidation process

Ambient	**Temperature**	**Time**	**Comments**
N_2	600°C	3 minutes	Temperature ramp up to prevent warping
N_2	1000°C	5 minutes	Temperature stabilization in a neutral ambient
O_2	1000°C	5 minutes	Dry oxidation to prevent stacking faults (QUEISSER; LOON, 1964)
H_2O	1000°C	90 minutes	Wet oxidation
N_2	1000°C	10 minutes	Increases the density of the oxide by removing the H_2 resulting from the wet oxidation step (PLISKIN; LEHMAN, 1965)
N_2	600°C	3 minutes	Temperature ramp down to prevent warping

Table 3 – Photo-lithography process

Process	**Parameters**
Hexamethyl Disilazane application to improve the resist adhesion to the substrate	4000rpm, 30s, 60s rest
AZ5214 resist application	4000rpm, 30s
Soft bake for the resist densification	4 minutes at 90°C
UV light exposure	CMOS REGAT mask (17a), 6 seconds
Resist inversion in the hot plate	1 minute 45 seconds at 110°C
UV light flood exposure	No mask, 40 seconds
Development	Metal ion free (MIF) 300, 16 seconds, deionized water

The sample is then processed using the Ga^+ FIB such as to remove the aluminium hard mask in the channel of the chosen devices, leaving only a thin strip that will be the fin after plasma etching. Table 4 presents the parameters used for the aluminium milling and the resulting with of the aluminium thin strip. Figure 18 shows the resulting device, with the aluminium mask milled and a thin strip of aluminium to form the fin. The processing time for each device is around 10 minutes using the presented parameters.

Table 4 – FIB parameters for Al hard mask milling

Beam Energy	**Beam Current**	**Milling depth**	**Milling gap**	**Resulting width**
30kV	30pA	60nm	150nm	**30nm to 100nm**

After both SF_6/Ar and C_4F_8/SF_6 plasma etch it was observed that the regions where the milling was performed were etched differently that the remaining silicon, contrary to what was expected. Further studies on this etching discrepancies were performed and are discussed in Section 3.2.

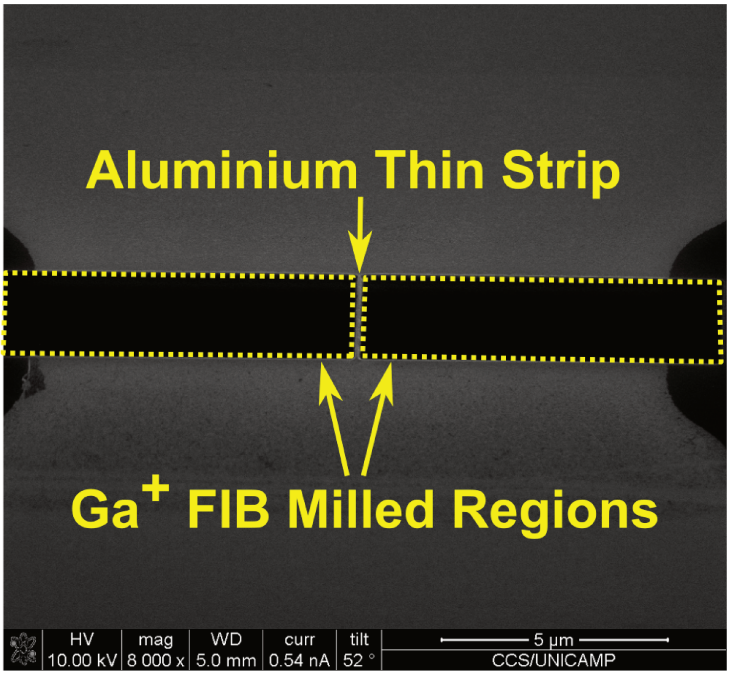
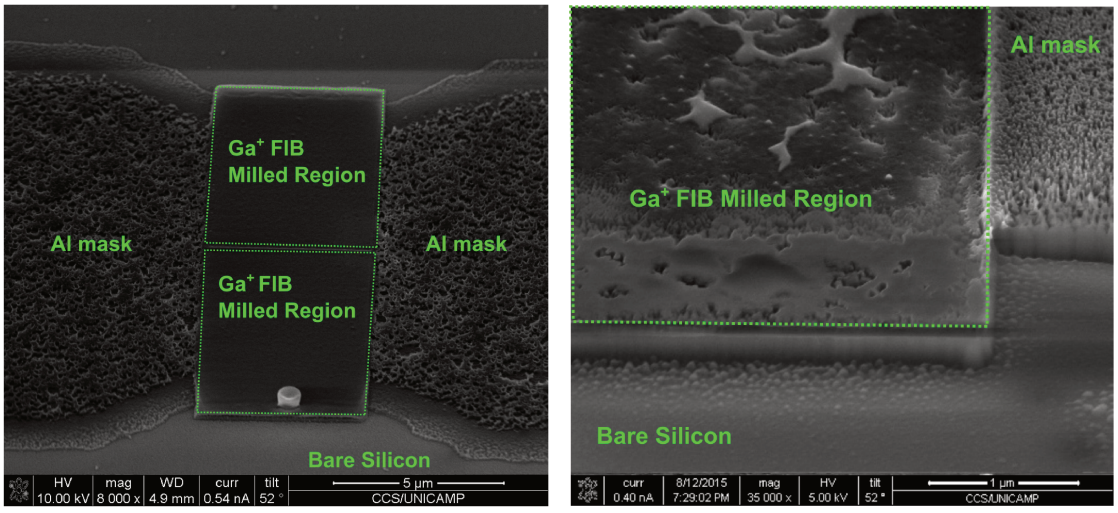


Figure 18 – Resulting etch mask after the milling



(a) (b)

Figure 19 – a) Active region after SF_6/Ar plasma etch. b) Active region after C_4F_8/SF_6 plasma etch. In both cases the etch in the Ga^+ FIB milled regions is different than on the bare silicon, as evidenced by the step on the edge.

Also, after etching, strong traces of gallium remained on the sample, as seen in the EDS mapping in Figure 20. While this serves to support the study on the Ga^+FIB and its effect on the silicon etch, the gallium incorporation in the devices will be further discussed in Chapter 4.

Aluminium hard mask was subsequently removed and three minutes dry oxidation at 1000°C was performed to reduce fin sidewall roughness due to plasma etch (TAKAHASHI et al., 2004). Optical lithography using the mask shown in Figure 17b was used

for gate patterning and 200nm of aluminium as sputter deposited by lift off process to act as an ion implant mask. Phosphorus was implanted to form the source and drain regions of the FinFETs with 30KeV energy, $1x10^{14}$ cm^{-2} dose and 7° tilt. Both aluminium hard mask and sacrificial oxide are stripped by wet etch and rapid thermal annealing (RTA) for 60 seconds at 1000°C is performed to recrystallize the implanted silicon and for dopant activation.

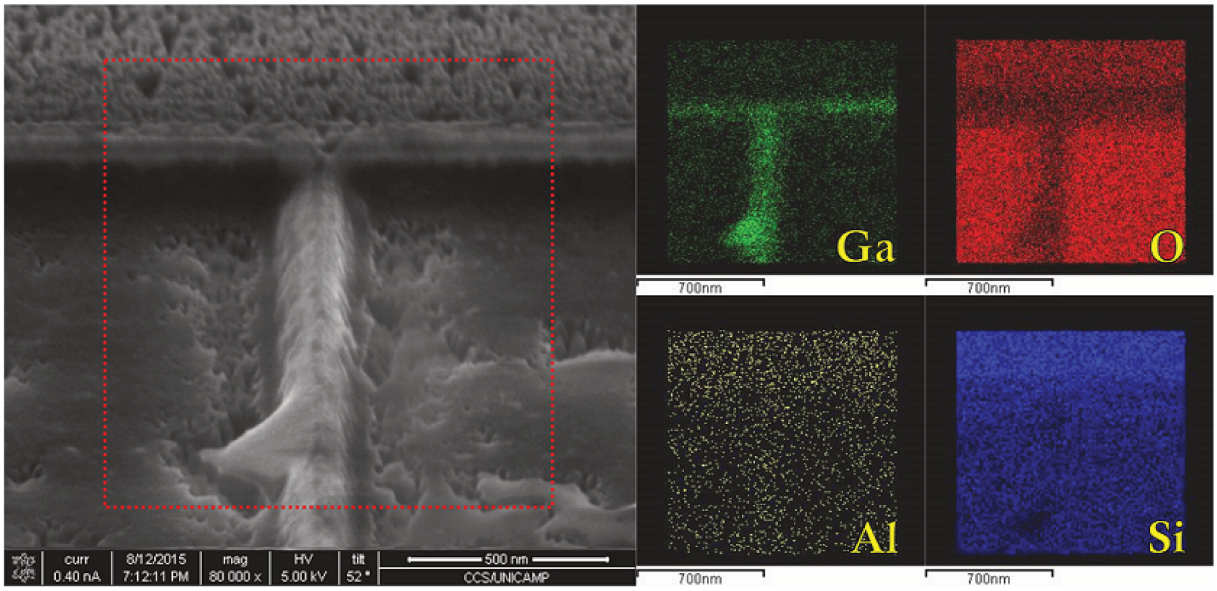


Figure 20 – EDS spectrum of the fin region, showing strong gallium incorporation on the edge of the milled region and on the fin.

Gate dielectric formation follows, with ECR plasma oxynitridation to grow SiON. Gas flows of 3sccm of O_2, 7sccm of N_2 and 20sccm of Ar were used, following previous works, with ECR power of 425W and 5mTorr process pressure, for 20 minutes (MIYOSHI, 2008; SANTOS, 2013). An array of capacitor dots with 200µm of diameter in p-type bulk silicon is fabricated in parallel with the samples for the evaluation of the gate stack C-V characteristics without the influence of other parameters, such as random gallium incorporation and fin dissimilarities. The transistor gate is patterned again and 20nm of TiN with a 100nm Al cap layer is deposited by DC reactive sputtering. The cap layer is deposited *in situ* to prevent oxygen incorporation in the metal gate (LIMA et al., 2013; LIMA, 2015).

Metal contact pads are formed by optical lithography followed by resist hardening for 20 minutes in the hot plate at 110°C. SiON on the source and drain pads is removed by HF wet etch for 15 seconds just prior to 200nm aluminium sputter deposition.

The fabricated FinFET device is presented in Figure 21, along with a fin cross section. It can be observed that a three-dimensional fin could be obtained with the aluminium hard mask FIB milling method, although its aspect ratio may still be improved. Furthermore, not only the grown SiON cover the fin entirely, but also the TiN layer

and the Al cap layer present no discontinuations, indicating the adequate step coverage of the deposition method. The image blurriness is due to the SEM magnification limit, and a clearer image could be obtained using a transmission electron microscope (TEM) technique.

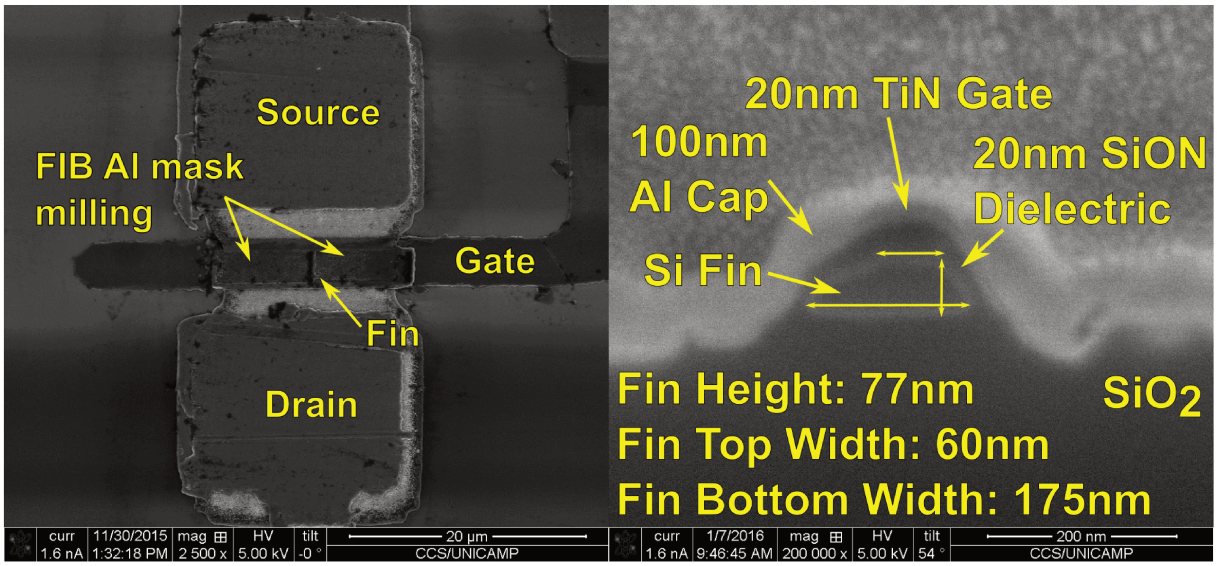


Figure 21 – Fabricated FinFET device, along with fin cross section presenting metal gate coverage of the fin

3.2 Reactive Ion Etch Calibration

3.2.1 Initial Determination of the Ga^+ Focused Ion Beam Effect in the Etching Rate

Three hypothesis were raised to explain the etching rate differences observed in FIB processed regions, when compared to unprocessed silicon. One was that the FIB-induced amorphisation of the underlying silicon leads to lower etching rates, when compared to crystalline silicon. The second hypothesis was that aluminium residues were still left on the sample, even after hard mask milling, which would slowdown the etching process. The last hypothesis was that the gallium incorporation in the silicon, arising from the Ga^+ FIB, would prevent the silicon etch.

Three samples were prepared to be etched in RIE, to test the formulated hypothesis. One control sample, with crystalline silicon and 20nm thick and 47µm wide aluminium lines; a sample with amorphous silicon (with phosphorus implantation) and the same aluminium lines; and a third sample processed in FIB with the same parameters used to cut the Aluminium hard mask for the FinFET fins. All three samples are subjected to RIE SF_6 and Ar etch with 2, 3, 4 and 5 minutes of etching, such as to evaluate the etching rate in different conditions.

3.2.1.1 Control Sample

The control samples were etched for 2, 3, 4 and 5 minutes and later the etching depth was assessed by cross sectioning the sample and measuring. The etching depth results are shown in the graph in Figure 22. The etch rate was obtained from the slope of the linear fit of the measurements in the graph. In the interval from 2 minutes to 5 minutes the silicon etching is nearly linear, which is supported by the reasonably good linear fitting. The y-axis intersection of the linear fit is below zero, which indicates that from zero to two minutes the etching is non-linear. The etching non-linearity can be attributed either to silicon native oxides on the sample surface or to plasma ramp up on the initial moments of etching. Either way, the evaluation of the etching rate in the next samples is performed in the same manner, as the slope of the linear fit of the measurements, ignoring the non-linearities in the initial moments of plasma etching.

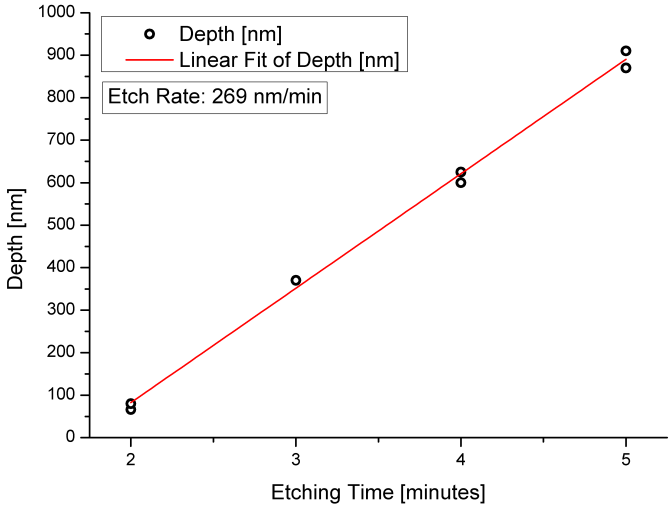


Figure 22 – Etching depth achieved in RIE with different etching times for crystalline control sample.

With this sample we could also analyse the steepness of the sidewall achieved in SF_6/Ar RIE and surface roughness after etching. Figure 23 (a and b) shows that the sidewall has a distinct slope for different etching times, owing to the isotropic characteristics of the SF_6/Ar etch. In Figure 23c it is possible to see how the RIE etching produces severe roughness in the sample. The etching rate of 269nm/min obtained in Figure 22 will be used for comparisons with the other samples.

3.2.1.2 Amorphous Silicon Sample

With this sample we aim to see how the amorphisation induced by the focused ion beam changes the etching rate of the silicon sample in SF_6 and Ar plasma. Since we want to evaluate the gallium effect separately, this sample has phosphorus implantation,

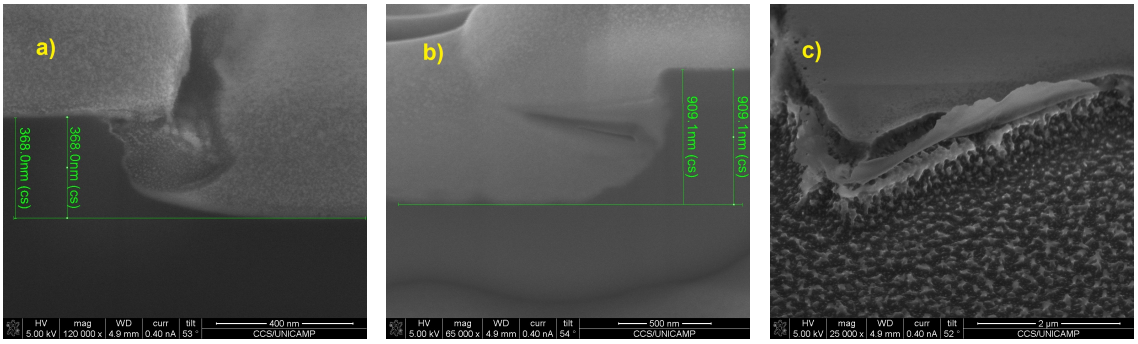


Figure 23 – Etching depth was measured from the step between the aluminium covered and bare silicon regions. Sidewall profile after 3 minutes of RIE (a) and 5 minutes of RIE (b). Silicon roughness after 5 minutes of RIE (c).

but no annealing, such as to remain amorphous. We estimate, by TRIM simulations that the amorphous layer extends for about 70nm or 80nm beneath the surface of the sample, which is much more than the amorphisation induced by the focused ion beam.

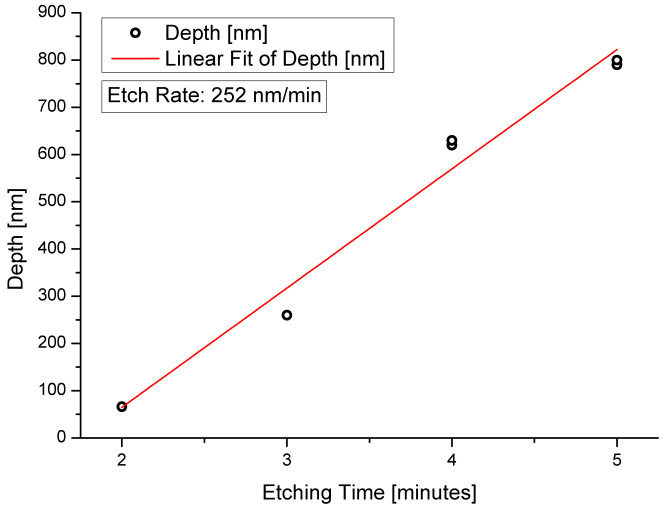


Figure 24 – Etching depth achieved in RIE with different etching times, for the silicon sample with a 80nm amorphous layer.

It can be seen in Figure 24 that the amorphous layer on the surface of the sample has little impact on the etching rate, which changes from 269nm/min in the control sample to 252nm/min in this one.

3.2.1.3 FIB Processed Sample

With this sample we aim to see if the gallium incorporation changes the etching rate of the silicon sample in SF_6 and Ar plasma, or if the source of the differences is the aluminium residues. The sample has the same aluminium lines as the others. It was processed in FIB such as to cut a 7µm X 3µm rectangle half in the aluminium strip, half

on the bare silicon, with 30pA beam current, 1µs dwell time, and 60nm depth – the same parameters used for the fin definition of the previous round of FinFETs. The measured depth after the cut is around 120nm, though. The samples were etched in SF_6/Ar RIE for 2, 3, 4 and 5 minutes and then cross sectioned and measured.

In Figure 25 it can be observed the cross section of the whole region processed in FIB, done in each of the samples to assess the depth differences between the aluminium layer and FIB processed region (1), between the FIB processing in the aluminium stripe and outside the aluminium stripe (2), and between the FIB processed region and the bare silicon region (3).

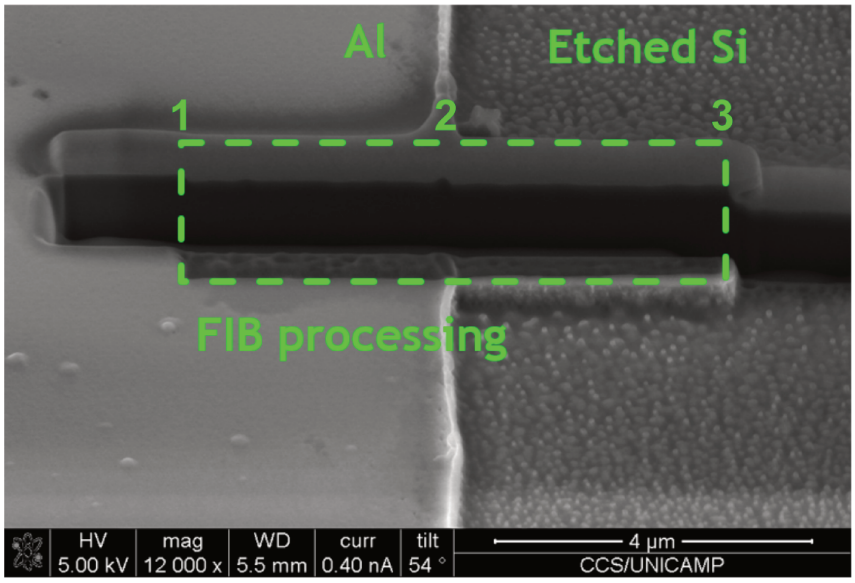


Figure 25 – Cross section of the whole region processed in FIB, including the aluminium stripe and bare silicon region.

When measuring the height difference between aluminium layer and the FIB processed region, which is marked in Figure 25 as number 1, it was found that it was constant for all etching times, around 120nm. This means that removing the aluminium layer with the Ga^+ focused ion beam is not enough to enable normal silicon etching. As evaluated during FinFET fabrication, the milled region does not etch at the same rate as the bare silicon elsewhere in the sample. This can be either caused by aluminium residue or by Ga incorporation hindering the silicon etch. To evaluate which of the two is dominant for the masking effect, the region marked as 2 in Figure 25 is observed. This is the edge between the FIB processing on the aluminium strip and on the bare silicon. There was no significant height difference in this region, even for longer etching times. This means that FIB milled regions that did not have aluminium in any time of the processing still present the masking effect on SF_6/Ar plasma. As such, it is concluded that the dominant etch retardant factor is the gallium incorporation in the silicon. Furthermore, the etching depth between the region milled in FIB and the bare silicon, marked as 3 in Figure 25,

is basically linear with etching time, as seen in Figure 26. The Ga incorporation in the silicon region milled using the focused ion beam creates a mask in the SF_6/Ar the sustains 5 minutes plasma etch and 720nm etch depth.

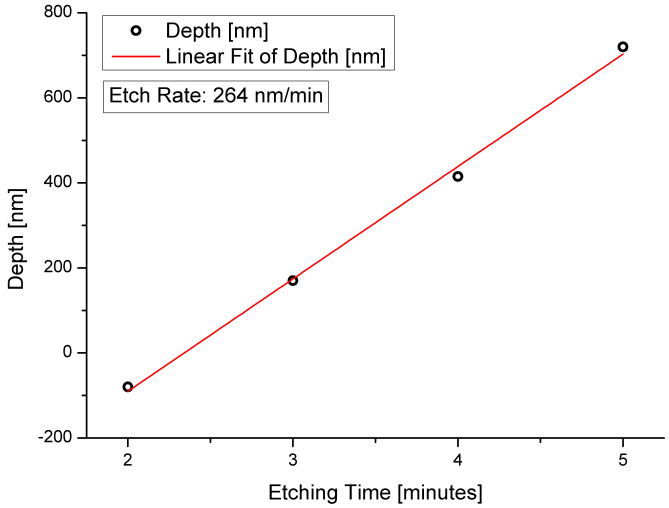


Figure 26 – Height difference between the FIB milled region and the bare silicon for the RIE with different etching times.

This experimental determination raised two important conclusions regarding the etching process. First, the masking agent observed previously is the gallium incorporation in the silicon layer, arising from the Ga^+ FIB processing. This masking factor can be thus used for the definition of multiple fin devices with reduced processing time. Instead of substrate sputtering as in the milling processed, the etch mask can be formed by irradiating gallium ions only on top of the desired fins, as will be discussed in the next section. Second, the capacitively coupled plasma RIE induces a high degree of substrate roughness, as seen in Figure 22c, due to the high energy ion bombardment. An alternative to reduce the etch induced roughness is to switch to the inductively coupled plasma RIE and separately control the forward bias, such as to reduce the ion impinging energy and bombardment.

3.2.2 Ga^+ Masking for Multiple Fin Fabrication

To enable the reproducible fin definition with Ga^+ incorporation, several process parameters have been optimized. The objective is to fabricate thin fins, which give improved electrical characteristics when used for FinFET fabrication. Figure 27 presents schematically the gallium incorporation, as dots, in the silicon layer after a FIB shallow cut. With 30KeV beam energy, Ga^+ ions form a Ga-rich layer of approximately 20nm (VOLKERT et al., 2007). During fluorinated plasma etch, the region with Ga atoms forms a mask which protects the silicon beneath it from etching, thus creating the fins.

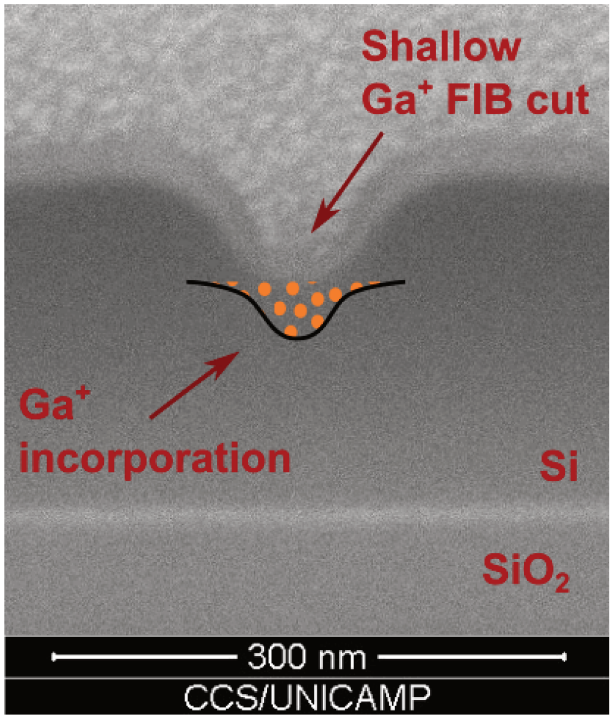


Figure 27 – Cross section presenting a shallow cut made with the Ga^+ FIB and indicating schematically the Ga^+ incorporation in the silicon layer

As such, the fin width is strongly controlled by the distribution of Ga ions which impinge the sample. Maximum Ga^+ incorporation with minimum straggle is desired in order to fabricate fins with minimum width. Different ion beam currents, from 0.5nA to 30pA, have been used and evaluated regarding the fin width after silicon etch. The beam energy was 30 KeV and the cut depth was set as 60nm. All fins were defined in the same sample which was afterwards etched for 5 minutes in C_4F_8/SF_6 plasma. Fin bottom width measurements were performed using FIB/SEM cross sections and measurement tools. Figure 28 presents how the resulting fin width reduces by reducing the focused ion beam current. The insets present cross sections of a fin fabricated using 0.5nA beam current and one using 30pA current in the same scale. For a current of 30pA, knowing that the parallel definition of nine lines of 8µm takes 39 seconds, we can estimate the implanted dose, according to Equations 3.1 and 3.2, where Q is the charge, t the time, q the electron charge and A the implanted area. From the cut cross section we have that the bottom width – where most of the gallium ions are implanted – is 70nm, and thus the total area of the lines is $5.04 \times 10^{-8} cm^2$. The focused implanted dose, with the 30pA current is then calculated as $1.44 \times 10^{17} cm^{-2}$, agreeing with (HENRY et al., 2010) which reports that a dose of $10^{17} cm^{-2}$ allows masking etching up to the depth of 600nm. In the present case the etching depth explores was only up to 340nm, the silicon layer thickness of our SOI substrates, and thus this dose is enough to completely protect the fins during

the silicon etch.

$$I = \frac{dQ}{dt} \tag{3.1}$$

$$Dose = \frac{Q.q}{A} \tag{3.2}$$

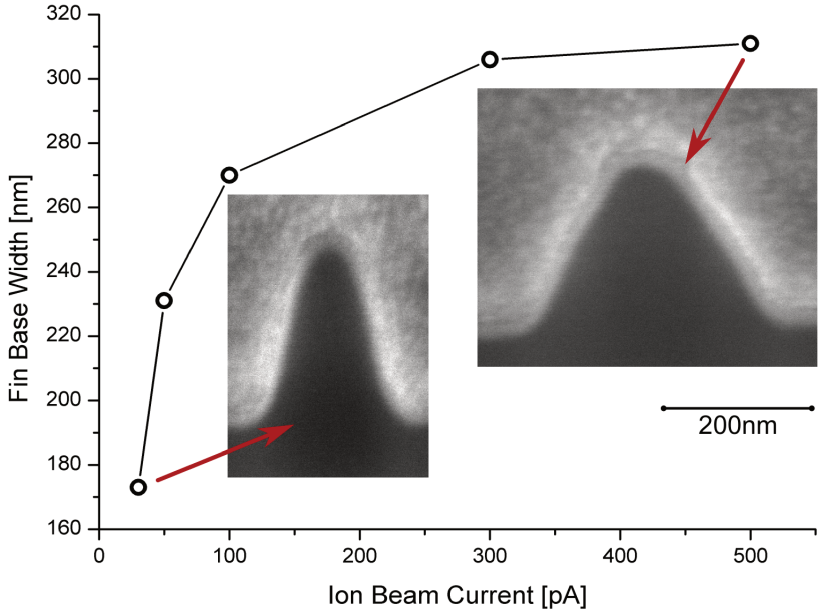


Figure 28 – Evaluation of fin width using different ion beam currents for the fin definition

The resulting fin width is also controlled by the cut aspect ratio. A higher aspect ratio indicates lower ion spread and then higher Ga concentration in the desired region. Increasing the cut depth results in increased aspect ratio. The fin height, however, is controlled, by the remaining silicon layer beneath the shallow cut, creating a trade-off between fin width and height. The nominal cut depth of 150nm – which results in a real depth of 70nm – was found to provide a good compromise between fin width and height. By changing the SOI substrate silicon layer thickness – using wet oxidation to reduce its original thickness of 340nm to any desired thickness – fins with different heights could be obtained, as presented in Figure 29.

The plasma etching step has been optimized in turn, such as to control the etching depth and fin profile from batch to batch. The GaF_x mask has low selectivity and highly suffers from mask sputtering, and thus the etching step has to be carefully optimized. Even though the C_4F_8/SF_6 plasma chemistry provides good etching directionality, it depends on a high sputtering rate to continually remove the polymer formed in the trench bottom and continue etching. As such, it provided high mask sputtering and was find

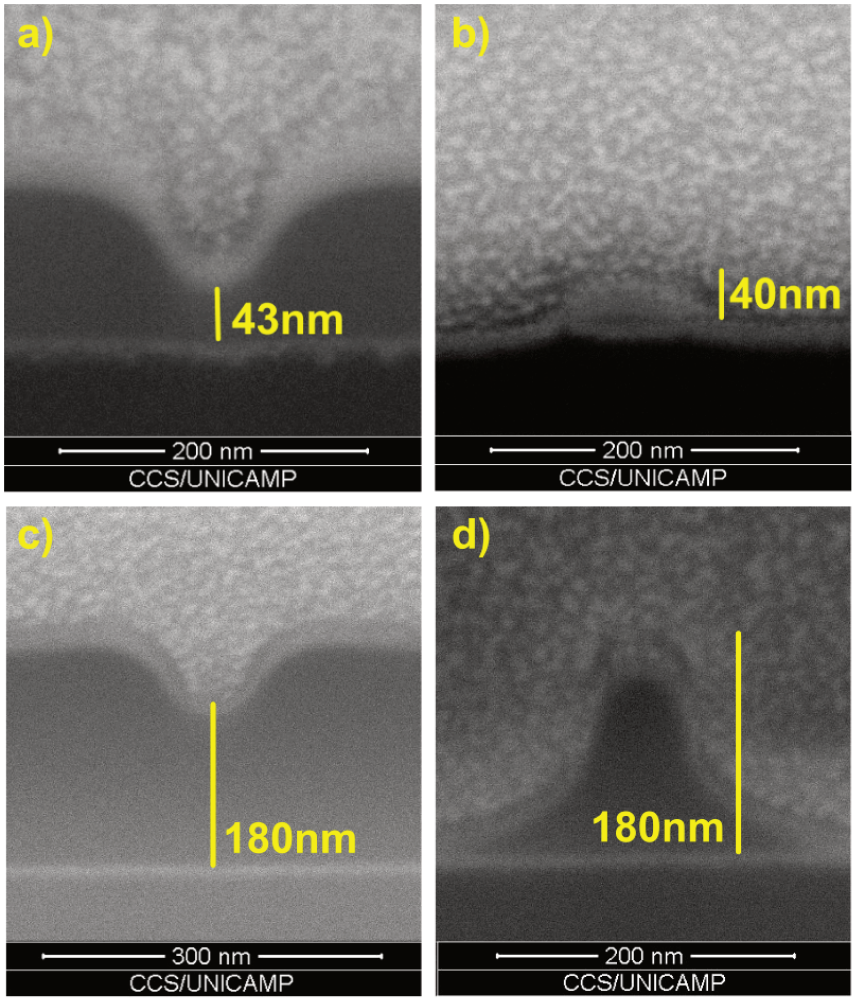


Figure 29 – Cross sections of FIB shallow cut for Ga incorporation (a)(c) and resulting fin after SF6/Ar plasma etch (b)(d), presenting the dependence between the fin height and remaining silicon layer beneath the shallow cut.

unsuitable for this process. Another issue with C_4F_8/SF_6 plasma etch was that for our chamber conditions (26sccm C_4F_8, 12sccm SF_6, 1200W RF power, 12W forward power, 20°C chamber temperature, 20mTorr process pressure), the etching rate of Si was around 90nm/min and the SiO_2 etching rate about triple of it. When using SOI substrates, it is desired that the etch stops – or greatly reduces – when reaching the buried oxide. Due to these issues, the C_4F_8/SF_6 gas mixture used in the previous FinFET run was replaced by a SF_6/Ar etch. Silicon etching in SF_6/Ar is partially isotropic, however, and thus tall fins present a thin upper part and a wide base, as is can be seen in Figure 29d. This is not considered detrimental, since it provides increased mechanical stability for the fabricated fins. Although the forward power was increased to 80W, to improve etching directionality, mask sputtering is not an issue due to the high chemical etching factor of this recipe (POMOT et al., 1986). Using 10sccm of SF_6, 15sccm of Ar, 1200W RF power, 80W forward power and 20mTorr process pressure, the etching rate of Si was 16nm/second, or 960nm/minute. Moreover, the etching rate of SiO_2 was about a tenth, being thus suitable

for SOI substrate etching.

Table 5 summarises the chosen parameters for the Ga^+ fin definition for FinFET fabrication.

Table 5 – Final fin definition parameters

FIB Energy and Current	**Mask Width**	**Mask Depth**
30kV and 30pA	FIB lines	150nm (70nm real depth)
Ga Implant Dose	**Plasma Etch Chemistry**	**Gas Flows**
$1.44x10^{17}cm^{-2}$	SF_6 and Ar	10sccm and 15sccm
Forward Power	**RF power**	**Etch Rate**
80W	1200W	16 nm/s

3.3 Ga^+ Focused Ion Beam Lithography FinFETs

After calibration of the Ga^+ maskless lithography process, FinFET prototypes could then be fabricated with great flexibility regarding the number of fins, as well as fin height and width. For the first run of multiple fin FinFETs, the same photomask was used, with process adjustments to accommodate the new fin definition method. The fabrication flow is summarised in Figure 30.

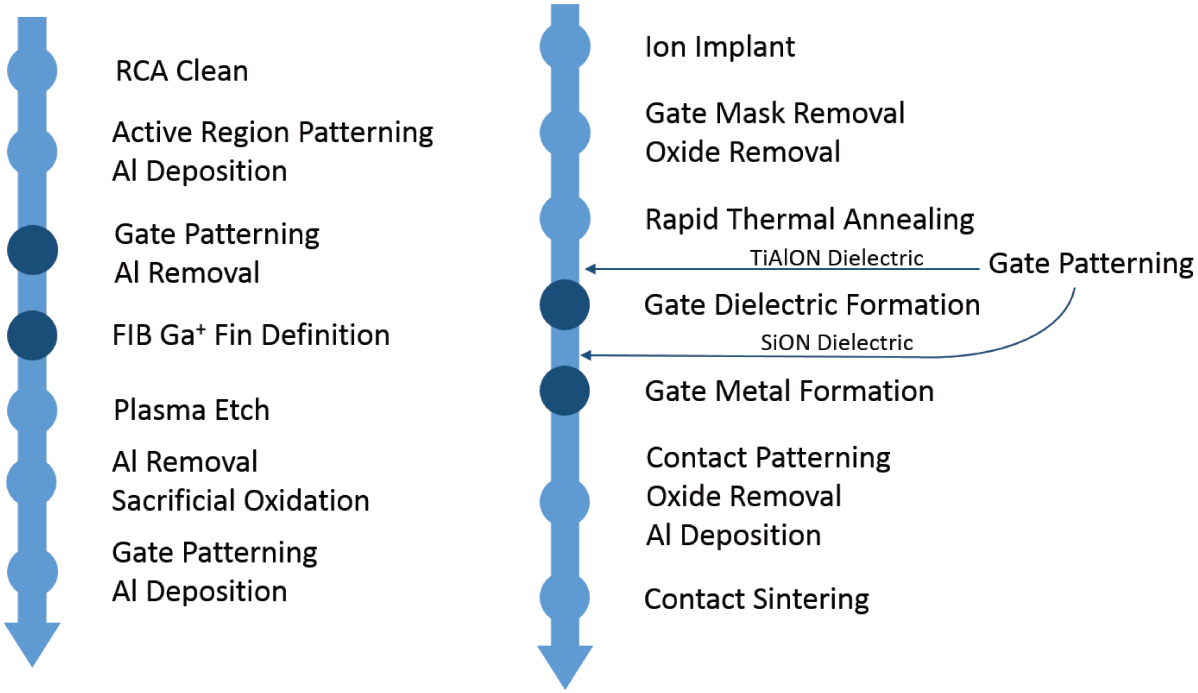
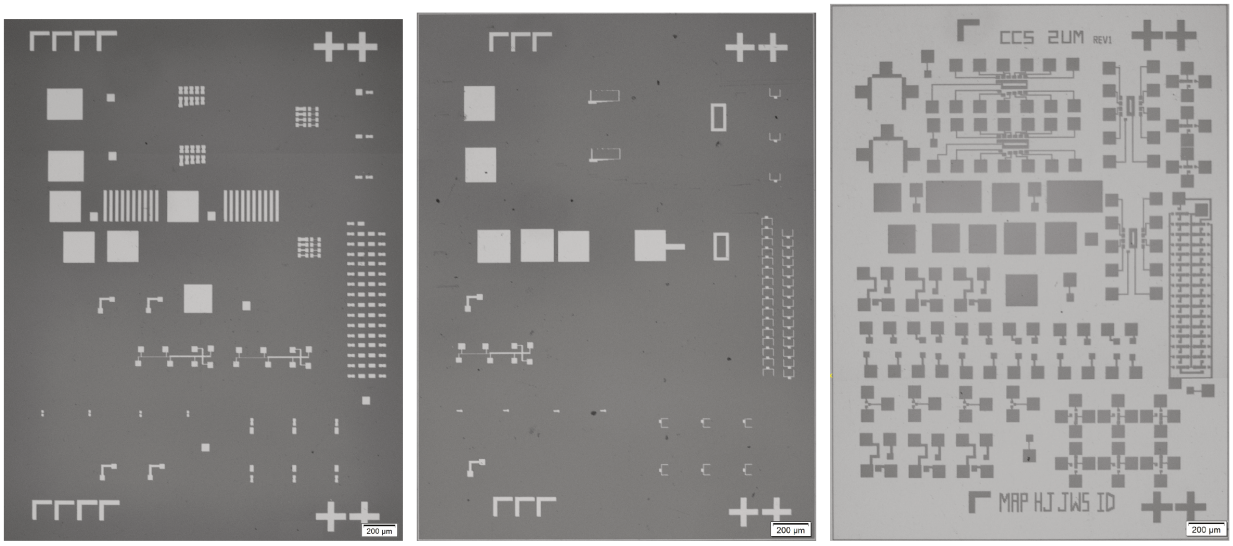


Figure 30 – Process flow for the FinFET fabricated with Ga^+ Fin Definition

This set of devices was fabricated using the same batch of photomasks as the previous one. The micrograph of the mask is repeated in Figure 31 for clarity.



(a) Mask for the active area (b) Mask for the gate (c) Mask for the contact pads

Figure 31 – Set of photomasks used for the FinFET fabrication.

To obtain the multiple fin FinFETs the source and drain regions are covered with an aluminium hard mask, while the channel is left with exposed silicon. In the channel the fins are defined by Ga^+ FIB incorporation, achieved through fast shallow cuts in the silicon. To obtain the exposed silicon channel prior to fin definition, an additional optical lithography and aluminium etch steps were introduced in the process indicated in the darker dots of Figure 30.

The SOI substrate with 340nm of silicon on top of 400nm of oxide was cleaned using the RCA standard clean described previously and the active region was patterned using the same mask used in the previous process and same lithography recipe. A 50nm thick layer of aluminium was sputter deposited to act as an etching hard mask for the source and drain region. The aluminium thickness was increased from 20nm to 50nm to sustain the plasma etching process better – reducing the source and drain silicon roughness – and because its thickness is no longer critical – in the Al hard mask milling process, the FIB processing time was dependent on the hard mask thickness, and now it is not. After lift off of the deposited metal, the gate is patterned, leaving the channel of each transistor exposed. Aluminium etch in H_3PO and HNO_3 acid at 60°C is performed for 4 seconds, in order to expose the silicon on the device channel but not under-etch onto the source and drain regions. The photorresist covering the sample is then removed and the Ga^+ FIB lithography is performed.

Nine parallel fins are defined in six transistors of each die using a 30KeV Ga^+ ion beam with 30pA current. The 7µm long shallow lines patterned present a 70nm depth, with a silicon layer below them of 270nm, which will approximately be the fin height. Concomitantly to this run of devices, further tests have been performed to asses the optimal silicon layer thickness, and improved results regarding fin aspect ratio and controllability

were obtained with thinner silicon layers, as described in the previous section. The FIB processing time for each device is around 30 seconds, a sensible improvement from the 10 minutes processing time of the aluminium hard mask FIB milling process. The lower processing time is also related to lower gallium incorporation in the FinFET, which will be discussed in the next chapter.

Inductively coupled plasma (ICP) etch is performed to obtain the FinFET active region using a 10sccm SF_6 and 15sccm Ar plasma with 1200W inductive power and 80W forward power, for 22 seconds. As mentioned previously, the semi-isotropic plasma etch is used for its low sputtering, which can damage the GaF_x etch mask. The Al hard mask is etched in the same acid mixture and the sample is oxidized for 3 minutes at 1000°C in O_2 ambient to remove plasma etch damage.

A 100nm aluminium hard mask was deposited on the gate so only the source and drain are implanted. Phosphorus implantation with 30KeV energy and $5x10^{14}$ cm^{-2} dose was performed at a 7° tilt to avoid channelling. The hard mask is subsequently removed, along with the sacrificial oxide grown in a former step, and RTA is performed for 60 seconds at 1000°C for dopant activation and silicon recrystallization.

Gate stack formation follows annealing, and for this batch of samples, different gate stacks were evaluated regarding their suitability for multiple fin FinFET devices. Two different dielectrics were used, as well as two different titanium nitride metal formation methods, and the process steps for each combination is summarized on Table 10. Arrays of 200µm diameter control capacitors are fabricated alongside the FinFETs beyond this point to easily evaluate and compare C-V characteristics of the different gate stacks. For the control capacitor array, p-type silicon with (100) wafer orientation was used. The run was thus divided in four and each had a slightly different processing to obtain a different gate stack, and the process are described in the sequence.

Table 6 – FinFET gate stacks for metal electrode and dielectric comparisons.

	Reactive Sputtering TiN	**Plasma Nitridated TiN**
SiON dielectric	ECR plasma oxynitridation, gate patterning, reactive sputtering TiN/Al deposition	ECR plasma oxynitridation, gate patterning, e-beam Ti evaporation, ECR plasma nitridation, sputtering Al deposition
TiAlON dielectric	gate patterning, e-beam Ti/Al evaporation, ECR plasma oxynitridation, reactive sputtering TiN/Al deposition	gate patterning, e-beam Ti/Al evaporation, ECR plasma oxynitridation, e-beam Ti evaporation, ECR plasma nitridation, sputtering Al deposition

Plasma oxynitridation was used for silicon oxynitride (SiON) growth as gate di-

electric on part of the samples. The remote ECR plasma provides a reactive ambient of N_2, O_2 and Ar while providing low sample surface sputtering. Gas flows of 3sccm of O_2, 7sccm of N_2 and 20sccm of Ar were used, following previous works, with ECR power of 425W and 5mTorr process pressure, for 15 minutes (MIYOSHI, 2008; SANTOS, 2013). Since the observation, in he last FinFET batch, that 20 minutes of oxynitridation provides about 20nm of SiON, the time was reduced to obtain lower EOT for the transistor dielectric. The samples with SiON as the dielectric had the gate patterned after dielectric formation. SiON is etched before contact deposition and passivates the exposed fins.

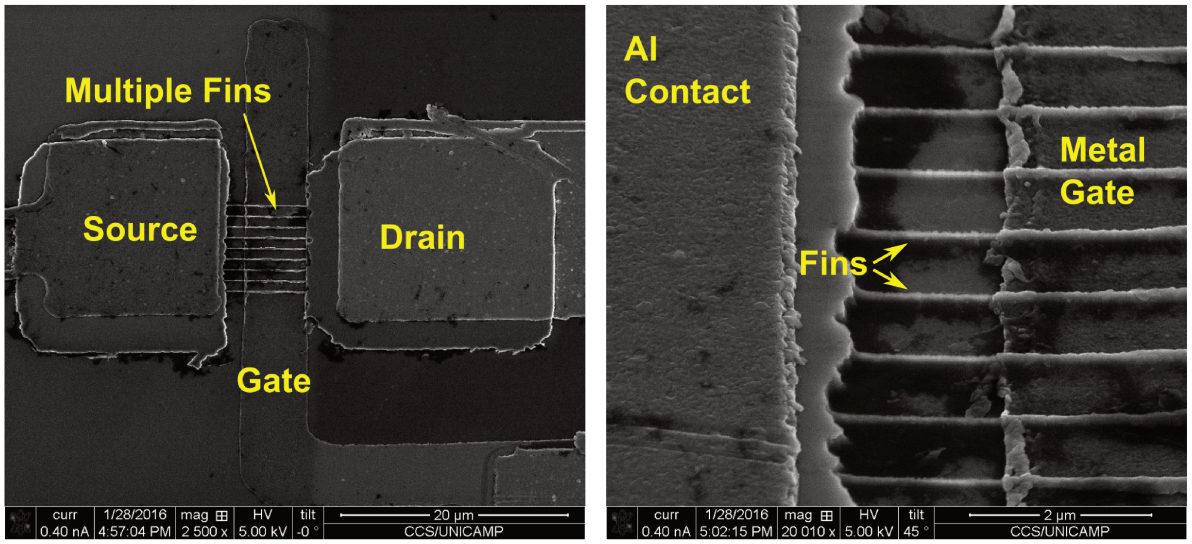
The samples with titanium-aluminium oxynitride (TiAlON) as the dielectric had the gate photomask patterned in order to expose the transistor channel for the gate stack formation and ensuing lift-off, due to the difficulty in etching TiAlON which would be required otherwise. TiAlON was formed by a two-step process, first the deposition of ultra-thin layers of titanium and aluminium and subsequent plasma oxynitridation. The ultra-thin layers were deposited by ultra high vacuum electron beam evaporation of 7Å of titanium with 32mA beam current and deposition rate of 0.7Å/s, and subsequent deposition of 3Å of aluminium with 50mA beam current and deposition rate of 0.5Å/s[2]. The evaporation was performed at the pressure of 5.1×10^{-8} Torr, which provides very accurate thickness and purity control. Remote plasma oxynitridation in O_2, N_2 and Ar converts the Ti and Al layers into TiAlON. The samples were also processed in ECR plasma, with the same parameters used for SiON growth. Instead of silicon consumption, now consumption of Ti and Al is desired. Since the plasma oxynitridation is performed *ex situ*, oxidation of the metal films can occur. To reduce oxygen exposure, the samples were transported submerged in deionized (DI) water.

Titanium nitride as the gate metal is formed on part of the samples by reactive sputter deposition and in the other part by titanium e-beam evaporation and plasma nitridation, in a manner that all four combinations of dielectric and TiN formation method are fabricated. Reactive sputtering deposition of TiN was achieved as described earlier, with a titanium target and a N_2 and Ar plasma (LIMA, 2011). A 20nm of TiN was deposited as the gate metal and an Al cap layer 100nm thick is used as the cap layer to avoid oxygen incorporation in the TiN film. The second method of TiN formation is similar to the method described above for TiAlON formation. A 10Å thick layer of titanium is evaporated to the sample by e-beam using a beam current of 32mA and deposition rate of 0.7Å at 2.2×10^{-8} Torr pressure. The samples are then nitridated *ex situ* in a N_2 and Ar remote plasma, with flows of 5sccm and 25sccm, respectively, 425W ECR power, 5W chuck RF power and 4mTorr process pressure, for 20 minutes (GARCIA, 2014). Since this process aims to obtain a metallic layer, oxidation avoidance is crucial, with the samples being minimally exposed to clean room air. After TiN formation by plasma nitridation,

[2] All metal e-beam evaporation have been performed in the LPD/IFGW laboratory, and we are very grateful to the staff there, to whom part of this work is owed.

an aluminium cap layer still remains to be deposited, which is done by sputter deposition. After gate metal and cap layers are deposited, lift off is performed and the gate stack is fully created.

Contact pads are formed by lithographic definition, 200nm aluminium deposition and lift off. The final device can be seen in Figure 32a, with the source, drain, gate and multiple fins indicated. An approximation in the fins in Figure 32b shows that the metal gate is conformally deposited on top and on the side of the fins.



(a) Multiple fin FinFET fabricated using Ga^+ FIB lithography

(b) Approximation in the fins

Figure 32 – Multiple fin FinFET prototype

3.4 Lithography Calibration

Since the photomask used in the previous processes was not entirely suitable for FinFET fabrication, especially using Ga^+ FIB lithography for fin definition, a new mask was fabricated, with minimum dimensions of 1µm and gate length of 1µm and 3µm. To achieve 1µm in a Karl Suss MJB3 UV300 Mask Aligner (KARL SUSS,) with nominal resolution of 1µm, however, careful parameter optimizations had to be performed.

The first step was to change the employed photoresist from AZ5214-E to AZ5206-E, with reduced thickness and improved resolution. When spinned at 4000rpm, the AZ5214-E has a 1.4µm layer thickness, while the AZ5206-E spinned at 5000rpm is only 0.5µm thick (CLARIANT, AZ ELECTRONIC MATERIALS,). Lower resist thickness, when using the same family of resists, translates in lower achievable dimensions, but also puts constraints in the maximum metal thickness for lift off metallization.

To obtain successful lift-off metallization, a negative angle in the developed photoresist walls is required. When using a dark field mask, this can be achieved with an

inversion tone resist, by inverting a thin top layer of resist. The second exposure, with mask, is then diffracted, and upon development, the negative angle walls are achieved, as presented schematically in Figure 33. To achieve 1µm resolution, two parameters were iterated: the first flood exposure, that controls the thickness of the inverted layer, and the second exposure, with mask, that solubilizes the desired feature. Since in an inversion tone resist the inverted layer becomes insoluble, if this layer is too thick, development issues will arise. If the second exposure is two short the pattern will not fully develop, and if it is too long patterns close by will merge.

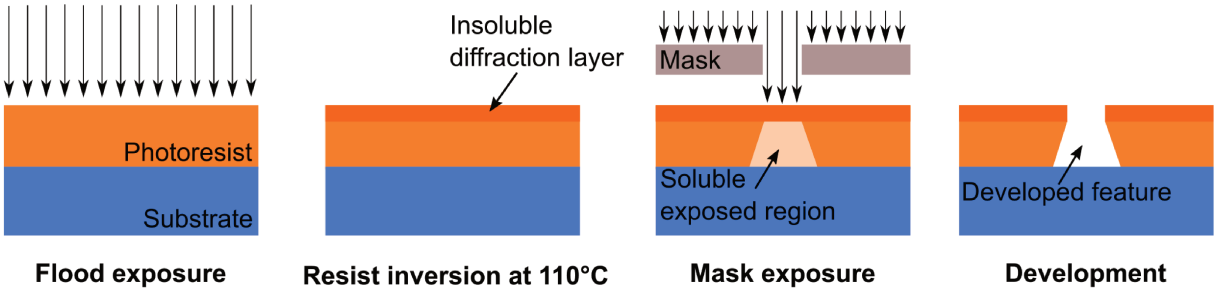


Figure 33 – Schematic of lithographic process to obtain negative angled walls using a dark field mask

In the first mask layer, used for the active region definition, the critical features are source/drain pads connected by short 1µm wide lines (Figure 34a) and 1µm wide long parallel lines (Figure 34b). To achieve such dimensions – or within 20% of deviation – the first and second exposure times were ranged from 0.5 seconds to 0.8 seconds and from 20 seconds to 15 seconds, respectively. The parameters kept stable were the first bake, to densify the resist, of 60 seconds at a 90°C hot plate; the second bake, to invert the diffraction layer, of 45 seconds at a 110°C hot plate; and the development time of 9 seconds in pure AZ 300 MIF developer (AZ ELECTRONIC MATERIALS, 2013).

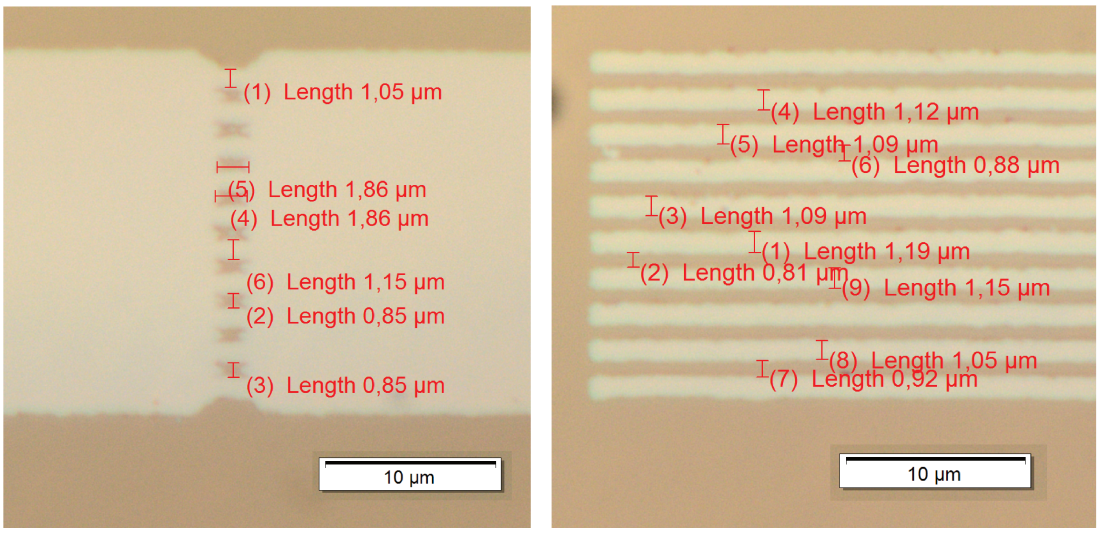


Figure 34 – Minimum obtained dimensions

Using the parameters in Table 7, with 0.8 seconds of flood exposure and 15 seconds of mask exposure, dimensions within 20% of deviation were achieved. Such features were measured after sputter deposition of a 50nm layer of aluminium and subsequent lift-off, in order to adequately duplicate the FinFET fabrication process for the active region. It is believed that further optimizations, to obtain dimensions closer to 1µm, may be possible if other process parameters are tighter controlled, such as storage temperature and humidity. Nonetheless, line widths around 1.11µm, as presented in Figure 34, are already a satisfactory result for this work. This is true specially because structure of interest for this work has a gap between the source and drain pads, where the fins are defined using Ga^+ FIB lithography.

Table 7 – Parameters for the active region mask lithography

Process	**Parameters**
HMDS application for increased adhesion	5000rpm, 30 seconds, 1 minute rest
AZ5206 resist application	5000rpm, 30 seconds
Resist soft bake for solvent evaporation and resist densification	90°C hot plate, 1 minute
Exposure to obtain the diffraction layer	0.8 seconds, without mask
Resist inversion	110°C hot plate, 45 seconds
Exposure for pattern transfer	15 seconds, with FinFET1 mask
Development	MIF 300, 9 seconds, rinse in DI water

Proximity effects in optical lithography are the reason dense and isolated patterns have to be exposed differently to achieve similar results. Alternatively, corrections are made during pattern design, employing adjustments to compensate for the proximity effect (LEVINSON, 2010). The active region mask layers presents dense arrays of parallel lines, while the gate definition mask is composed of sparse features, where the minimum dimension is an isolated 1µm wide line, the transistor gate. As such, the same exposure parameters presented in Table 7 resulted in undefined gate structures.

The second exposure was thus varied from 23 seconds to 25 seconds, in order to find the correct time that achieves the target dimension of 1µm and defines all structures. The measured dimensions are presented in Figure 35. The arrows indicates that although the exposure time of 23 seconds achieves dimensions close to the target dimension of 1µm, it presents structures with undefined gate, thus the 0µm gate length. In the context of this work it is acceptable to have gate lengths of 2µm instead of 1µm, but a lack of defined gate results in no ion implant masking and thus a FinFET channel with complete n-type doping. Furthermore, it is interesting to observe in Figure 35 the wide spread of the measure gate length. In the 23 seconds and 25 seconds exposure time, the difference the thinnest defined feature and the thickest is around 0.8µm, while in the other case,

the spread reaches 1.2µm. This means that even if the target dimension is achieved in one region, other regions may present gate lengths that differ significantly, possibly due to resist thickness non-uniformities along the sample surface.

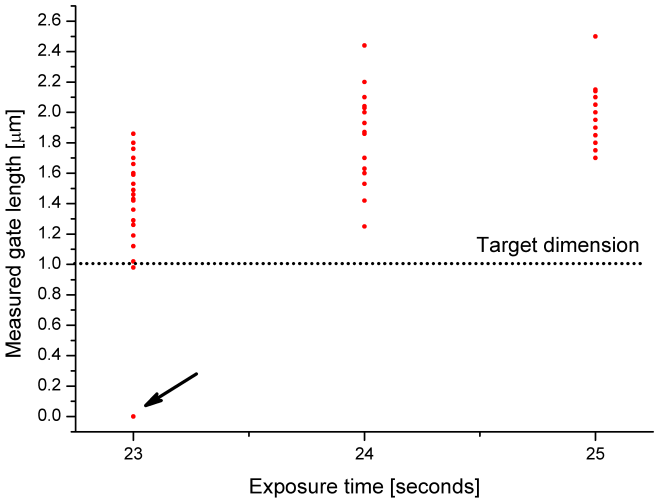


Figure 35 – Minimum obtained dimensions for the gate as a function of exposure time.

Table 8 presents the selected parameters for the gate definition, using 23.5 seconds mask exposure time to avoid feature non-definition. The development time has been increased to 10 seconds in order to achieve more uniform results between the samples.

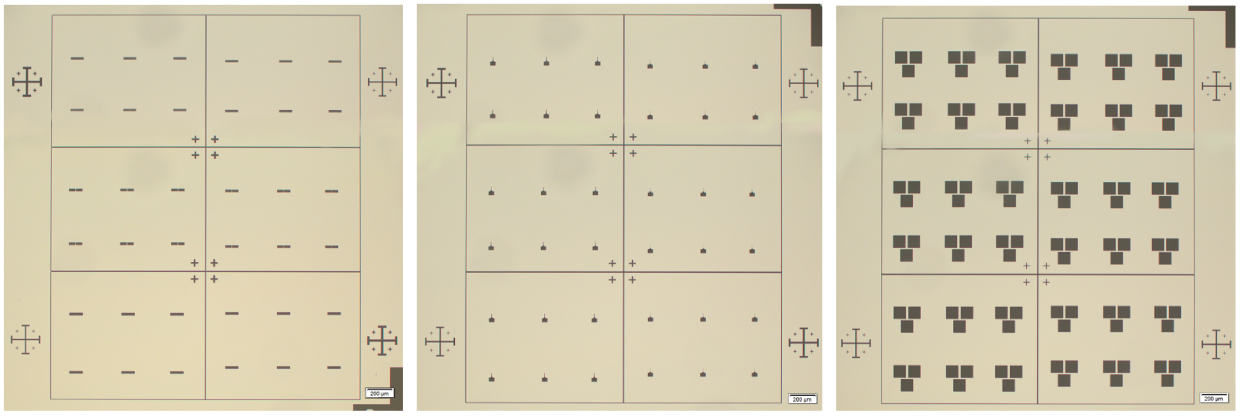
Table 8 – Parameters for the gate mask lithography

Process	**Parameters**
HMDS application for increased adhesion	5000rpm, 30 seconds, 1 minute rest
AZ5206 resist application	5000rpm, 30 seconds
Resist soft bake for solvent evaporation and resist densification	90°C hot plate, 1 minute
Exposure to obtain the diffraction layer	0.8 seconds, without mask
Resist inversion	110°C hot plate, 45 seconds
Exposure for pattern transfer	23.5 seconds, with FinFET2 mask
Development	MIF 300, 10 seconds, rinse in DI water

3.5 Optimized Ga^+ Focused Ion Beam Lithography FinFETs

This set of FinFET devices was fabricated using the Ga^+ FIB lithography described in Subsections 2.1.4 and 3.2.2, and the photomasks fabricated for the FinFET

process and shown on Figure 36[3]. The lithography recipes have been optimized and described in Section 3.4.



(a) Active area mask definition (b) Gate mask definition (c) Contact pads mask definition

Figure 36 – Set of photomasks used for the FinFET fabrication.

A summary of the process steps is given on Figure 37. Since the active region mask was fabricated already with a gap in the transistor channel, the lithography and aluminium removal step could be excluded from the process flow. Furthermore, in this sample the different gate stack material evaluation is also performed. To improve fin passivation, an isolation oxide is deposited by CVD after gate metal formation. Also, to reduce the prototypes series resistance, a thin layer of titanium is deposited in the contacts, prior to aluminium deposition.

The starting substrate was a SOI wafer, with 340nm of silicon and 400nm of buried oxide. After complete RCA clean, the sample was cleaved in two and the silicon top layer was thinned to 87nm and 125nm by wet oxidation at 1000°C and subsequent oxide strip using HF. The active region was patterned using the lithography recipe described in Section 3.4, in Table 7 and the active region FinFET mask, presented in Figure 36a. A 50nm thick layer of Al is then deposited by DC sputtering.

The fins are defined using Ga^+ FIB lithography and it can be seen in Figure 38 how the silicon layer thickness beneath the cut is closely related to the fin height after silicon etch.

Sacrificial oxidation for plasma etch damage reduction is performed in the conventional furnace at 1000°C in O_2 ambient, for 3 minutes. The gate is patterned with the recipe presented in Table 8 and 150nm of Al is deposited by DC sputtering. The hard mask is thinned so lift off metallization can still be performed, but guaranteeing that ion implant at 30KeV is still masked by TRIM simulations. Phosphorus ion implant is then

[3] The design of the photomask set was performed in the context of this work and has been fabricated at the Renato Archer Center for Information Technology (CTI Renato Archer), for which we are very grateful.

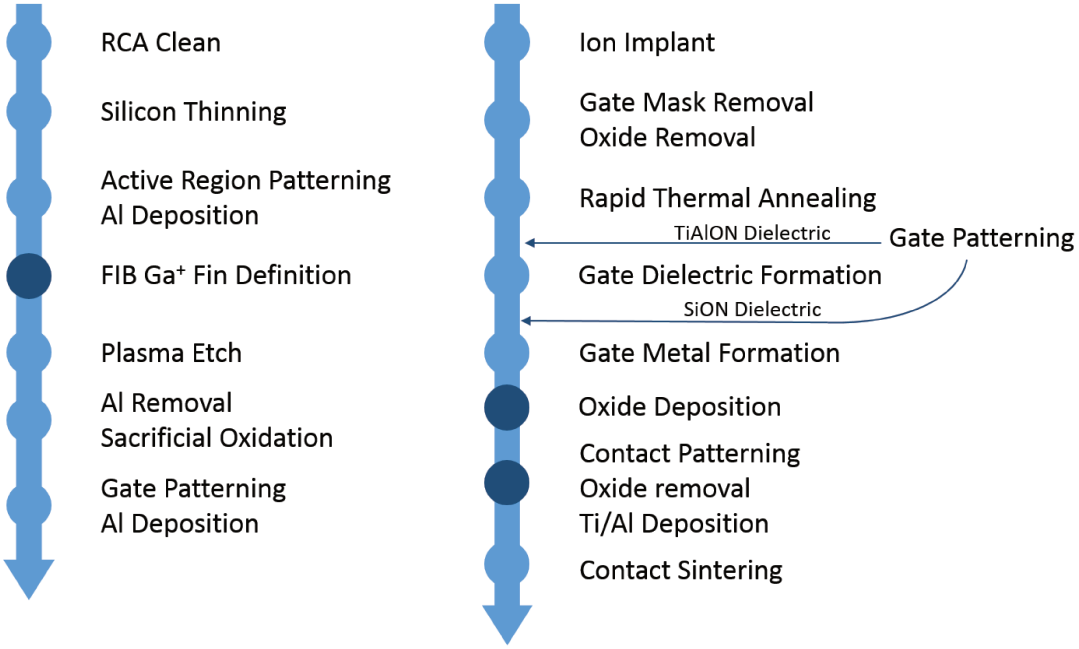
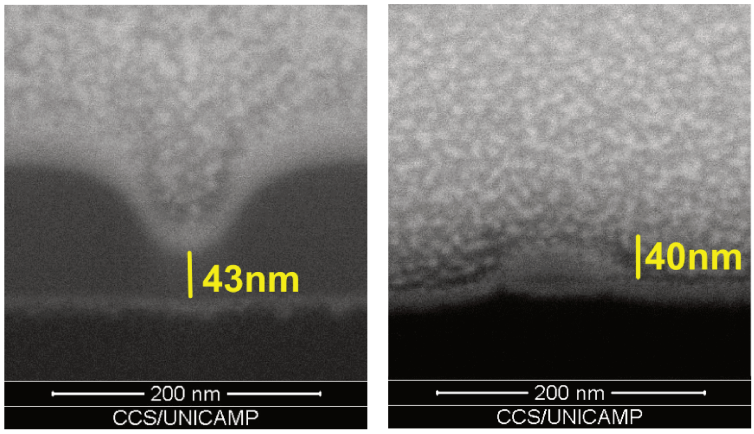


Figure 37 – Process flow for the FinFET fabricated with Ga^+ Fin Definition and the FinFET Mask



(a) FIB shallow cut cross section for fin definition

(b) Resulting fin cross section after silicon etch

Figure 38 – Sample before and after silicon etch, showing the close relation between the silicon layer thickness beneath the FIB cut and resulting fin height

performed at 30Kev, with $5x10^{14}$ cm^{-2} dose and 7° tilt. Aluminium hard mask is removed by wet etch and sacrificial oxide is stripped in HF.

The samples are cleaned and RTA is performed at 1000°C for 60 seconds for silicon recrystallization and P^+ activation as n-type dopants. Further 9 minutes in the conventional furnace at 1000°C in inert ambient is performed to enhance dopant diffusion under the gate and avoid misalignment issues. This is necessary since the prototyping process is not self aligned. SILVACO simulations were used to determine the diffusion time and the simulated device showing its doping profile is presented in Figure 39, showing a cross section along one fin. For nine minutes thermal processing the junction underlap is

0.25µm, which gives a metallurgical channel length (L_{met}) of 0.5µm for the devices with nominal gate length of 1µm. In the simulated profile it is also possible to note a difference in the silicon layer thickness in the source/drain and in the channel, which occurs due to the shallow FIB cuts needed for fin definition.

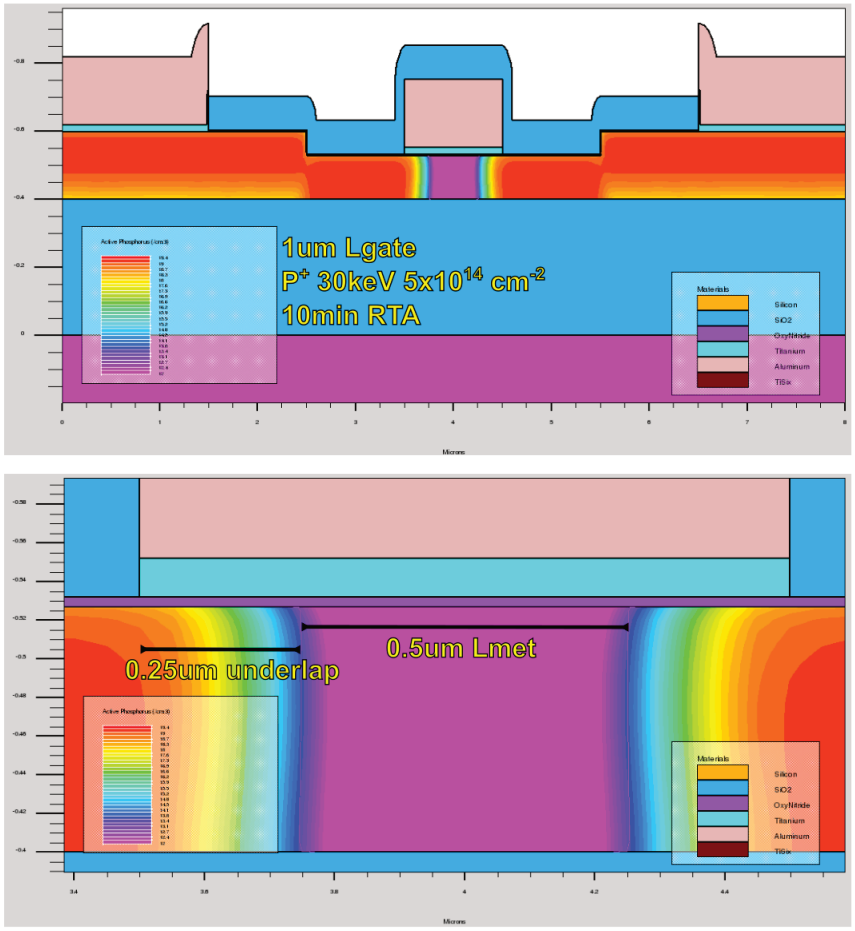


Figure 39 – SILVACO simulation of the complete device, presenting the doping profile after 10 minutes thermal treatments.

After the thermal treatment the samples are cleaned once again and the gate dielectric is formed, following the same process steps described for the previous sample. If the dielectric is TiAlON, the gate is patterned prior to Ti and Al deposition. Otherwise, SiON is grown and then the gate is patterned to receive the metal electrode.

SiON is grown using the same process parameters used before, 3sccm of O_2, 7sccm of N_2 and 20sccm of Ar gas flows, ECR power of 425W and 5mTorr process pressure, for 15 minutes.

TiAlON is formed by Ti and Al deposited by e-beam evaporation and plasma oxynitridation. A thin layer of 7Å of Ti was evaporated using 30mA beam current, which results in a deposition rate of 0.8Å/s. Aluminium with 3Å thickness is then evaporated using a 68mA beam current and deposition rate of 0.7Å/s. The evaporation is performed at ultra high vacuum of $1.5x10^{-8}$ Torr, presenting thus high purity and excellent thickness

control.

TiN either deposited by DC reactive sputtering or by titanium e-beam evaporation and plasma nitridation. An aluminium cap layer deposited on top of the gate electrode by DC sputtering. After TiN/Al lift off, SiO_2 is deposited by ECR-CVD using 10sccm O_2, 20sccm Ar and 200 sccm SiH_4 for 10 minutes at 5mTorr process pressure and 500W ECR power. The deposited thickness is expected to be approximately 200nm. The contacts are then patterned using the mask presented in Figure 36c and a 30 minutes hard bake at a 110°C hot plate is performed to increase resist adhesion and density. The isolating oxide beneath the patterned contacts is stripped in buffer HF for 15 seconds. A thin layer of titanium is deposited by DC sputtering and 150nm of aluminium covers it, to form the contact pads. The final fabricated devices are presented in Figure 40.

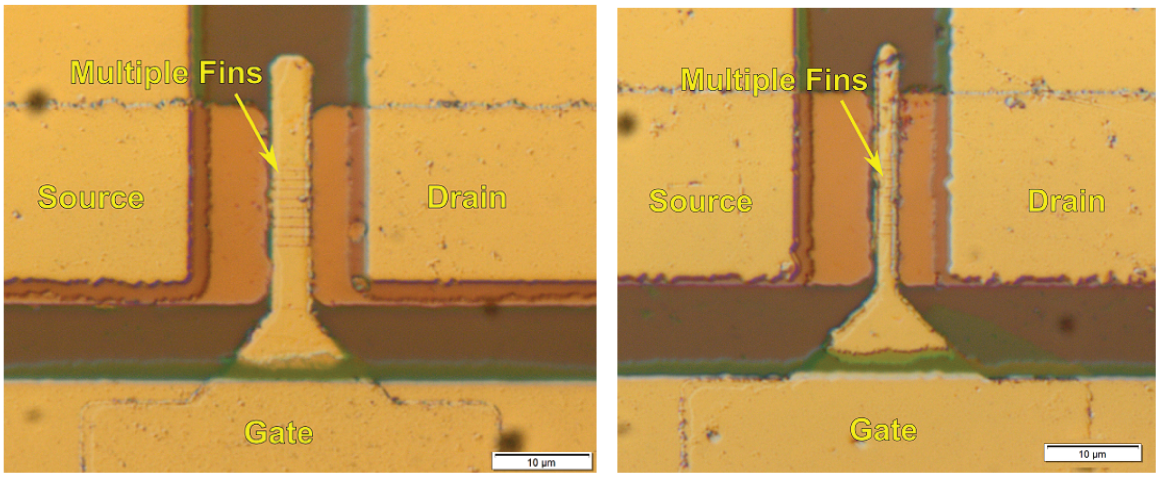


Figure 40 – Fabricated devices

4 Characterizations and Discussions

In this chapter morphological and electrical characterization of the different methods used for FinFET fabrication will be presented and discussed. The different fin definition processes will be evaluated regarding their morphological characteristics: process-induced gallium incorporation and achieved dimensions. The gate stack alternatives are in turn assessed regarding their capacitance-voltage behaviour, and parameters such as flat band voltage (V_{FB}), work function (WF), equivalent oxide thickness (EOT) and oxide leakage are compared. After different annealing times, the gate stacks are also evaluated regarding their parameter stability. The electrical characterisations of fabricated FinFET prototypes are then presented, with the discussion being focused on the extracted parameters such as threshold voltage (V_{th}), low field mobility (μ_0) and source and drain series resistance (R_{SD}). Critical analysis of the results are important to understand and evaluate the fabricated devices, whether they work as expected or do not.

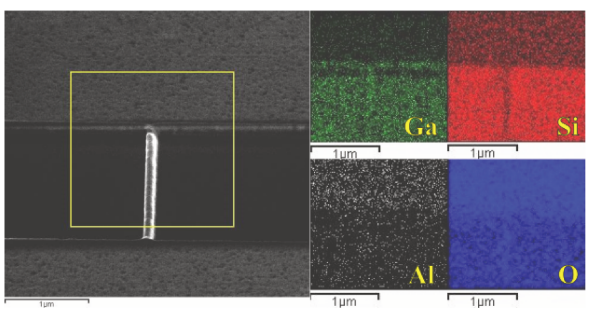
4.1 FinFET Morphological Characterisations

This section will discuss two morphological characteristics of the fabricated FinFETs: the process-induced gallium incorporation in the fins and the fin dimensions. Using the evaluated morphological characteristics, comparisons between the different processes used for FinFET fabrication are made such as to better evaluate them.

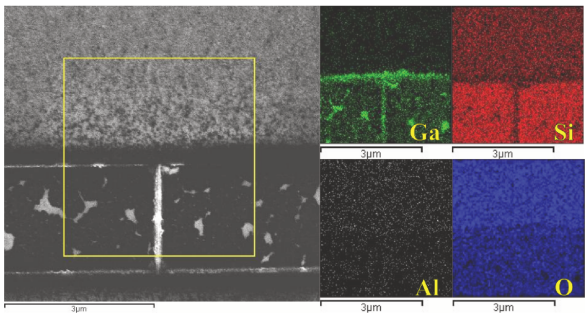
4.1.1 Ga^+ incorporation in the fin

Since the Dual Beam FIB/SEM employed (FEI Nova 200 NanoLab, product data in (FEI Company, 2003)) uses a gallium ion source, it is expected a high degree of Ga incorporation in the processed transistors. Gallium incorporation in the fins was evaluated using the energy dispersive X-ray spectroscopy (EDS) system X-Max from Oxford Instruments (Oxford Instruments, 2008) with 20mm^2 detector area. The EDS mapping of fins fabricated by fin milling, Al hard mask milling and Ga^+ lithography can be observed in Figure 41a, Figure 41b and Figure 41c, respectively. All samples have been analyzed after FIB processing and plasma etching. It can be noted, in the first two cases, that galliumis positively detected in the milled region and fin area. In the latter case, however, no trace of gallium is detected by the EDS analysis. When superimposing the EDS spectra of the different fin definition processes, in Figure 41d, the absence of the Ga peak in the Ga^+ FIB lithography reinforces that no trace of gallium could be detected. In an EDS analysis, the material detectability limit is usually 1000ppm in weight (GOLDSTEIN et al., 2003; HAFNER, 2005), which is equivalent to a gallium concentration of 2x10^{19}cm^{-3}

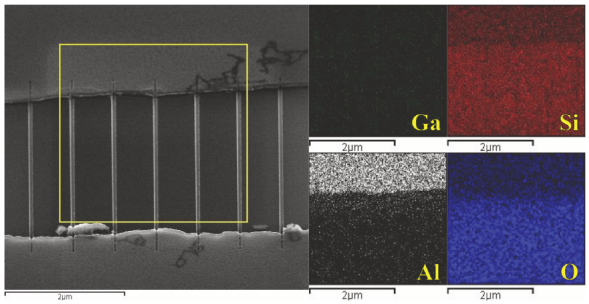
in silicon. No trace of gallium in the samples processed using Ga^+FIB lithography does not mean that gallium incorporation is totally absent in this samples. We can affirm, however, that that the incorporated gallium concentration in the Al hard mask milling and fin milling processes is much higher – possibly one order of magnitude or more – than in the Ga^+ lithography process. A more sensitive characterisation method such as secondary ion mass spectrometry (SIMS) (BENNINGHOVEN et al., 1987; FLETCHER; VICKERMAN, 2013) could be used to determine the gallium concentration on the fins fabricated by the different FIB methods. Material analysis using SIMS would also present the Ga distribution in the silicon layer, in terms of depth, rendering important understanding of the Ga distribution in the fins.



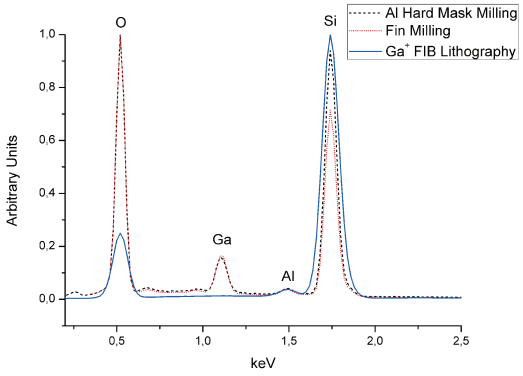
(a) Fin milling



(b) Al hard mask milling



(c) Ga^+ FIB lithography



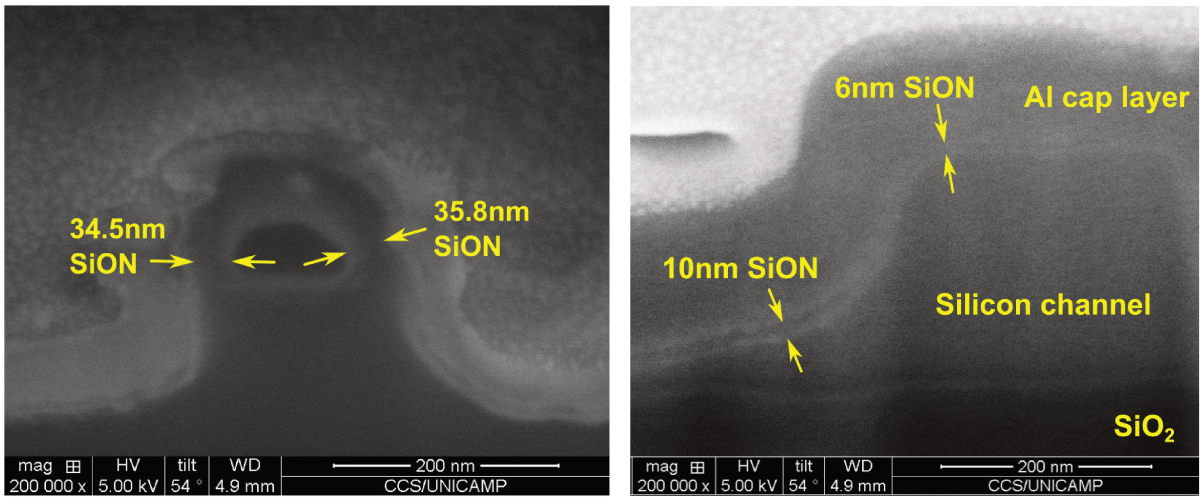
(d) Spectra of the different processes, showing the absence of the Ga peak in the Ga^+ FIB lithography process.

Figure 41 – EDS comparisons of Ga^+ incorporation in the transistor fin after FIB processing and plasma etching, for the different fin definition processes.

This reduction in process induced gallium incorporation is closely related to the reduction in FIB processing time when comparing the first two milling processes with the Ga^+ lithography. As presented in Chapter 3, the FIB processing time for fin definition, using the Al hard mask FIB milling process is around 10 minutes, while using Ga^+ FIB lithography the fins are defined in only 30 seconds, both processes using the same beam current. Gallium is a p-type dopant in silicon, and thus the impact of reducing its concentration, when fabricating MOSFET devices can be great. While works have even used the

Ga^+ ion-beam for ion implantation of p-type junctions (WANZENBOECK; BERTAGNOLLI, 2003; SANTOS et al., 2013), in the case of FinFETs the channel doping level should not be affected by the fin definition method. Moreover, in modern FinFET devices the body doping should be kept to a minimum, to avoid non-uniformities which contribute to V_{th} shifts (SHIN et al., 2009). Again, while the exact Ga concentration in the fins after FIB processing is unknown and should be further explored using more sensible techniques, the EDS analysis indicates that the Ga doping has decreased significantly.

At this point it should be noted that a significant physical thickness difference has been observed in SiON grown in fins fabricated using FIB milling and Ga^+ FIB lithography processes. The two samples presented in Figure 42 have been processed together for 15 minutes in $N_2/O_2/Ar$ plasma in room temperature for the SiON growth – similar conditions to the gate stacks evaluated in this section. While the FIB milled sample presents approximately 35nm of SiON (Figure 42a), the SiON layer on the other is less than 10nm thick[1]. When studying SiO_2 thermal oxidation, Deal and Sklar (1965) evaluated that the different gallium concentration in silicon does not affect the SiO_2 growth rate. Gallium has a segregation coefficient of ~20 in the Si-SiO_2 interface, it does not segregate to the SiO_2 dielectric layer, however, it quicky diffuses to the ambient and does not affect the growth rate (GROVE et al., 1964). However, the cited works all study thermal oxidation of silicon, and it could be argued that plasma oxynitridation of silicon is in fact affected by the gallium concentration, since the only difference between the two samples is the fin definition method, which have significant gallium incorporation differences, as discussed.



(a) (b)

Figure 42 – Difference in SiON layer thickness grown in a FIB milled fin (a) and in a fin defined using Ga^+ FIB lithography.

[1] Although the image is not as clear as desired, due to the equipment resolution limit and charging issues, it is still possible to see the faint edge of the dielectric layer.

4.1.2 Fin Dimensions

Fins obtained by silicon FIB milling have their dimensions controlled mostly by the beam shape. The focused ion beam, although presenting a sub-10nm diameter, still has a Gaussian distribution, and thus the Ga^+ ions spread to a certain degree. As such, to obtain straight and vertical sidewalls is challenging using this technique, besides the difficulties in achieving fins with sub-100nm width (FREY et al., 2003). Figure 43 presents a fin fabricated by FIB milling. It can be seen that the achieved fin is more wide than tall. One interesting effect of fabricating FinFETs using this technique is that while milling, not only the silicon layer is removed, but also part of the buried oxide, which results in the silicon fin standing on top of an oxide pillar. When the gate dielectric and electrode are deposited, they extend beneath the fin, as seen in Figure 43. This transistor configuration is known as Π-gate, and provides current drive enhancements and improved subthreshold characteristics, when compared to traditional triple gate FinFETs (PARK et al., 2001).

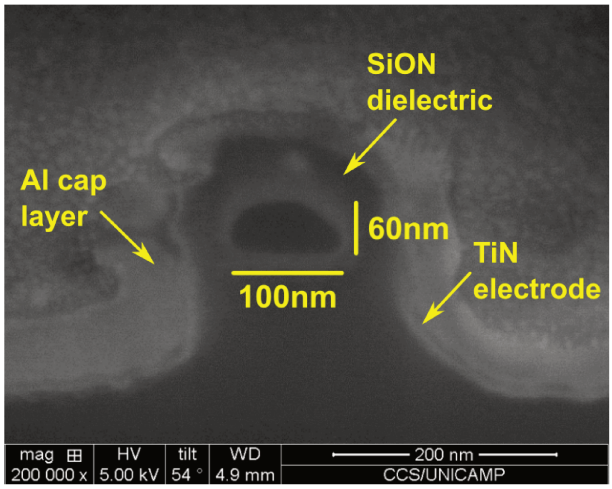


Figure 43 – Fin obtained using FIB silicon milling method

Using the Al hard mask FIB milling method, the final fin dimension is limited by the thin aluminium strip left in the center of the hard mask. This thin strip is in turn controlled by the gap left between the two shallow milled regions. Not only that, but since the milled regions are masked in the C_4F_8/SF_6 etching by the GaF_x mask formed by the Ga^+ incorporation, the fin sidewall is not vertical, but tapered. The fin base is thus considerably larger than its top. Figure 44 present a cross section of a fin defined by Al hard mask FIB milling, where the fin top width is 60nm, the fin height 77nm and the fin base width 175nm.

The fins obtained by Ga^+ FIB lithography, on the other hand, have their dimensions mostly controlled by the Ga incorporation distribution during the shallow cut, as well as silicon layer thickness and etching method. Figure 45 shows three different fins obtained using the same method, but with different initial silicon layer thickness in the SOI substrate. It is possible to see that when using a thinner silicon layer, the fabricated

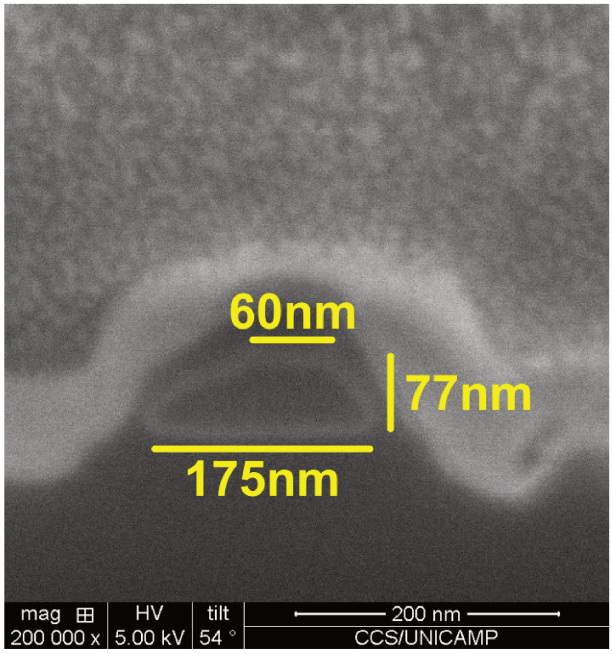
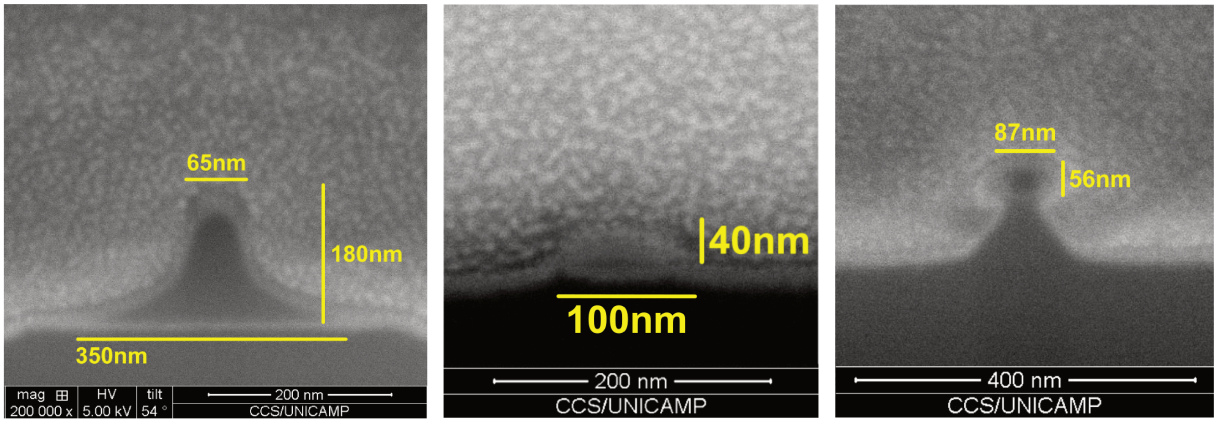


Figure 44 – Fin obtained using Al hard mask FIB milling method

fins present reduced bottom width, when compared to the taller fin in Figure 45a. This is due to plasma etching in SF_6/Ar, that, while used for its reduced mask sputtering, also results in semi-isotropic etching. The taller fin in Figure 45a remains with sub-100nm width from the top until about two-thirds of its height, when it forms the wider base. On one hand, this base provides the fins with increased mechanical strength, reducing the chance damages such as fin removal during cleaning processes. On the other hand, fins with smaller dimensions provide increased electrostatic control of the gate over the channel – gate-to-channel-coupling – which in turn helps suppressing transistor short channel effects (DAL et al., 2007; COLINGE et al., 2008). It is important to point that FinFETs do not require to have fins with perfectly rectangular cross sections. For example, the devices presented by Intel present angled sidewalls, with a triangular cross section (AUTH, 2012; NATARAJAN et al., 2014). In fact, a triangular fin shape results in significant leakage current suppression, when compared to rectangular fins (GAYNOR; HASSOUN, 2014).

It is assessed, thus, that Ga^+ FIB lithography is a viable alternative for FinFET prototype fin definition. Comparing the different methods using the focused ion beam, it provides the lesser degree of process induced Ga incorporation and the highest degree of fin dimension control. Fins with sub-100nm width were obtained, when using a thin silicon layer (Figure 45c). Tall fins can also be fabricated, as presented in Figure 45a, and a wide base provides mechanical strength to support process related damages. Moreover, the processing time is greatly reduced when comparing milling techniques to Ga^+ lithography, enabling the fabrication of more prototypes in the same time.



(a) Tall fin with wider base (b) Near-flat fin (c) Near-circular fin

Figure 45 – Different fins obtained using Ga^+ FIB lithography definition method.

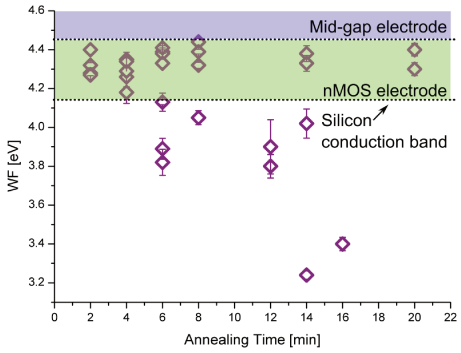
4.2 Gate Stack Alternatives Comparisons

The different gate stack alternatives were evaluated using arrays of control capacitors, which were processed alongside the FinFETs and subjected to annealing iterations at 450°C using a 92% N_2, 8% H_2 ambient. The capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured after each annealing iteration and parameters such as flat band voltage (V_{FB}), equivalent oxide thickness (EOT) and work function (WF) were extracted from these measurements by CVC simulations and analysis, with fitting errors below 10% (HAUSER; AHMED, 1998). All C-V measurements have been performed at 1MHz and series resistance compensation have been applied to the curves.

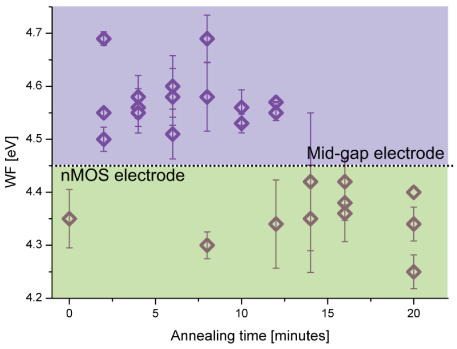
The electrical behaviour of a device should change as little as possible throughout its operation and similar devices should present similar electrical characteristics. Parameters shifts cause IC reliability issues, and for this reason the parameter stability – how little the parameter values shift – of work function (WF) and flat band voltage (V_{FB}) (CHUNG et al., 1991; AGARWAL et al., 2015). Figure 46 presents the extracted work function of the different gate stacks in each step of the annealing iteration, showing how much the work function varies with thermal processing. The work function values are categorized in either pMOS, nMOS or mid-gap electrodes, according to Chau et al. (2005) and the silicon valence and conduction band energies. The metal gate work function influences the transistor threshold voltage and variations in threshold voltage translate in reduction of reliability in very large system integration (VLSI) (CHUNG et al., 1991; AGARWAL et al., 2015). It can be noted, from Figure 46b that the SiON/TiN formed by plasma surface treatment stack presents work function values only in the mid-gap and nMOS electrode ranges, while the other studied stacks present higher variations for this parameter with annealing time.

The effective work function of a metal deviates from the value measured in vacuum due to charged states in the dielectric-metal interface (YEO, 2004). Dipoles and charged

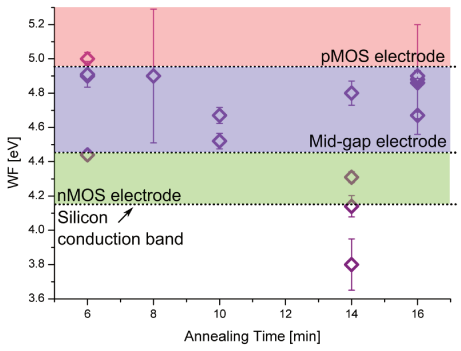
traps are dependent on the dielectric and metal selection, but also on processing parameters which induce additional states on the interface (LIMA, 2015). Annealing in 92%N_2 and 8%H_2 ambient passivates unsaturated bonds, reducing ellectrically active interface states, and improving the dielectric-metal and silicon-dielectric interfaces (CARTER et al., 2003; SCHMIDT et al., 2005). Thermal processes also lead to interlayer diffusion, which also have the effect of shifting the effective electrode work function – a process used for work function tunning of metal gate electrodes (LU et al., 2005; LIMA et al., 2014). Low values of electrode work function (e.g. 2.6eV) can be observed in Figure 46d, for the TiAlON/TiN by plasma surface treatment gate stack. It is believed that this is due to Al diffusion from the dielectric to the interface with the metal gate, which reduces the effective work function of the TiN electrode. The Al segregation to the surface can also create a low-κ interface layer, which, in series with the bulk dielectric, drastically reduces the total capacitance (KIM et al., 2008). Discussion will return to this low-κ interface layer when the EOT of the TiAlON dielectric is discussed. The other gate stacks (Figure 46a and Figure 46c) also present a certain degree of WF instability. In the case of SiON/TiN by reactive sputtering gate stack, WF variation are likely related to dipole variations in the dielectric-electrode interface (ADACHI, 2008; LIMA, 2011).



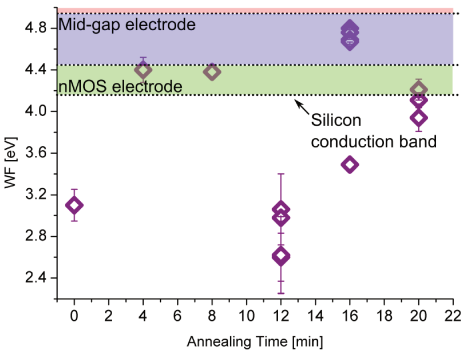
(a) SiON/TiN by reactive sputtering



(b) SiON/TiN by plasma surface treatment



(c) TiAlON/TiN by reactive sputtering



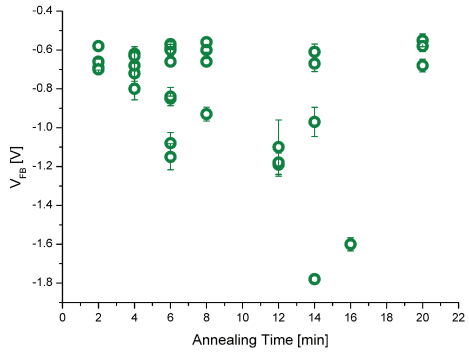
(d) TiAlON/TiN by plasma surface treatment

Figure 46 – Work function variation with 450°C annealing time for the different gate stack structures. The values are indicated whether they are more suitable for pMOS, nMOS or mid-gap electrodes.

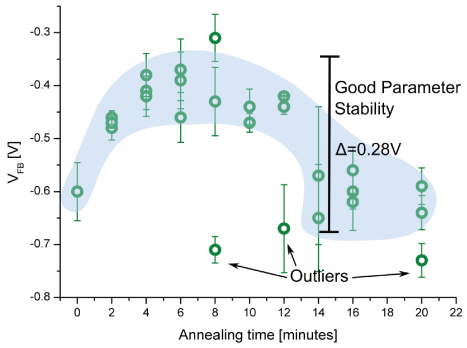
From Figure 47 we can see that the SiON/TiN by plasma surface treatment structure presents reasonably good parameter stability, with 0.28V variation in V_{FB} with up to 20 minutes annealing. The parameter stability with different annealing times, for the SiON/TiN by plasma surface treatment gate stack can be also observed from the overlay of capacitance voltage curves, presented in Figure 48. It can be noted that the curves are almost superimposed, with slight shifts. Again, it is expected that similar devices present similar electrical characteristics, and the superimposition of the C-V measurements indicate that this is the case for the SiON/TiN by plasma surface treatment gate stack. A 0.28V V_{FB} variation in sensitive applications or VLSI is unacceptable, however. In this work this variation range is considered adequate when compared to the other studied options. Contrasting with this parameter stability is the TiAlON/TiN by reactive sputtering gate stack, that presents up to 10V V_{FB} shift when subjected to 20 minutes of annealing. Even when annealed only to 16 minutes, seen in the graph inset, V_{FB} values range from -0.1V to -1.15V. V_{FB} shifts in metal oxides, according to Nabatame et al. (2007), are caused by interface dipoles between the dielectric and SiO_2 interfacial layers. The oxygen from the dielectric diffuses to the interface, causing re-oxidation at the interfacial-SiO_2/Si interface, and generating additional dipoles. Oxygen positively charged vacancies also play a part in V_{FB} roll off (BERSUKER et al., 2010). In our case a similar effect may be happening, associated to Al diffusion to the gate-dielectric interface, which increases even further the dipole density and consequently causes V_{FB} shifts.

From Figure 49 we can obtain two important conclusions. The first is that TiAlON has higher EOT than expected, and the second is that the leakage current is in general very high. Since EOT is extracted from the difference between the maximum and minimum capacitance, measuring a high capacitance results in a low EOT. But the confidence in the capacitance measurement is reduced when capacitors present both high leakage and high series resistance (YANG; HU, 1999; LUO; MA, 2004). In the case where the leakage is negligible, a series measurement model is used, which accounts for the capacitor series resistance and provides reliable measurements. In the cases where the leakage current is high, but series resistance is low (i.e. below 50Ω), the latter can be neglected and a parallel measurement model provides accurate capacitance values. When both effects are significant, such as in Figure 49a, where the capacitors present around 500Ω series resistance and leakage current density around 6.3A/cm^2 at -1V, more complex models are required for the accurate capacitance measurement and EOT extraction (LUO; MA, 2004). In this work, however, all capacitors have been measured using the series and the parallel models and only the series resistance is subtracted from the measurements, which lead us to doubt EOT values extracted from capacitors with high leakage current densities (above 0.5A/cm^2).

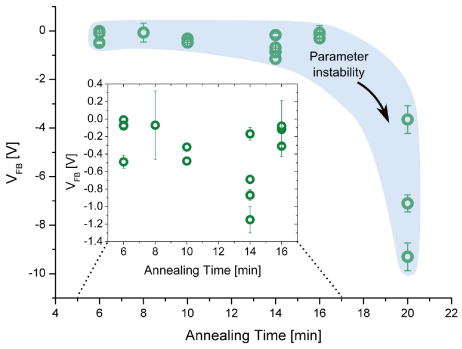
As such, although in Figure 49a EOT values as low as 0.2nm are reported, a higher measurement confidence is obtained where the leakage current is lower, and the measured



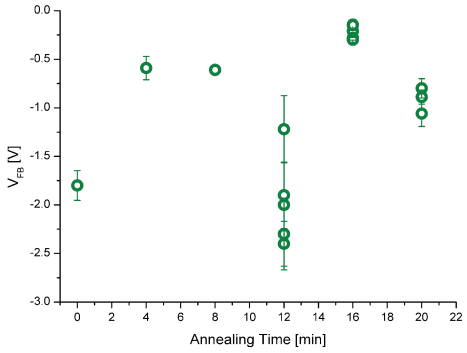
(a) SiON/TiN by reactive sputtering



(b) SiON/TiN by plasma surface treatment



(c) TiAlON/TiN by reactive sputtering



(d) TiAlON/TiN by plasma surface treatment

Figure 47 – Flat band voltage variation with 450°C annealing time extracted from capacitance-voltage measurements for the different gate stack structures. Cases b and c present remarkable parameter stability or instability.

EOT is 11.9nm for the TiAlON/TiN by reactive sputtering stack, as the arrows indicate in the graph. With a gate electrode formed using a different method, in Figure 49b, the EOT is evaluated as the average value of the measurements indicated by the arrow in the graph: 15.2nm. Since the dielectric is the same, the EOT should be similar also. However, as will be discussed later, it is suspected that the gate electrode incorporates part of the oxygen from the TiAlON layer, increasing the dielectric effective thickness which would be then dependent on the electrode formation method.

For the gate stacks with SiON dielectric, a seemingly opposite behaviour is observed: the lower leakage current measurement (e.g. 10 minutes annealing time in the Figure 49d) is associated with a low EOT as well. In Figure 49d, the average EOT measurements at the 10 and 12 minutes annealing marks is 3.6nm. When observing Figure 49c, a certain trend for the EOT values can be noticed: while most of the values are spread up to 20nm, a group of points is closely positioned in the bottom part, highlighted in the graph. Unfortunately there are no leakage current measurements associated with said EOT points. The average value of the highlighted measurements, however, is also 3.6nm. The good agreement between the two stacks and the low leakage associated with the

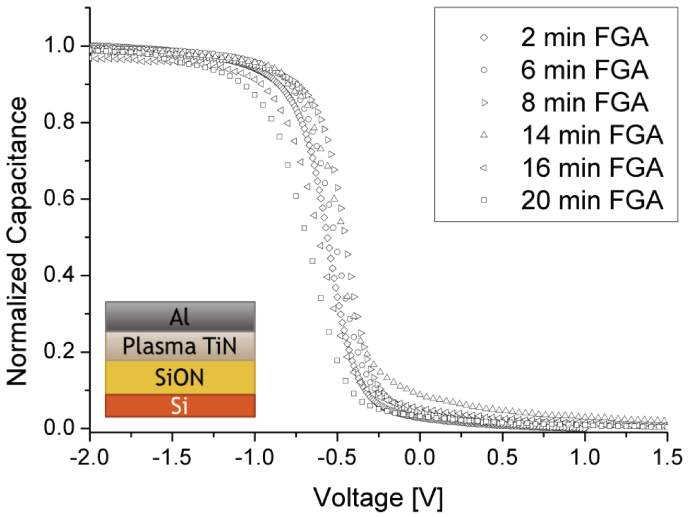


Figure 48 – C-V characteristics of SiON/TiN by plasma surface treatment gate stack with different annealing times.

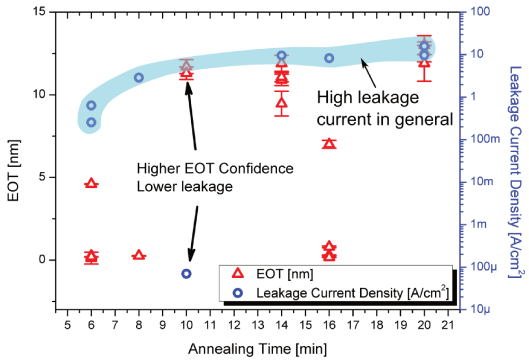
measurements in Figure 49d provide adequate confirmation that the EOT for the SiON dielectric is indeed 3.6nm. Table 9 summarizes the extracted EOTs and the associated extraction error for the different gate stacks, according to the discussion presented.

Table 9 – Extracted EOT for the different gate stacks

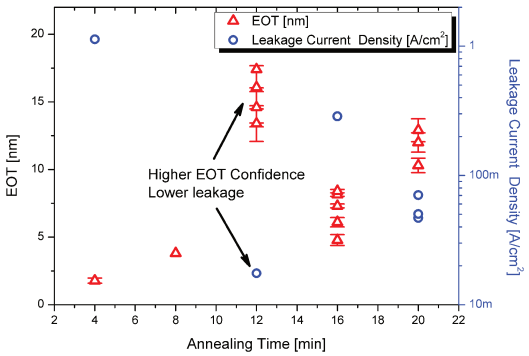
Gate Stack Structure	**Equivalent Oxide Thickness (EOT)**
SiON/TiN by reactive sputtering	3.6nm ± 0.09nm
SiON/TiN by plasma treatment	3.6nm ± 0.06nm
TiAlON/TiN by reactive sputtering	11.5nm ± 0.8nm
TiAlON/TiN by plasma treatment	15.2nm ± 1.38nm

Silicon oxynitride films present lower leakage currents than silicon oxide, and the work in (GUO; MA, 1998) shows SiON films with EOT of 1.5nm and leakage current densities as low as 2mA/cm^2, while our 3.6nm films present 10mA/cm^2 to 100mA/cm^2 leakage current density. Other results for SiON present much higher leakage current, such as 88A/cm^2 for 0.7nm (EOT) layers (MATSUSHITA et al., 2004), however, 0.7nm films present tunneling current that is not as prevalent in 3.6nm ones. Thickness non-uniformities in the SiON dielectric could be part of the reason for the high leakage in our case, where part of the film is much thinner than the rest. Charges in the dielectric – traps and vacancies – due to the plasma formation could also increase the leakage current, and may be reduced with a high temperature anneal after SiON growth (MA et al., 1993).

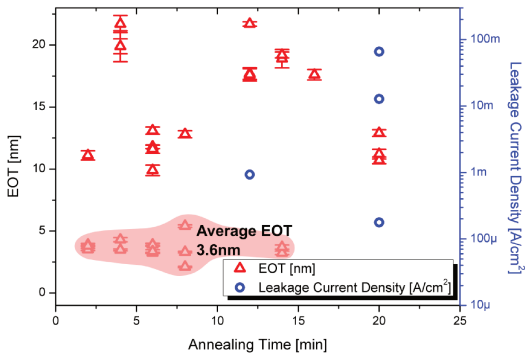
Comparing our TiAlON film with results for high-κ dielectrics, the work presented in (WILK et al., 2000) claims leakage current densities in the order of 10^{-6}A/cm^2 for hafnium silicates and in the work in (LEE et al., 2000) the current density though hafnium



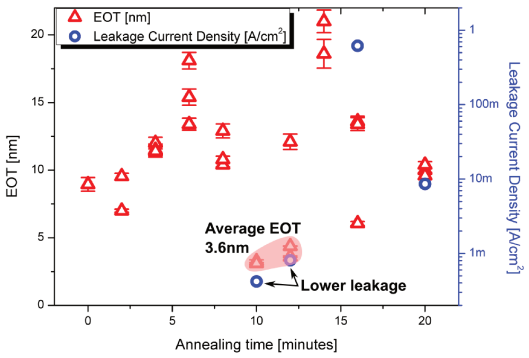
(a) Equivalent oxide thickness and leakage current at -1V for the TiAlON/TiN by reactive sputtering gate stack structure, which presents high overall leakage current density.



(b) Equivalent oxide thickness and leakage current at -1V for the TiAlON/TiN by plasma treatment gate stack structure.



(c) Equivalent oxide thickness and leakage current at -1V for the SiON/TiN by reactive sputtering gate stack structure, with leakage current density below 100mA/cm^2.



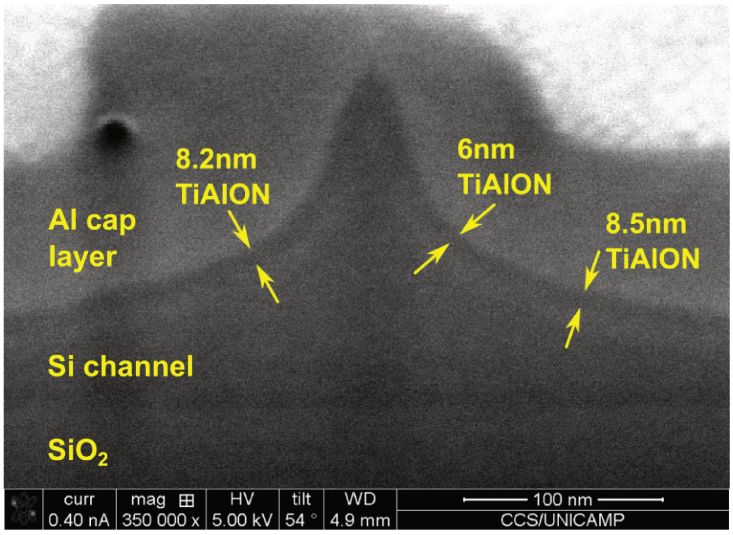
(d) Equivalent oxide thickness and leakage current at -1V for the SiON/TiN by plasma treatment gate stack structure, with most measured leakage current density below 10mA/cm^2.

Figure 49 – Comparison between EOT and leakage current density between TiAlON and SiON gate stack alternatives

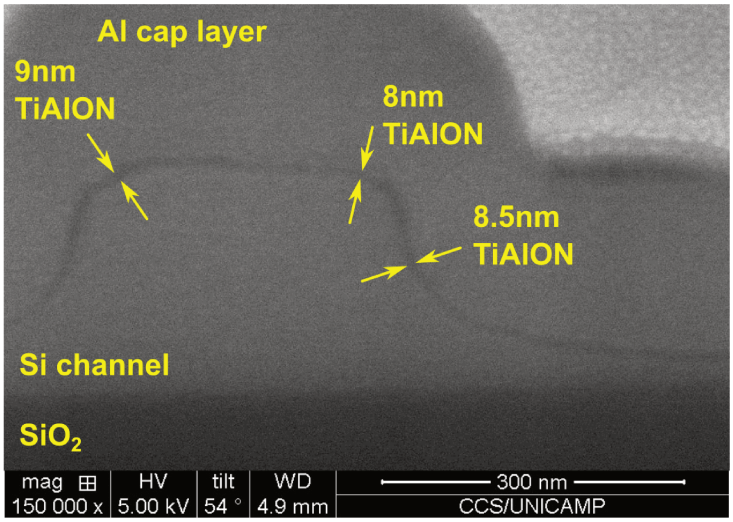
oxide is 10^{-2}A/cm^2. In the case of metal oxides and oxynitrides, such as TiAlON, a critical factor to obtain low leakage currents is the film crystallinity. For the case of Ta_2O_5, the leakage current increases three orders of magnitude when the material converts from amorphous to polycrystalline, with annealing (EZHILVALAVAN; TSENG, 1998). It is possible that the TiAlON film used in this work is not completely amorphous, and this would be an explanation for the high leakage current density measured and presented in Figure 49a. Since TiAlON is formed by metallic Ti and Al deposition and subsequent plasma oxynitridation, remains of the polycrystalline nature of the metallic films could still be present. The dielectric morphological characterisation, however, is beyond the scope of this thesis and is further discussed in Miyoshi (2008).

Thus, regarding work function values, V_{FB} parameter stability and, to a degree, leakage current density, it is considered that the SiON/TiN by plasma surface treatment gate stack presents the best characteristics, among the studied alternatives. Although TiAlON as an alternative high-κ dielectric is supported by other works (AUCIELLO et al., 2005; MIYOSHI, 2008; MIYOSHI et al., 2010; MIYOSHI et al., 2012), in this work the measured EOT is much higher than expected. It is still unclear whether the titanium from the electrode diffused to the dielectric layer, forming thus a thicker dielectric, or other process occurred. When comparing the formation methods for TiN, reactive sputter deposition and titanium evaporation followed by plasma surface treatment, the latter presents a lower overall leakage current for the SiON dielectric and improved parameter stability. The electrode work function for the TiN obtained using plasma surface treatment present values solely within the nMOS and mid-gap electrode ranges, for the different annealing times. This is not the case for the reactive sputter deposited TiN, that presents a higher degree of parameter variation. It is suspected that the parameter stability and suppression of leakage current is due to the very dense – and likely with lower density of vacancies – e-beam evaporated titanium, which serves as base for the TiN electrode. A 105μΩ.cm resistivity was assessed though four point probe measurements on the TiN films, and this rather low resistivity is indicative of a high density film (CHOU et al., 2001). Our reactive sputter deposited TiN films, on the other hand, present resistivity around 260μΩ.cm (LIMA, 2011).

To evaluate the physical thickness and step coverage of the TiAlON dielectric, cross sections have been performed on three dimensional MOS gate structures. Figure 50 presents the TiAlON layer on the three dimensional silicon channel, a thinner fin in Figure 50a and a wider pillar in Figure 50b. In both cases the TiAlON layer appears to fully envelop the structure, covering both horizontal and vertical features. Its physical thickness was estimated to be around 8nm, which roughly agrees with previous TEM measurements of 6.7nm (MIYOSHI et al., 2012). Comparing this estimated physical thickness with the equivalent oxide thickness (EOT) extracted from the C-V measurements, an inconsistency is noted: how can a high-κ dielectric present higher EOT than physical thickness? A definite answer for this question is not yet known, but it is suspected that the aluminium from the TiAlON dielectric is diffusing to the interface with the TiN electrode, creating a low-κ semi-metallic interface layer (KIM et al., 2004; KIM et al., 2008). This is supported by the WF reduction observed in Figure 46. A low-κ interface layer results in reduced total capacitance, even if the underlying dielectric has a high dielectric constant. As such, it can be the reason for the high value of the extracted EOT.



(a) TiAlON/TiN by reactive sputtering stack



(b) TiAlON/TiN by plasma treatment stack

Figure 50 – Silicon fin with TiAlON dielectric completely covering it for two different TiN formation methods. Physical thickness of TiAlON estimated around 8nm. Charging issues prevent observing the TiN layer in these SEM images.

4.3 FinFET Electrical Characterisations

The fabricated FinFETs have worked as nMOS transistors, as expected, and in this section their electrical characteristics will be discussed. The discussion has been divided between FinFETs fabricated by Al hard mask FIB milling and Ga^+ FIB lithography for the fin definition, due to their distinct characteristics regarding process-induced gallium incorporation, fin dimensions and, as will be seen, electrical performance. Electrical parameters have been extracted from the transistor measurements, to assist the discussion and allow comparisons between the devices and with other results from the literature. The parameter extraction procedures are further detailed in Appendix A.

4.3.1 Al hard mask FIB milling

Electrical characterisations of the FinFETs fabricated by Al hard mask FIB milling have been performed to extract electrical parameters such as output resistance (R_{OUT}), threshold voltage (V_{th}), subthreshold slope and maximum transconductance. Figure 51 presents the I_{DS}xV_{DS} characteristics of the FinFETs, where the gate bias ranges from -2V to 2V with 0.5V steps. From the linear region slope of the highest gate bias curve we can qualitatively assess a relatively high source and drain series resistance (R_{SD}). This conclusion is confirmed by the R_{SD} extraction using the method described in (CAMPBELL et al., 2011), with further details being given on Appendix A.3. The fabricated FinFETs present R_{SD} of 70kΩ. Figure 52 presents the extraction graph, with where R_{SD} is evaluated for every value of the gate effective voltage (V_{GS}-V_{th}), and a single value is extracted from the trend in high gate bias. The high series resistance is partly caused by low source and drain junction doping concentration (N_D). Resistivity measurements by four-point probe were performed to determine N_D and junction resistivity measured was 3.32 mΩ, which is equivalent to a N_D of $2x10^{19}$ cm^{-3} (SZE; IRVIN, 1968; MOUSTY et al., 1974). This is a low doping concentration compared to current transistors N_D values of above 10^{20} cm^{-3} (LEE et al., 2015). Lower transconductance values are also a result of the increased series resistance due to lower phosphorus concentrations in the source and drain regions, which will be discussed later. Misalignments between gate and source/drain junctions also dramatically increase the series resistance, and the non-self-aligned replacement metal gate process used in this work is prone to such misalignments. A self aligned process could be developed be either replacing the Al cap layer on the TiN gate by a metal with high melting point such as tungsten – in a gate first process (SEO et al., 2011) –, or depositing an oxide and using chemical mechanical polishing (CMP) after dopant activation, to remove the dummy gate – a self-aligned gate last process (CHATTERJEE et al., 1997; PACKAN et al., 2009).

Regarding the gate control over the drive current, it can be observed that a 0.5V variation in the gate bias results in approximately 0.5µA variation in the drain current. A higher drain current response with the gate bias variation can be obtained by reducing the gate dielectric effective thickness. Increasing the gate leakage current, now below 0.5nA at V_{GS}=2V, should be avoided when reducing the dielectric thickness. The output resistance of 55MΩ is given as the inverse slope of the linear fit on the saturation current (HUANG et al., 1992). The extracted R_{OUT} is comparable with FinFET prototypes fabricated in other works (HISAMOTO et al., 2000; KAVALIEROS et al., 2006; NATARAJAN et al., 2014). High output resistance is desired for both analog and digital applications, and the fabricated FinFETs show promising results. Reductions in the channel length, however, should pressure for process improvements in order to maintain the device output characteristics.

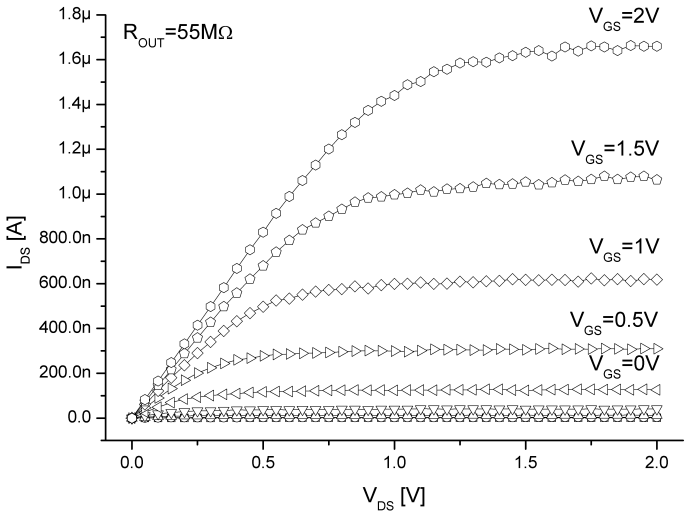


Figure 51 – $I_{DS}xV_{DS}$ of Al hard mask milled FinFET

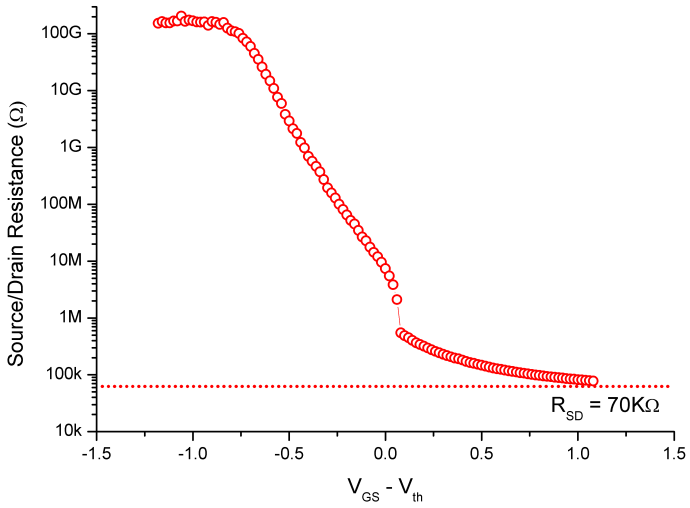


Figure 52 – R_{SD} of Al hard mask milled FinFET

The threshold voltage in the linear region, extracted from the $I_{DS}xV_{GS}$ curve in Figure 53, is -1.3V. Since no V_{th} adjustment has been performed, this parameter is controlled mostly by the TiN work function. We are studying single prototype FinFETs and thus a negative V_{th} can be accepted. If applied to a circuit, however, the V_{th} of the transistors should be carefully adjusted. The limited transconductance of 500nS in the linear region, shown in Figure 53 is attributed to the single fin design which restricts the maximum current flow, and it is expected to increase as a multiple fin prototype is developed. The decrease of 86% in the transconductance with a 1V increase in V_{GS} indicates that mobility scattering mechanisms are severe in the device. Scattering can be attributed mostly to fin surface roughness in this case, and optimizations can be performed.

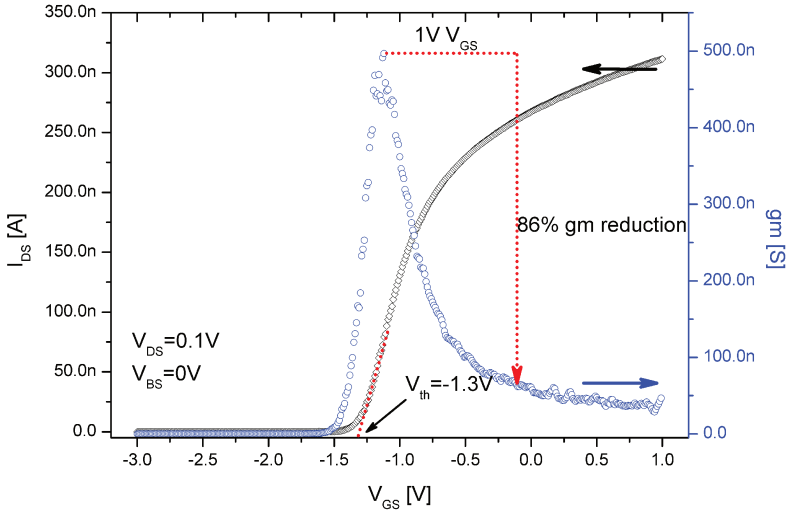


Figure 53 – $I_{DS}xV_{GS}$ of Al hard mask milled FinFET

The very high series resistance also contributes to reduce the maximum transconductance, and to remove its effects from the extracted parameters, the Y-function (GHIBAUDO, 1988; DIOUF et al., 2013) was employed. Both V_{th} and low field mobility (μ_0) can be evaluated by plotting $Y(V_{GS})$, with Y given by Equation 4.1. From Figure 53 the $Y(V_{GS})$ was calculated an is presented in Figure 54. From it, linear fit in the strong inversion region provides V_{th} as the x-axis intersection, and low field mobility (μ_0) can be extracted from the slope, as shown in Equation 4.2.

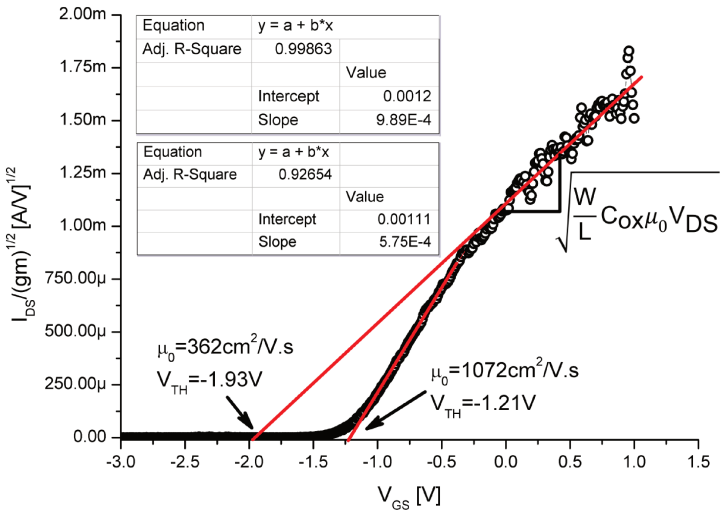


Figure 54 – $I_{DS}/\sqrt{gm}$ versus V_{GS} showing the extraction procedure for the Y-Function method.

$$Y = \frac{I_{DS}}{\sqrt{gm}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_{DS}} \, (V_{GS} - V_{th}) \tag{4.1}$$

$$Slope = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_{DS}} \tag{4.2}$$

The result, however, is not perfectly linear, as assumed by the method. Two fittings are performed, to present the distinction between the extracted parameter values, in the lower part of the curve, and in the upper part. In the lower part, the value of V_{th}, -1.21V, is close to that extracted in Figure 53, -1.3V. from Equation 4.2, knowing that the channel width and length are 251nm (from the cross section in Figure 44) and 5µm respectively, that C_{ox} is 18µF/cm^2 for this devices, and that V_{DS} is 0.1V, we can calculate μ_0. The low field mobility (μ_0) of 1072cm^2/V.s is much higher than expected, though. From (RUDENKO et al., 2008) it is expected that long channel relaxed silicon FinFETs with SiON dielectric present μ_0 below 600cm^2/V.s. The linear fitting of the region with higher bias, however, provides more credible results, with μ_0 of 362cm^2/V.s. This value for the carrier mobility is reinforced by a separate measurements of the same run of devices, with the same 0.1V of drain bias, which was also used for the Y-function extracted, and is presented in Figure 55. In this case, the resulting curve is considerably more linear, and a linear fitting results in -0.85V of V_{th} and mobility equals to 372cm^2/V.s. This value of mobility agrees with the previous, and 372cm^2/V.s is thus accepted as the extracted value for the μ_0 parameter. The threshold voltage parameter extraction in Figure 54 has to be analysed critically also. Returning to the I_{DS}vV_{GS} measurement in Figure 53, its clear that when V_{GS} is -1.93V, the FinFET is not conducting, as opposed to the gate bias of -1.21V. While we determine V_{th} as -1.21V, it can also be concluded that while the Y-function extraction is a rather effective tool to remove the series resistance effects from the transistor measurements, when non-linearities are present in the Y(V_{GS}) graph, the linear fitting has to be done carefully. The low field mobility is better extracted from the part of the curve with higher gate bias, such as that the transistor is in strong inversion and the mobility characteristics are better represented. The threshold voltage, however, is more reliably extracted from the region near the curve bend, closer to the x-axis intersection.

The leakage current of 10pA seen in Figure 56, is in accordance with current technology devices, and shows an adequate gate-to-channel coupling (JURCZAK et al., 2009), which in turn implies the successful operation of the top gate as well as the side gates. The subtheshold slope of 120mV/dec, seen in the same graph, is considerably better than previous results using the focused ion beam, but still not ideal (LIMA et al., 2013). Interface trapped charges explain both the mobility scattering observed in the transconductance curve and the degradation of subthreshold characteristics. Traps

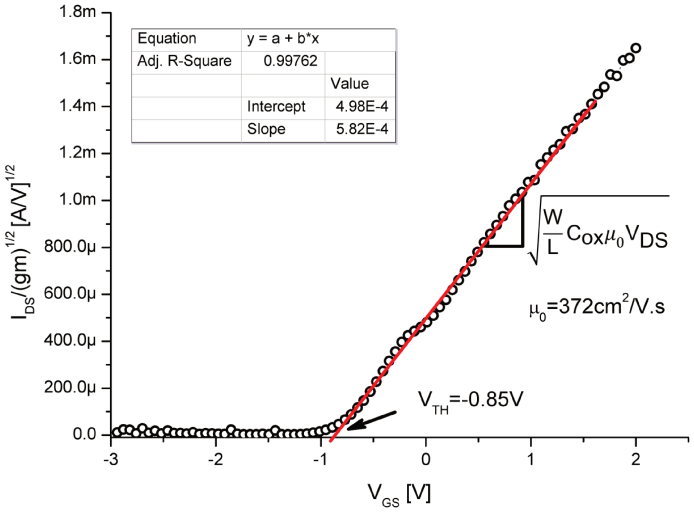


Figure 55 – $I_{DS}/\sqrt{gm}$ versus V_{GS} showing the extraction procedure for the Y-Function method for a different measurement, from the same FinFET run.

can arise from either vacancies and defects created by Ga^+ FIB processing during fin definition or from surface sputtering during SiON plasma growth (LIMA et al., 2015).

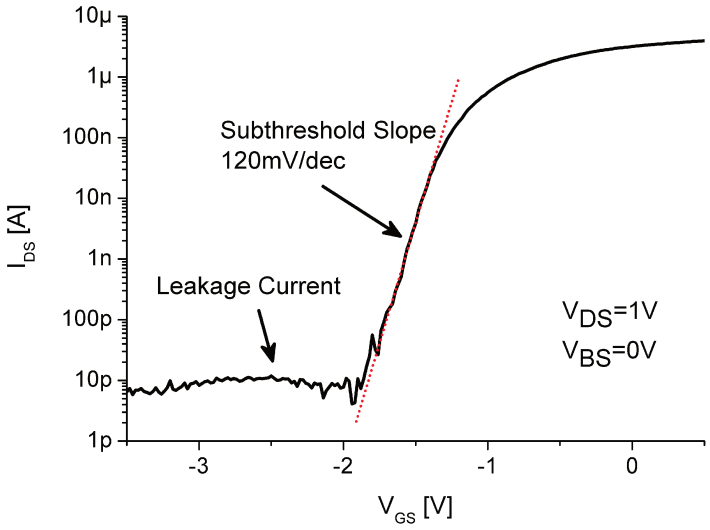


Figure 56 – Subthreshold characteristics of Al hard mask milled FinFET

4.3.2 Ga^+ FIB Lithography

As seen in Subsection 4.1.1, when using Ga^+ FIB lithography for fin definition, a sharp reduction in random gallium incorporation in the transistor channel is achieved. It was expected that improved device electrical behaviour would thus be a result. The FinFETs fabricated using this method, however, either did not work, or presented deterio-

rated electrical characteristics, which will be discussed in this subsection. Some hypothesis are proposed to explain why the change from Al hard mask milling fin definition to Ga^+ FIB lithography fin definition resulted in loss of transistor performance:

- Fin dimensions reduced from 175nm fin width and 70nm fin height to 100nm fin width and 40nm of fin height. The reduced fin dimensions impose higher restrictions on cleaning procedures in order to reduce fin damage.
- Fin cross section shape changed from trapezoidal to round or triangular with round sides. Round shapes are challenging to guarantee conformal thin film coverage, and void in the gate dielectric or electrode could prevent the transistor from working.
- Gallium incorporation in the fin provides p-type doping in the channel that gives rise to clear source and drain junctions upon ion implantation. The p-type channel is able to successfully constrain the source and drain junction leakage current.

Nonetheless, some devices presented transistor behaviour, and will be discussed in the following paragraphs, focusing on their gate stacks and electrical characteristics.

4.3.2.1 TiAlON/TiN by reactive sputtering

FinFETs with TiAlON dielectric and TiN metal gate deposited by reactive sputtering worked with distinct $I_{DS}xV_{DS}$ transistor characteristics, presented in Figure 57. If we compare the drain current in this case with the last transistor presented, we have that now, for 1V V_{GS} and 2V V_{DS}, I_{DS} is 0.73µA, while in the other transistor it is 0.6µA. In this present case, however, the FinFET has nine parallel fins, instead of a single fin. This means that the drain current increase is in fact a decrease per fin.

In Figure 58a it can bee seen that the extracted V_{th} is -85mV, much closer to zero than in the former case, where V_{th} was -1.3V. This threshold voltage shift towards mid-gap values – which is, closer to zero – reflects the work function evaluation of the TiAlON/TiN by reactive sputtering gate stack, performed in Section 4.2. This gate stack presented work function values predominantly in the mid-gap electrode range.

The subthreshold characteristics are also degraded for this device. As seen in Figure 58b, the subthreshold slope is 200mV/dec, indicating a high interface trap density. The minimum leakage current around 30pA, which rapidly increases as V_{GS} decreases indicates that the channel cannot properly close, even when the gate bias is set to negative values.

The source and drain series resistance (R_{SD}) was extracted using the Campbell et al. method (CAMPBELL et al., 2011) as in the previous case, and for this device the series resistance is 2.3MΩ, more than thirty time higher than the last result presented, even though the source and drain doping was increased from $2x10^{19}$ cm^{-3} to $7x10^{19}$ cm^{-3}

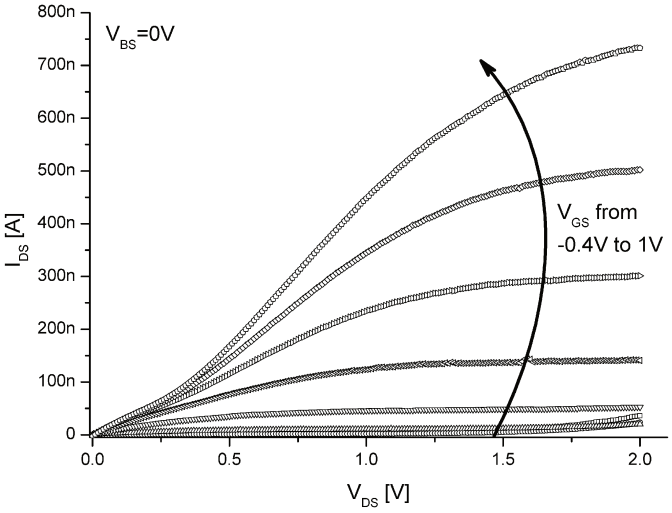


Figure 57 – $I_{DS}xV_{DS}$ of FinFET with TiAlON/TiN by reactive sputtering gate stack

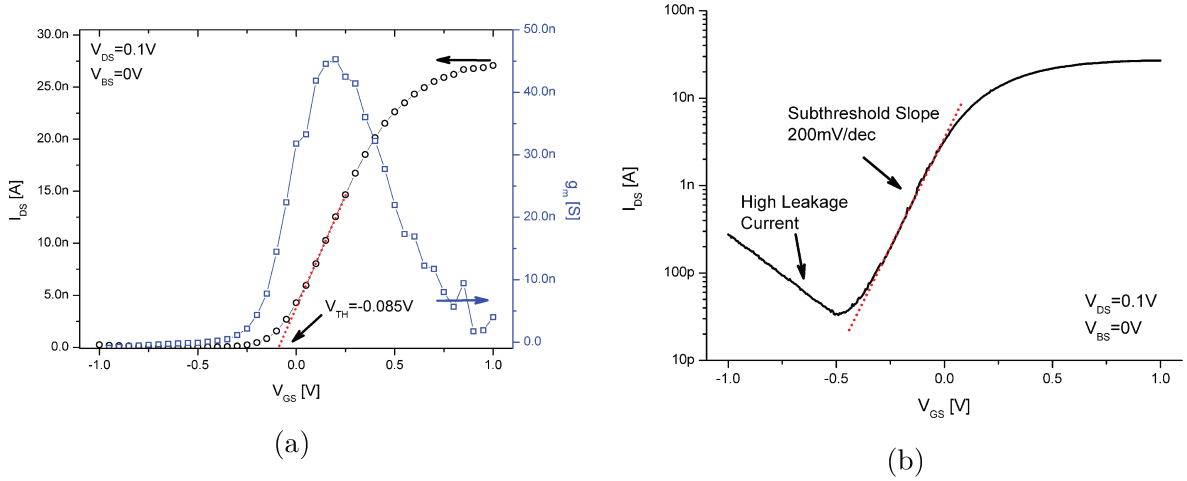


Figure 58 – $I_{DS}xV_{GS}$ of above-threshold (a) and subthreshold (b) characteristics of FinFET with TiAlON/TiN by reactive sputtering gate stack

according to the four-point-probe measurements. The high series resistance could be seen qualitatively from the $I_{DS}xV_{DS}$ curve in Figure 57 in the region of low drain bias where the transistor is not yet responding, resembling a bird's beak. Furthermore, it is difficult to clearly identify the linear and saturation regions from this graph, another indicative of high series resistance. Series resistance increase can be linked to gate misalignment, which introduces a high parasitic resistance in the channel.

Using the same Y-function extraction (GHIBAUDO, 1988) of μ_0 and V_{th} for the measured data of this device, to account for the high series resistance, we note on Figure 59 that the curve in strong inversion does not present a clearly linear region, as in the previous case, where the linear fitting should be performed. We then have to choose a semi-linear region where to to fit the extraction curve. Following the assesment done in

the previous case, the higher gate bias region is chosen for the mobility extraction, while the threshold voltage is extracted using the lower gate bias region. When fitting the higher portion, the resulting slope is higher ($7.7\text{x}10^{-4}$ compared to $5.75\text{x}10^{-4}$), but the extracted low field mobility (μ_0) is lower. This is mainly due to the transistor width, that is now 1.25µm, since in this case we have a multiple fin FinFET. The μ_0 of $81.78\text{cm}^2/\text{V.s}$ further solidifies the analysis that the drain current has not followed the increase in gate width. V_{th} is extracted through the Y-function method as the x-axis intersection of the linear fit of the $Y(V_{GS}$ curve near the bend, as discussed prior, and its value is -0.03V. Again, it is higher than the V_{th} extracted using the simplified extrapolation method, which can also be attributed to parameter shifts caused by the high series resistance. This is expected, however, and in Figure 60, from (TAUR, 2000), it can be seen that when removing the effect of series resistance from the measurements the parameter values are altered. The intrinsic device – or effective, as in Leonhardt et al. (2015) – is how the transistor behaves without parasitic effects, and from this characteristics the parameters are more reliably extracted.

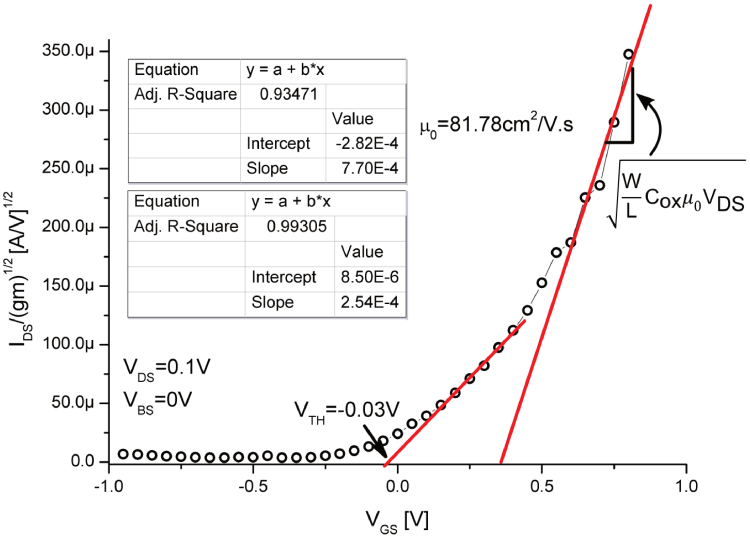


Figure 59 – $I_{DS}/\sqrt{gm}$ versus V_{GS} showing the extraction procedure for the Y-Function method.

4.3.2.2 SiON/TiN by plasma surface treatment

While in the gate stack evaluations, the SiON/TiN by plasma surface treatment gate stack was assessed as the best alternative, the FinFETs fabricated using this combinations have worked only to a certain extent. Figure 61 presents the output characteristics of a FinFET fabricated using Ga^+ FIB lithography for fin definition and with the SiON/TiN by plasma surface treatment gate stack. It can be seen that although the gate bias does control the drain current – increasing V_{GS} by 0.2V increases I_{DS} by 70nA at a drain bias

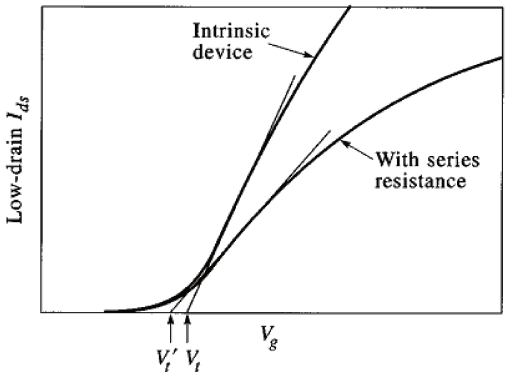


Figure 60 – Transistor $I_{DS}xV_{GS}$ characteristics at low V_{DS} with and without the series resistance effect, showing how the extraction of V_{th} is dependant on this parameter. From (TAUR, 2000)

of 4.5V – the device characteristics are not good. In the region of low V_{DS} the curves as superimposed, indicating low gate control. Furthermore, even with 0V of gate bias the transistor presents significant drain current, which increases with the drain bias increase – a resistor-like behaviour. This indicates that the channel does not fully close, and a high leakage current is present. From the $I_{DS}xV_{GS}$ measurements in Figure 62 we have that the drain current is 2.6nA when the gate bias is -1V, well below threshold. When comparing to the 10pA leakage current in the Al hard mask milled FinFET, it is possible to see that indeed leakage is an issue in this device.

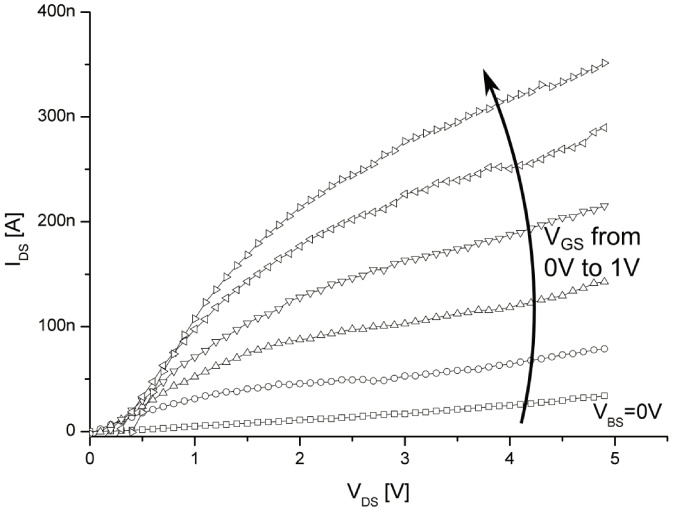
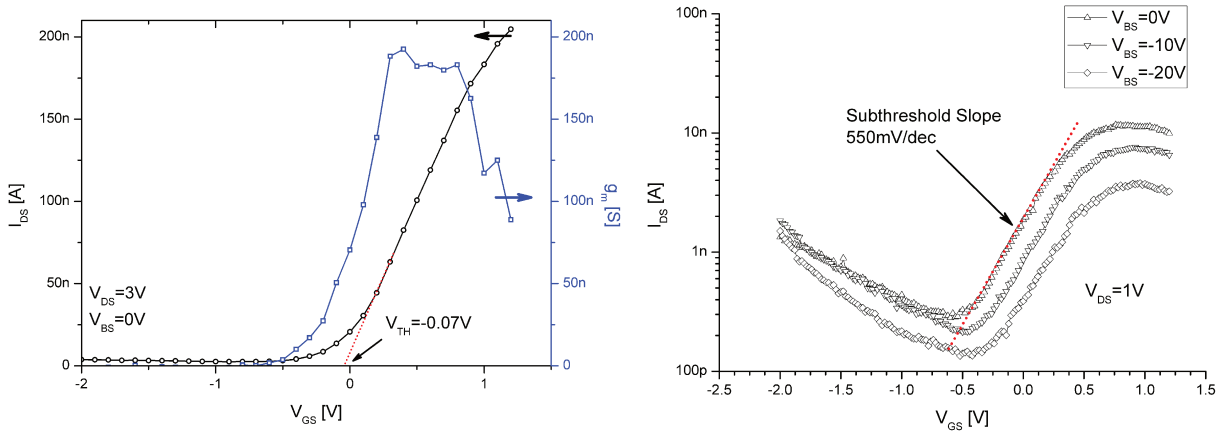


Figure 61 – $I_{DS}xV_{DS}$ of FinFET with SiON/TiN by plasma surface treatment gate stack

The $I_{DS}xV_{GS}$ characteristics of the FinFET were measured for a drain bias of 3V, to avoid the contact issues at low drain bias, seen in Figure 61a. A low value of maximum transconductance can be observed, below 200nS, even for this high drain bias. In Figure 61b the FinFET has been measured using a drain bias of 1V to analyse its subthreshold

characteristics. Voltage steps of -10V have been applied to the backside of the transistor, and we observe that for V_{BS} of -20V the leakage current decreases considerably, even though it remains much higher than expected. A 500mV/dec subthreshold slope is even farthest from optimal than the previous FinFET analysed.

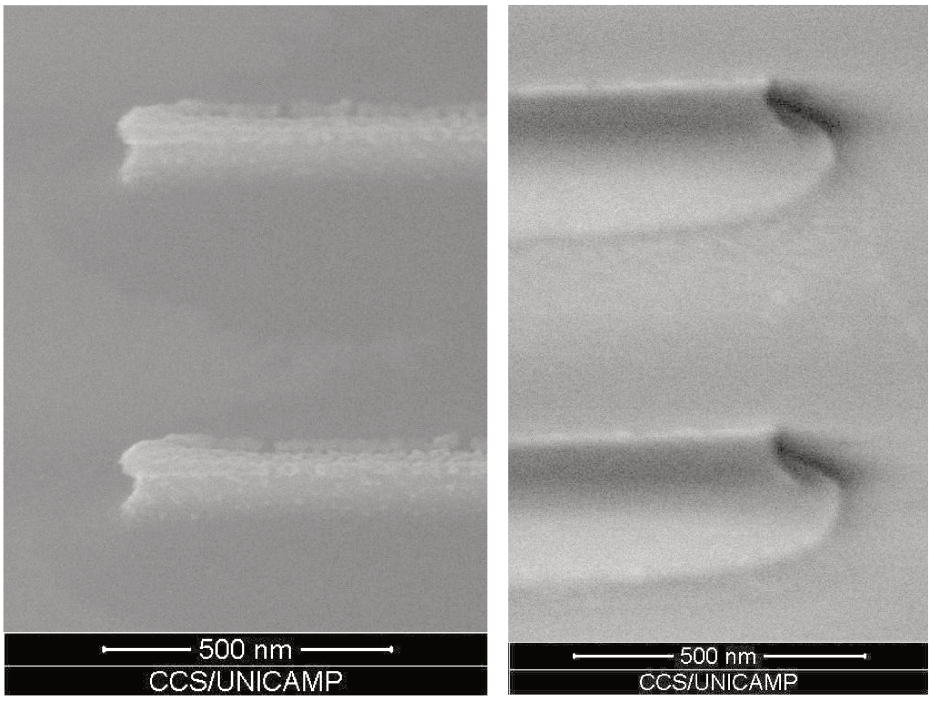


(a) (b)

Figure 62 – I_{DS}xV_{GS} of above-threshold (a) and subthreshold (b) characteristics of FinFET with SiON/TiN by plasma surface treatment gate stack

The degraded characteristics presented by this FinFET prevent accurate parameter extractions. From the previous results we can qualitatively asses that the series resistance in this case is even higher than the 2.3MΩ extracted in the previous. A series resistance as high as 5MΩ could explain the curves superimposition when V_{DS} is low, seen in Figure 61, which are characteristic of contact issues in the transistor. Also, the low transconductance at 3V of drain bias, in Figure 61a is also an indicative of series resistance issues, as well as low carrier mobility. While a definite answer for the low field mobility (μ_0) is not possible for this case, is is considered that this parameter is even lower than 81.78cm^2/V.s, as in the last case, since this FinFET characteristics are much degraded. We believe that the mobility, in this case, is below 50cm^2/V.s,which is unacceptable for long channel FinFETs. The lower mobility could be due to remote phonon scattering from vacancies in the TiN electrode, created during the plasma surface treatment, but the relatively thick dielectric should be able to screen this scattering. It is believed that the interface charge density in this device is fairly high, which explains both the low mobility and the high subthreshold slope. In the work presented in (KOBAYASHI et al., 2011), electron mobility degradation and increase in the subthreshold slope were observed after proton irradiation, which increases the number of charged interface traps. In Zhu et al. (2004) Coulomb scattering due to interface trapped charges is also the main cause for mobility degradation. In the fabricated FinFETs, sacrificial oxidation just after fin etch greatly reduces the fin roughness, as seen in Figure 63 before and after it.

Residual roughness in the fins may still remain, however. Plasma growth of SiON can further introduce trapped charges in the interface, whose effect is more apparent in the FinFETs fabricated by Ga^+ FIB lithography due to the narrow fin resulting from this technique. Despite the remote plasma processing in the ECR system where the SiON dielectric is grown, surface sputtering may still be occurring, which potentially lead to increase trapped interface charge density in the fins. One possibility to reduce the interface traps is to perform a rapid thermal annealing (RTA) after dielectric growth, which reportedly can reduce its density in up to one order of magnitude (MA et al., 1993).



(a) (b)

Figure 63 – Silicon fin before (a) and after (b) sacrificial oxidation and oxide stripping, showing how the sidewall roughness greatly reduces.

It is important to point that the degraded electrical characteristics of this transistor in fact supports the assessment, made on Chapter 1, that novel gate stack materials should be tested on transistors, and more important, 3D transistors, to provide an accurate and complete characterisation. The SiON/TiN by plasma surface treatment was identified as the best option, when the alternative gate stacks were studied. That study, however, only involved C-V characteristics and leakage measurements of gate stack structures. When applied to a FinFET, this same gate structure does not perform as expected, which can be attributed to its sensitivity to device and process aspects particular to FinFETs – step coverage, sidewall roughness, carrier mobility scattering and others.

5 Conclusions and Future Work

In this work, different methods for FinFET prototyping were studied. Fin definition through fin FIB milling, aluminium hard mask FIB milling and Ga^+ FIB lithography were evaluated. Comparisons based on process induced gallium incorporation and fin dimensions were performed, and the fins fabricated using Ga^+ FIB lithography presented superior characteristics. FinFET prototypes have been fabricated using two of these methods, with better results being achieved by the Al hard mask FIB milling fin definition. The reasons for the low performance of FinFETs fabricated using Ga^+ FIB lithography are suspected to be due both with the lower Ga incorporation in the fins and with the fin dimensions, which makes them more susceptible to process related damages. Comparing the two processes, it is important to point that Al hard mask milling is an adaptation of a mature process with confirmed results (LIMA et al., 2013), while the Ga^+ FIB lithography for fin definition was developed entirely in this work, from the identification of the gallium masking to calibration of the fin definition process and application to working FinFET devices.

Nonetheless, possibly the most important contribution of this work is the development of a novel method for multiple fin FinFET prototyping, which provides great flexibility regarding the number of fins and fin width. It allows device fabrication using a Ga^+FIB with greatly reduced processing time and process induced gallium incorporation in the sample. A FIB/SEM system is a versatile equipment, and in conjunction with this technique, complex prototype devices can be more easily fabricated in research institutes. It is believed that the present difficulties can be overcome and FinFETs with adequate electrical behaviour can be fabricated using this method for fin definition.

Although optimal electrical performance could not be achieved with the fabricated FinFETs, important developments have been presented regarding prototyping methods and gate stack alternatives. An effort towards process integration for the successful fabrication of FinFETs has been made, and slight changes can allow devices with different gate stacks, source and drain silicidation and other features. Most fabrication steps have been carefully evaluated, and this work has presented details and parameters such as that the FinFET prototype fabrication could be replicated. Special attention was given to in depth evaluation of the results, both structural – such as cross sections with magnification close to the FIB/SEM resolution limit – and electrical – with careful parameter extraction and result discussion. It is expected that such attention to detail helps future works in device prototyping, either in replicating the processing itself and in comparing the results.

Alternatives were explored in both the FinFET gate stack and in the fin definition.

Table 10 presents the parameter comparison between different studied gate stacks, and highlights the spread of parameter values observed. The SiON/TiN by plasma treatment gate stack alternative is regarded as the best option in terms of parameter stability, since both the work function and the flat band voltage show little spread for the different measurements. This results in almost superimposed C-V curves, for the different annealing times. In regard to leakage current density, the TiAlON dielectric still presents problems, which can be attributed to layer crystallization. The SiON/TiN by reactive sputtering gate stack presents the lowest leakage current density, with its maximum reaching only up to 65mA/cm^2 at -1V.

Table 10 – Parameter comparisons of gate stack alternatives

	Reactive Sputtering TiN	**Plasma Nitridated TiN**
SiON dielectric	**WF** 3.2eV to 4.46eV **V_{FB}** -3.8V to -0.55V **EOT** 3.6nm **Leakage** 177µA/cm^2 to 65mA/cm^2	**WF** 4.25eV to 4.69eV **V_{FB}** -0.73V to -0.31V **EOT** 3.6nm **Leakage** 420µA/cm^2 to 0.61A/cm^2
TiAlON dielectric	**WF** 1.34eV to 5eV **V_{FB}** -9.3V to -0.01V **EOT** 11.9nm **Leakage** 70µA/cm^2 to 15.8A/cm^2	**WF** 2.6eV to 4.8eV **V_{FB}** -2.4V to -0.14V **EOT** 13.4nm **Leakage** 17mA/cm^2 to 1.1A/cm^2

Different FinFET devices have been fabricated, with different gate stacks and different fin definition methods, rendering a range of morphological and electrical parameters, which are presented in Table 12. Again, it can be noted that the FinFETs fabricated using the Al hard mask FIB milling fin definition method present superior electrical characteristics, such as higher carrier mobility, lower subthreshold slope and lower series resistance. The threshold voltage is much more negative than expected for a mid-gap or nMOS electrode such as TiN, and can be attributed to interface dipoles and charges in the gate stack. Nonetheless, important morphological achievements were obtained with the FinFETs fabricated by Ga^+ FIB lithography method, both in terms of the number of fins and the fin width. It is believed that minor process adjustments will results in improved performance, when using this technique.

Valuable improvements regarding FinFET fabrication in Brazilian research institutes have been achieved. Table 12 compares morphological and electrical parameters of FinFETs presented in the works of (LIMA et al., 2013) and (RANGEL et al., 2013) with the devices presented in this work. Where the parameter has not been explicitly given, it was estimated from the published graphs and images. It can be seen that this work presents important contributions regarding number of fins and dimensions, alternative dielectric materials, as well as dramatically reducing the subthreshold slope. Although a subthreshold slope of 120mV/dec is still much higher than the ideal value of 60mV/dec, it still shows that achievements are being made. The low field mobility (μ_0) of 372cm^2/V.s,

extracted after removing the parasitic elements, is a very good result, consistent with relaxed silicon channel FinFETs reported elsewhere (RUDENKO et al., 2008).

Table 11 – Parameters of the different FinFETs presented in this work

Parameters	**FinFET Al Hard Mask FIB Milling**	**FinFET Ga^+ Lithography**	**FinFET Ga^+ Lithography**
Fin Definition Method	Al Hard Mask FIB Milling	Ga^+ FIB Lithography	Ga^+ FIB Lithography
Number of Fins	1	9	9
Fin Width	170nm	87nm	100nm
Gate Length	5µm	5µm	5µm
Gate Dielectric	SiON	TiAlON	SiON
Gate Electrode	TiN by reactive sputtering	TiN by reactive sputtering	TiN by plasma treatment
$\mathbf{V_{th}}$	-1.21V	-0.03V	-0.07V
$\mathbf{\mu_0}$	372cm^2/V.s	81.78cm^2/V.s	below 50cm^2/V.s
Subthreshold Slope at V_{BS}=0V	120mV/dec	200mV/dec	550mV/dec
I_{DS} at V_{GS}=1V and V_{DS}=1V	0.6µA	0.44µA	0.1µA
$\mathbf{R_{SD}}$	70kΩ	2.3MΩ	∼5MΩ

Table 12 – Parameter comparison between FinFETs fabricated in Brazilian research institutes

Parameters	**FinFET in Lima et al. (2013)**	**FinFET in Rangel et al. (2013)**	**FinFETs in this work**
Fin Definition Method	FIB Milling	EBL	FIB Milling and Ga^+ FIB Lithography
Number of Fins	1	1	1 and 9
Fin Width	100nm	210nm	175nm to 87nm
Gate Length	10µm	2.5µm	5µm
Gate Dielectric	SiO_2	SiO_2	SiON and TiAlON
Gate Electrode	TiN/Al	Poly-Si	TiN/Al
$\mathbf{V_{th}}$	0.5V	-0.25V	-0.85V to -0.03V
Subthreshold Slope at V_{BS}=0V	320mV/dec	250mV/dec	120mV/dec
I_{DS} at V_{GS}=1V and V_{DS}=1V	0.65µA	8.25µA	0.6µA

Some open questions still remain from the study of gate stack alternatives. A thorough evaluation of the TiAlON dielectric is needed, in order to identify the origin of the work function reduction and EOT increase. SIMS characterisations could confirm what was pointed, in this work, as the reason: Al segregation to the dielectric-electrode

interface. Moreover, step coverage evaluation should be performed on the TiN electrode formed by e-beam evaporation and plasma nitridation, similar to what was performed for the TiAlON layer. Transmission electron microscope (TEM) measurements should be done for the accurate assessment of this electrode, on 3D structures, to evaluate its suitability for 3D transistors.

As future work, alternatives to optimize the FinFET electrical characteristics still exist. It is suspected that the plasma growth of SiON creates defects and traps in the interface, which degrade the subthreshold slope. A thin thermally grown SiO_2 interfacial layer could be used to improve the interface, or high temperature thermal annealing of the obtained SiON film could reduce the interface trap density. Besides improving the subthreshold slope, the mobility is also expected to increase with this treatment. SiON, however, is not likely part of the future in CMOS transistors, and as such, future works should be focused on high-κ and higher-κ dielectrics for FinFETs. For the devices with TiAlON as a gate dielectric, the same thermal annealing might increase its density and improve the interface with the silicon substrate. Furthermore, a self aligned process for FinFET prototype fabrication should greatly reduce the devices series resistance. A gate first process could be implemented by replacing the aluminium cap layer in the gate by a metal with high melting point, such as tungsten. A self aligned replacement metal gate process could also be implemented with few changes, using oxide deposition and CMP following dummy gate deposition.

5.1 List of Publications

- Alessandra Leonhardt, Luiz F. Ferreira, Sergio Bampi and Leandro T. Manera, Effective device electrical parameter extraction of nanoscale FinFETs: Challenges and results **27th International Conference on Microelectronics (ICM)**, 2015.

- Carlos V. Carnio, Alessandra Leonhardt, Audrey R. Silva, Frederico H. Cioldin, Ioshiaki Doi, Leandro T. Manera and José A. Diniz, TiN gate electrodes fabrication by Ti e-beam evaporation and ECR plasma nitridation **25th Materials for Advanced Metallization (MAM)**, 2016.

- Carlos V. Carnio, Alessandra Leonhardt, Audrey R. Silva, Frederico H. Cioldin, Ioshiaki Doi, Leandro T. Manera and José A. Diniz, TiN gate electrodes fabrication by Ti e-beam evaporation and ECR plasma nitridation **Microelectronic Engineering, Proceedings of the 25th Materials for Advanced Metallization**, 2016 (Submitted).

- Alessandra Leonhardt, Frederico. H. Cioldin, Marcos V. P. dos Santos, Lucas P. B. Lima, José A. Diniz and Leandro T. Manera, Ga^+ focused ion beam lithography as a viable alternative for multiple fin FinFET prototyping **The 60th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN)**, 2016.

- Alessandra Leonhardt, Marcos V. P. dos Santos, Lucas P. B. Lima, José A. Diniz and Leandro T. Manera, Ga^+ focused ion beam lithography as a viable alternative for multiple fin FinFET prototyping **Journal of Vacuum Science & Technology B)**, 2016 (Submitted).

- Alessandra Leonhardt, Lucas P. B. Lima, Frederico. H. Cioldin, Marcos V. P. dos Santos, José A. Diniz and Leandro T. Manera, FinFET prototypes fabricated by aluminium hard mask FIB milling for fin definition and SiON/TiN/Al gate stack **31st Symposium on Microelectronics Technology and Devices (SBMicro)**, 2016.

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APPENDIX A – Parameter Extractions

This appendix will briefly explain the procedures used for electrical parameter extraction throughout the work. Al methods use transistor current-voltage measurements in certain bias conditions, which are further processed to result in the desired parameters.

A.1 Output Resistance

The output resistance (R_{OUT}) indicates how well the transistor behaves as a constant current source in the saturation region. This parameter is extracted as the inverse of the slope of the linear fit in of the drain current in saturation, as illustrated in Figure 64. The ideal value for the output resistance is infinity, which means that the drain current is perfectly constant when the transistor is in saturation mode. Channel length modulation reduces the output resistance, which is more pronounced in short channel devices.

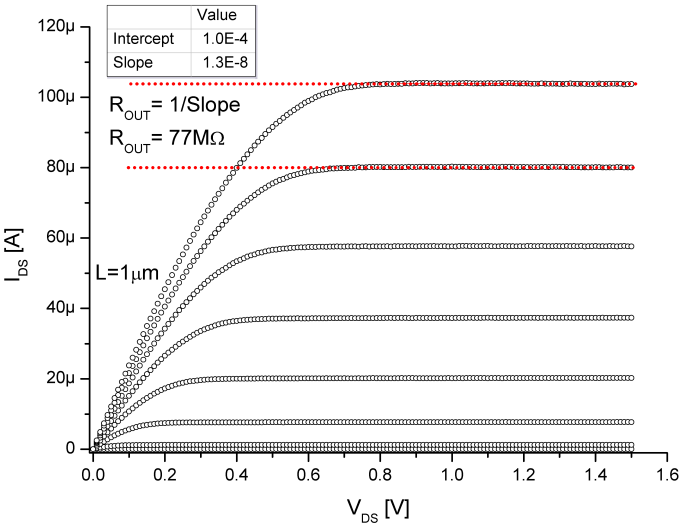

Figure 64 – Schematic of the procedure to extract the output resistance

A.2 Subthreshold Slope

The subthreshold slope is defined as the gate bias increase required to induce an increase in one decade – or ten times – in the drain bias. Figure 65 presents the schematic of the extraction procedure for the subthreshold slope, which was previously presented in Figure 56. In this case the increase of one decade in the drain current is caused by an increase of 120mV in the gate bias, and thus the subthreshold slope is 120mV/dec.

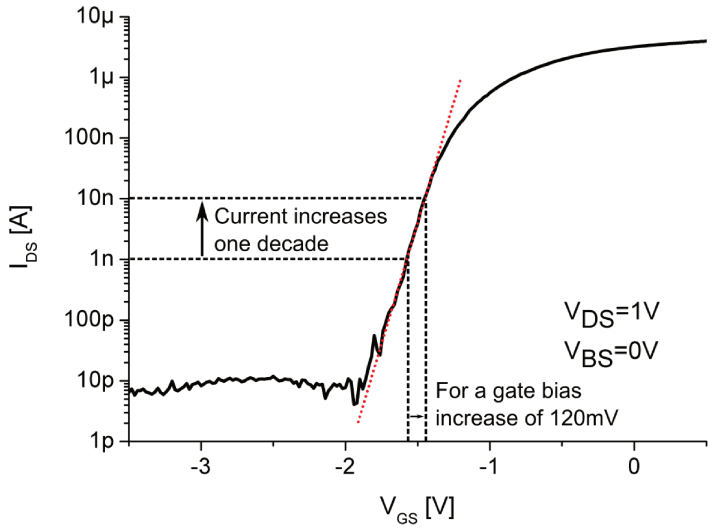

Figure 65 – Schematic of the procedure to extract the subthreshold slope

A.3 Series Resistance

The series resistance is extracted using the method presented in (CAMPBELL et al., 2011), which we later evaluated as suitable for nanoscale FinFETs extraction in (LEONHARDT et al., 2015). The methodology proposed uses the same device in two different – but very close – drain biases in order to obtain the series resistance as a function of the gate voltage overdrive. The extraction relies on the ratio of two $I_{DS}xV_{GS}$ curves

$$\frac{I_{D1}}{I_{D2}} = \frac{\mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \left(V_{GS} - V_{th1} - \frac{I_{D1} R_{SD}}{2}\right) (V_{D1} - I_{D1} R_{SD})}{\mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \left(V_{GS} - V_{th2} - \frac{I_{D2} R_{SD}}{2}\right) (V_{D2} - I_{D2} R_{SD})} \tag{A.1}$$

where the constants μ_{eff} (effective mobility), C_{ox} (oxide capacitance), W_{eff} (effective channel width) and L_{eff} (effective channel length) can be cancelled, since the measurements are made in the same device, yielding

$$R_{SD}^2 \left(\frac{I_{D2} - I_{D1}}{2}\right) + R_{SD} \left(V_{th2} - V_{th1} + \frac{V_{D1} - VD2}{2}\right) - \frac{(V_{GS} - V_{th1}) I_{D2} V_{D1} - (V_{GS} - V_{th2}) I_{D1} V_{D2}}{I_{D1} I_{D2}} = 0 \tag{A.2}$$

The source and drain resistance values are obtained after solving the polynomial equation. The method does not give a single value for the source and drain resistance, but its relationship with the gate voltage. A single value should be extracted from these curves at a high gate voltage, as discussed in (DIXIT et al., 2005).

Figure 66 presents the series resistance extraction for multiple FinFETs with the same fin width and different channel lengths, yielding a single value of series resistance of 302Ω at high gate bias. The graph and data has been extracted from (LEONHARDT et al., 2015), and the FinFETs were fabricated at IMEC and characterized on the PhD thesis of (FERREIRA, 2012). In (LEONHARDT et al., 2015) we conclude that this method provides consistent results since it only assumes that μ_{eff} and C_{ox} are constant for two very close drain bias.

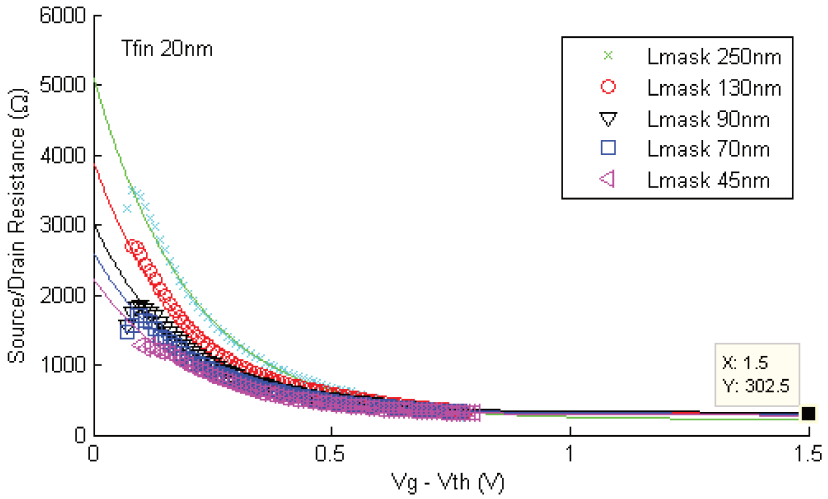

Figure 66 – Campbell et al. method with extrapolation of the curves to yield a single value for the series resistance R_{SD}.

A.4 Threshold Voltage and Low Field Mobility

In this work, the threshold voltage (V_{th}) is extracted in two different ways: by extrapolating the linear region of the $I_{DS}xV_{GS}$ and by using the Y-function method (GHIBAUDO, 1988). The Y-function method is also used to extract the low field mobility (μ_0).

The extrapolation method (ORTIZ-CONDE et al., 2002; SCHRODER, 2006) is a common and straightforward technique used to extract the threshold voltage by simply finding the x-axis intercept of the linear extrapolation of the $I_{DS}xV_{GS}$ curve at the point of maximum transconductance (g_m). A low drain bias should be applied to the device for this measurement. Figure 67 illustrates this method, and in this case V_{th} is -1.3V. This method is useful for a fast estimation of the threshold voltage, but the series resistance effects on the measurement reduce its accuracy. As discussed in the text, the value of V_{th} depends on the series resistance, and, as presented in Figure 68, when removing the parasitic elements from the transistor measurement, V_{th} shifts. Since the FinFETs fabricated in this work present high series resistance, a more accurate method to determine the threshold voltage is using the Y-function extraction.

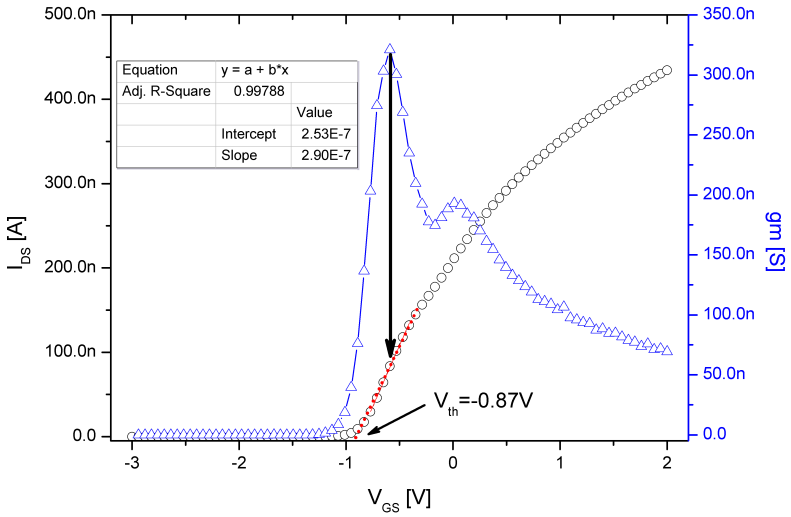

Figure 67 – Extraction procedure for the V_{th} parameter by extrapolating the I_{DS}xV_{GS} curve at the point of maximum transconductance.

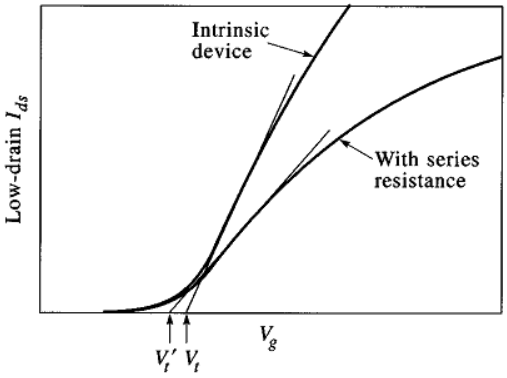

Figure 68 – Transistor I_{DS}xV_{GS} characteristics at low V_{DS} with and without the series resistance effect, showing how V_{th} changes when removing its effect. From (TAUR, 2000)

For the Y-function extraction we define Y as

$$Y = \frac{I_{DS}}{\sqrt{gm}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_{DS}} \, (V_{GS} - V_{th}) \tag{A.3}$$

when plotting Y(V_{GS}) we have a linear region, in strong inversion, where a linear fitting is performed. The slope of the resulting curve is given by

$$Slope = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_{DS}} \tag{A.4}$$

and μ_0 can thus be calculated if the channel length, width and oxide capacitance are known, as presented in Equation A.5. The x-axis intersection of the extrapolation of

the linear fitting provides V_{th}.

$$\mu_0 = Slope^2 \frac{L}{W} \frac{1}{V_{DS}} \frac{1}{C_{ox}} \tag{A.5}$$

Figure 69 presents a typical Y-function extraction, already presented in Figure 55. It is possible to observe that the plot of $Y(V_{GS})$ is fairly linear in strong inversion, allowing a precise extraction. The threshold voltage is given by the x-axis intersection, as -0.85V. The mobility is calculated from the slope of the linear fitting and is equal to $372cm^2/V.s$ in this case. The main advantage of this method is that since it divides the drain voltage by the transconductance, the series resistance influence on the extraction is minimized.

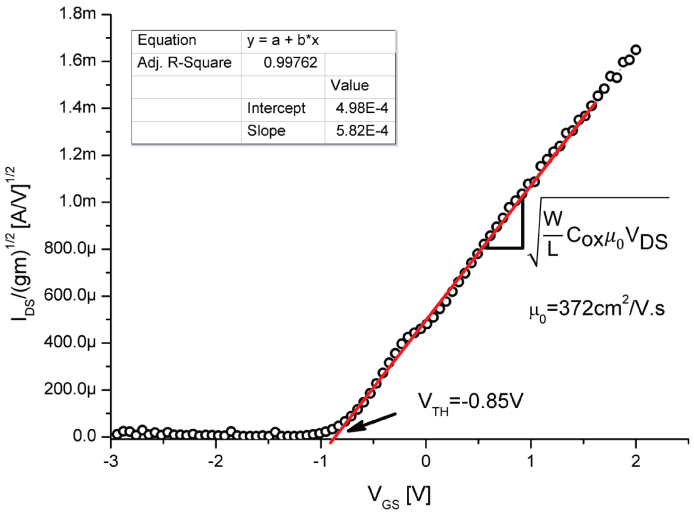

Figure 69 – $I_{DS}/\sqrt{gm}$ versus V_{GS} showing the extraction procedure for the Y-Function method