METAL GATE WORK FUNCTION ENGINEERING FOR FUTURE CMOS TECHNOLOGY NODES

LUCAS PETERSEN BARBOSA LIMA

CAMPINAS
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LUCAS PETERSEN BARBOSA LIMA

METAL GATE WORK FUNCTION ENGINEERING FOR FUTURE CMOS TECHNOLOGY NODES

ENGENHARIA DA FUNÇÃO TRABALHO DE ELETRODO DE PORTA METÁLICOS PARA FUTUROS NÓS TECNOLÓGICOS DA TECNOLOGIA CMOS

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Coorientador: Prof. Dr. Stefan De Gendt

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"*Science without religion is lame, religion without science is blind.*"
Albert Einstein

"All truths are easy to understand once they are discovered; the point is to discover them."
Galileo Galilei

Dedico este trabalho à meus pais, Jovelino e Elizabeth,
à minha irmã, Luiza, meus avós, e
aan mijn geliefde Marije.

ABSTRACT

To improve the performance of CMOS (*Complementary Metal-Oxide-Semiconductor*) devices with technology nodes below 100 nm, high-k dielectrics had to be introduced. However, traditional poly-Si based gate electrodes are not compatible with high-k dielectrics and therefore also their replacement is required to continue the scaling of CMOS devices. Metal based electrodes have been employed on the traditional planar MOSFET (*Metal-Oxide-Semiconductor Field Effect Transistor*) gate structure comprising high-k gate dielectrics. Effective work function values between 4.15 eV and 4.45 eV indicate that the material is appropriate for nMOS applications, while materials with EWF values between 4.95 eV and 5.15 eV are adequate for pMOS applications. Titanium nitride (TiN) films became the material of choice as a gate metal for devices with technology nodes below 65nm. TiN effective work function (EWF) values have been reported to be suitable for CMOS technology. EWF values are related to the film composition and dipole variations at the interface between TiN layer and dielectric.

In this work, TiN layers were tested for their suitability for MOS devices for both technology, planar and 3-dimentional transistors, such as FinFET (*Fin Field Effect Transistor)*. Two different deposition methods were used for TiN deposition: physical vapor deposition (PVD) and atomic layer deposition (ALD). PVD TiN films can present EWF values adequate for both nMOS and pMOS. Unfortunately, conformal films on 3-D FinFET structures, which is the technology choice for next generation CMOS scaling, are not easily obtained by PVD processes. ALD provides the desired conformality, but ALD TiN layers have EWF values suitable for pMOS applications only. For ALD TiN, lower EWF values can be achieved by mixing Al with TiN layer.

PVD technique was used to obtain 20-nm-thick TiN layers, with electrical resistivity value of 324 μΩ.cm. Raman spectroscopy results indicated the presence of Ti and N vacancies in PVD TiN layers. Furthermore, XPS results showed oxygen incorporation into the TiN film surface, attributed to exposure of TiN film to ambient air. In order to reduce the oxygen contamination, an Al cap layer was deposited *in situ* on top of the PVD TiN film. It is important to highlight that in this case the Al layer is used to avoid TiN surface oxidation and not for EWF tuning. MOS capacitors (with $TiN/SiO_2/Si$ and $Al/TiN/SiO_2/Si$ structures) and Schottky diodes (with TiN/Si and Al/TiN/Si structures) were fabricated to evaluate the electrical characteristics of the PVD TiN. Ideality factors between 1.0 and 3.1, and work function between 4.45 eV and 4.55 eV were extracted from TiN/Si and Al/TiN/Si structures. The

spread in ideality factor values is attributed to Ti and N vacancies in the TiN films, but the oxygen incorporation can also influence the ideality factor values. The flat-band voltage, TiN EWF and effective charge density values extracted from MOS capacitors, were found to be between -0.18 and 0.04 V, 4.05 eV and 4.35 eV, and -10^{11} cm^{-2} and 10^{12} cm^{-2}, respectively. Changes in PVD TiN EWF and flat-band voltage values are related mainly to dipole variations at the TiN/SiO_2 interface. Furthermore, the investigation of effect of dipole variations ($q\Delta_{SiO2}$) at the TiN/SiO_2 interface, extracted using PVD TiN EWF values from MOS capacitors and Schottky diodes, has demonstrated that the $q\Delta_{SiO2}$ term is mainly affected by the TiN oxidation at the interface with dielectric.

ALD TiN presents pMOS EWF values, its work function values can be tuned by mixing Al into TiN layer; and therefore, nMOS EWF values can also be achieved. With this, titanium aluminum (TiAl), Al and aluminum nitride (AlN) layers were introduced between the high-k (HfO_2) dielectric and ALD TiN electrode as Al diffusion sources. The extracted ALD TiN EWF values from MOS capacitors had demonstrated that a decrease of 1.09 eV on TiN EWF can be achieved using TiAl as Al source. Furthermore, a decrease of 0.26 eV and 0.45 eV on ALD TiN EWF were extracted from AlN/TiN structures. Furthermore, the extracted TiN EWF values are suitable for applications on pMOS, nMOS and mid-gap devices, and the Al diffusion is a good method for TiN work function tuning. Moreover, the electrical characterization of FinFET devices had demonstrated that the obtained TiN layers are suitable for CMOS technology.

Also, this work contains the development and fabrication of the first FinFET device in Brazil. These devices were fabricated with with $Al/TiN/SiO_2/Si$ as gate structure and the electrical performance of these transistors demonstrated that Al/TiN stack is suitable for nMOS applications.

Keywords: *Metal gate work function engineering, TiN, FinFET, PVD, ALD, Al diffusion.*

RESUMO

Para melhorar o desempenho dos dispositivos CMOS (*Complementary Metal-Oxide-Semiconductor*) com nós tecnológicos inferiores a 100 nm, dielétricos com alta constante dielétrica k (high-k ou alto-k) foram introduzidos. Eletrodos de porta tradicionais baseados em poli-Si não são compatíveis com dielétricos com alto-k e, portanto, a sua substituição é necessária para continuar o escalamento dos dispositivos CMOS. Eletrodos metálicos têm sido empregados em estruturas de porta de dispositivos tradicionais MOSFET (*Metal-Oxide-Semiconductor Field Effect Transistor*) planares, juntamente com dielétricos de alto-k. Filmes de nitreto de titânio (TiN) são utilizados como eletrodos de porta em dispositivos com tecnologia inferior à 65 nm. Valores da função trabalho eficaz (EWF) de filmes de TiN têm sido reportados como adequados para a tecnologia CMOS. Filmes com função trabalho eficaz com valores entre 4,15 eV e 4,45 eV são apropriados para aplicações em dispositivos nMOS, enquanto materiais com valores de EWF entre 4,95 eV e 5,15 eV são adequados para aplicações em dispositivos pMOS. Os valores de EWF estão relacionados com a composição do filme e variações de dipolo na interface entre a camada de TiN e o dielétrico. Neste trabalho, os filmes de TiN foram utilizados em dispositivos MOS, planares e FinFET (*Fin Field Effect Transistor*). Dois métodos de deposição foram utilizados para obtenção dos filmes de TiN: PVD (*physical vapor deposition*) e ALD (*atomic layer deposition*). Filme de TiN depositados por PVD podem apresentar valores de função trabalho adequados para dispositivos nMOS e pMOS. Infelizmente, filmes conformais em estruturas FinFET tri-dimensionais, que é a tecnologia escolhida para a próxima geração de dispositivos CMOS, não são facilmente obtidos através de processos PVD. Por outro lado, processos ALD fornecem a conformalidade desejada, mas filmes de TiN obtidos por ALD apresentam valores de função trabalho compatíveis somente com dispositivos pMOS. Contudo, valores mais baixos de EWF podem ser obtidos *misturando* Al com os filmes de TiN.

Filmes de TiN com 20 nm de espessura foram obtidos através de PVD, e apresentaram um valor de resistividade elétrica de 324 μΩ.cm. Resultados da espectroscopia Raman indicam a presença de vacâncias de Ti e N nos filmes de TiN depositados por PVD. Além disso, análises XPS mostram a incorporação de oxigênio na superfície dos filmes de TiN, que está relacionado com a exposição do filme de TiN ao ambiente. A fim de reduzir essa contaminação superficial de oxigênio, uma camada de Al foi depositada in-situ no topo dos filmes de TiN. É importante ressaltar que este filme de Al foi utilizado somente para evitar a oxidação superficial dos filmes de TiN e não para modificação da

função trabalho do TiN. Capacitores MOS (com estruturas Al/TiN/SiO_2/Si e TiN/SiO_2/Si) e diodos Schotkky (com estruturas Al/TiN/Si e TiN/Si) foram fabricados para o estudo das características elétricas dos filmes de TiN. Os valores de fator de idealidade entre 1,0 e 3,1 e EWF entre 4,45 eV e 4,55 eV foram extraídos das estruturas Al/TiN/Si e TiN/Si. Vacâncias de Ti e N presentes nos filmes de TiN afetam os valores extraídos para o fator de idealidade, mas a oxidação superficial dos filmes de TiN também podem influenciar os valores do fator de idealidade. Valores de tensão de banda plana entre -0,18 V e 0,04 V, TiN EWF entre 4,05 eV e 4,35 eV, e densidade de carga efetiva entre -10^{11} cm^{-2} e 10^{12} cm^{-2}, foram extraídos dos capacitores MOS. Mudanças nos valores da tensão de banda plana e função trabalho do TiN estão relacionados principalmente com as variações de dipolo na interface entre TiN e SiO_2. Além disso, o estudo sobre o efeito das variações de dipolo ($q\Delta_{SiO2}$) na interface TiN/SiO_2, os valores de EWF extraídos dos capacitores MOS e diodos Schottky, demonstraram que o termo $q\Delta_{SiO2}$ é principalmente influenciado pela oxidação dos filmes de TiN na interface com o SiO_2. Filmes de TiN depositados por ALD apresentam valores de EWF compatíveis com tecnologia pMOS, contudo, o valor da função trabalho pode ser modificada para valores adequados à tecnologia nMOS, através da incorporação de Al nos filmes de TiN. Com isso, filmes de Al, TiAl e AlN foram introduzidos entre os dielétrico de alto-k (HfO_2) e eletrodo de TiN (obtido por ALD), para serem utilizados como fonte para à difusão de Al. Os valores de EWF extraídos dos capacitores MOS com filmes de TiN depositados por ALD, demonstraram uma diminuição de até 1,09 eV no valor da função trabalho efetiva do TiN quando uma camada de TiAl foi utilizada como fonte para a difusão de Al. Além do mais, reduções de 0,26 eV e 0,45 eV foram observadas nos valores de EWF do TiN para estruturas de AlN/TiN. Além disso, os valores de função trabalho efetiva extraídos para os filmes de TiN são adequados para tecnologia pMOS, *mid-gap* e nMOS, e a difusão de Al é um método promissor para o ajuste da função trabalho do TiN. Contudo, a caracterização elétrica dos dispositivos FinFET demonstraram que os filmes de TiN utilizados neste trabalho são compatíveis e adequados para a tecnologia CMOS. Além disso, este trabalho contém o desenvolvimento e fabricação do primeiro dispositivo FinFET no Brasil. Estes dispositivos foram fabricados com a estrutura de porta Al/TiN/SiO_2/Si, e as características elétricas destes dispositivos demonstraram que a estrutura Al/TiN é apropriada para aplicações da tecnologia nMOS.

Palavras-chave: *Engenharia da função trabalho do metal, TiN, FinFET, PVD, ALD, Difusão de Al.*

ABSTRACT

Om de prestaties van CMOS-transistoren (*Complementary Metal-Oxide-Semiconductor*) voor toekomstige technologie noden te verbeteren, werden hoge-k diëlektrica ingevoerd. Omdat traditionele poly-Si gebaseerde poortelektroden niet compatibel zijn met hoge-k diëlektrica is ook hun vervanging noodzakelijk om de schaling van CMOS-transistoren voort te zetten. Metaalelektroden zijn gebruikt voor traditionele vlakke MOSFET-poortstructuren (*Metal-Oxide-Semiconductor Field Effect Transistor*) met hoge-k gate diëlektrica. Titanium nitride (TiN) films werden geselecteerd als het materiaal bij uitstek als poort metaal voor transistoren in de 65nm technologie node. TiN effectieve werkfunctiewaarden (EWF) zijn geschikt voor CMOS-technologie. Effectieve werkfunctiewaarden tussen 4.15 eV en 4.45 eV geven aan dat het materiaal geschikt is voor nMOS toepassingen, terwijl materialen met EWF-waarden tussen 4,95 eV en 5.15 eV geschikt zijn voor pMOS-toepassingen. EWF-waarden zijn afhankelijk van de electrode samenstelling en dipool variaties op de interfase tussen TiN lagen en diëlektrica.

In dit werk werden TiN-lagen getest op hun geschiktheid voor MOS-transistoren, in vlakke of 3D (*FinFET - Fin Field Effect Transistor*) technologie. Twee verschillende depositiemethoden werden gebruikt voor TiN-depositie: fysische damp depositie (*physical vapour deposition PVD*) en atoom laag depositie (*atomic layer deposition ALD*). PVD TiN films kunnen EWF-waarden leveren die voldoende zijn voor zowel nMOS en pMOS. Helaas zijn conforme films op 3-D FinFET-structuren, die de technologische keuze zijn voor de volgende generatie CMOS-schaling, niet gemakkelijk te verkrijgen door PVD-processen. ALD verschaft de gewenste conformaliteit, maar ALD TiN-lagen hebben EWF-waarden die alleen geschikt zijn voor pMOS-toepassingen. Met ALD TiN kunnen lagere EWF waarden worden bereikt door Al- met TiN-lagen te mengen.

De PVD-techniek werd gebruikt om 20-nm dikke TiN-lagen te deponeren met een typische elektrische weerstandswaarde van enkele honderden μΩ.cm. Ramanspectroscopie toonde de aanwezigheid van Ti en N vacancies in PVD TiN-lagen aan. Bovendien toonden XPS resultaten zuurstof aanwezigheid op het TiN filmoppervlak, toegeschreven aan blootstelling van TiN film aan omgevingslucht. Om zuurstof verontreiniging te verminderen, werd een Al-deklaag in situ gedeponeerd op de PVD TiN film. Het is belangrijk te benadrukken dat in dit geval de Al laag wordt gebruikt om TiN oxidatie te voorkomen en niet voor EWF tuning. MOS capaciteten (met TiN/SiO_2/Si en Al/TiN/SiO_2/Si-structuren) en Schottky diodes (met TiN/Si en Al/TiN/Si structuren) werden

gefabriceerd om de elektrische eigenschappen van de PVD TiN te evalueren. Idealiteit factoren tussen 1.0 en 3.1, en werkfunctie tussen 4.45 eV en 4.55 eV werden geëxtraheerd uit TiN/Si en Al/TiN/Si structuren. De spreiding in idealiteit factor waarden wordt toegeschreven aan Ti en N vacatures in de TiN films, maar de zuurstofopname kan ook invloed hebben op de idealiteit factor waarden. De vlakke band spanning, TiN EWF en effectieve ladingsdichtheid waarden gehaald uit MOS capaciteten bleken respectievelijk tussen -0.18 en 0.04 V, 4.05 eV en 4.35 eV en -10^{11} cm^{-2} en 10^{12} cm^{-2} te liggen. Veranderingen in PVD TiN EWF en vlakke band spanningswaarden hebben voornamelijk betrekking op dipool variaties aan de TiN/SiO_2 interfase. Voorts heeft het onderzoek van het effect van dipool variaties ($q\Delta_{SiO2}$) op de TiN/SiO_2 interfase, geëxtraheerd met PVD TiN EWF waarden van MOS-capaciteten en Schottky diodes, aangetoond dat de term $q\Delta_{SiO2}$ voornamelijk wordt beïnvloed door de TiN oxidatie bij het grensvlak met SiO_2. ALD TiN resulteert in pMOS EWF waarden, bovendien kunnen de werkfunctiewaarden worden afgestemd door Al in TiN-lagen te mengen, en daarom kunnen nMOS EWF waarden worden bereikt. Teneinde dit te onderzoeken werden titanium aluminium (TiAl), Al en aluminium nitride (AlN) lagen ingevoerd tussen het hoge-k (HfO_2) diëlektrium en ALD TiN elektrode als Al diffusiebronnen. De geëxtraheerde ALD TiN EWF waarden van MOS-capaciteten hadden aangetoond dat een verlaging van 1.09 eV TiN EWF kan worden bereikt met behulp van Al. Bovendien werd een vermindering van 0.26 eV en 0.45 eV vastgesteld voor ALD TiN EWF in AlN/TiN structuren. Hierdoor zijn de geëxtraheerde TiN EWF waarden geschikt voor toepassingen met PMOS, NMOS en mid-gap noden, en de Al diffusie is een goede methode voor de TiN werkfunctie tuning. Bovendien heeft de elektrische karakterisering van FinFET-transistoren aangetoond dat de verkregen TiN-lagen geschikt zijn voor CMOS-technologie.

Ook bevat dit werk de ontwikkeling en fabricage van de eerste FinFET-transistor in Brazilië. Deze transistoren werden gefabriceerd met $Al/TiN/SiO_2/Si$ als poort structuur en de elektrische evaluatie van deze transistors toonden aan dat Al/TiN stack geschikt is voor nMOS toepassingen.

Trefwoorden: Metaal poort werkfunctie engineering, TiN, FinFET, PVD, ALD, Al diffusie.

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Lucas Petersen Barbosa Lima

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS AND SYMBOLS

ALD – Atomic layer deposition

BOX – Buried oxide

C-V – Capacitance-voltage measurements

CMOS – Complementary metal-oxide-semiconductor

C_{oxinv} – Gate oxide capacitance per unit area

CVD – Chemical vapor deposition

ECR – Electron cyclotron resonance

EDS – Energy dispersive X-ray spectroscopy

E_{GSi} – The width of Silicon's forbidden band

ε_0 – Vacuum dielectric constant

ε_{Si} – Silicon dielectric constant

EWF – Effective work function

ϕ_F – Semiconductor Fermi potential

ϕ_{MS} – Difference between the work function of the gate electrode material and substrate

FinFET – *Fin* field effect transistor

FIB – Focused ion beam

FGA – Forming gas annealing

GIS – Gas injection system

I-V – Current-voltage measurements

I_{DS} – Drain-source current

$I_{DS}xV_{DS}$ – Drain-source current by drain-source voltage measurements

$I_{DS}xV_{GS}$ – Drain-source current by gate-source voltage measurements

I_{off} – Transistor off current

JL – Junctionless transistor

L – Channel length

μ – Charge-carrier effective mobility

MOS – Metal-oxide-semiconductor

MOSFET – Metal-oxide-semiconductor field effect transistor

$N_{A,D}$ – Substrate net doping

PVD – Physical vapor deposition

Q_0/q – Effective charge density

RIE – Reactive ion etching

RTA – Rapid thermal annealing

SEM – Scanning electron microscopy

SIMS – Secondary ion mass spectroscopy

SiNW – Silicon nanowire

SOI – Silicon-On-Insulator

SS – Sub-threshold slope

V_D – Drain voltage

V_{FB} – Flat-band voltage

V_G – Gate voltage

V_T – Threshold voltage

XRR – X-ray reflection spectroscopy

XPS – X-ray photoelectron spectroscopy

W – Channel width

CHAPTER 1

INTRODUCTION

1.1 Objectives

This work is focusing on the development and characterization of TiN films for metal gate applications for sub-100 nm CMOS (*Complementary Metal Oxide Semiconductor*) technology nodes. To enhance the device performance, it is important to have appropriate metal electrode work function values; for nMOS and pMOS applications the desired value ranges from 4.1 – 4.5 eV and 4.9 – 5.1 eV, respectively. The control of effective work function (EWF) value of TiN is essential to tune the threshold voltage and therefore, improve the CMOS device performance. The TiN film properties (such as resistivity, composition, dipoles, metal work function) are known to affect the electrical characteristics of this metal layer. Since these properties are most likely interdependent, an alternative and reliable work function extraction method is needed in order to study the influence of TiN film properties on the metal work function value.

Traditional methods to extract the gate metal work function are based on capacitance-voltage (C-V) measurements of MOS (*metal oxide semiconductor*) capacitors with different thickness of

gate dielectric and different electrode areas, which can incorporate different charge densities at the dielectric/semiconductor interface. This can induce an additional error in the work function extraction. This work presents an alternative method for work function extraction. Our method is based on current-voltage (I-V) and C-V measurements on Schottky diode and MOS capacitors, respectively, fabricated on the same substrate. The first advantage of our method is that we are extracting the same parameter with two different methods. The second advantage is that both devices were fabricated on the same substrate, which can reduce the defect incorporation on Si surface. Thus, with one substrate, it is possible to extract the work function with two different measurements. Hence, this method was used to study the influence of TiN film composition and dipole at metal/dielectric interface on TiN EWF for metal layer obtained by physical vapor deposition (PVD).

In addition, different TiN EWF values can be achieved by doping this metal layer with different elements, such as Al and N. In this sense, this work also presents the study of the Al doping influence on TiN EWF by MOS capacitors. For those devices, the dielectric (HfO_2), metal electrode (TiN) and Al source (such as AlN, TiAl and Al layers) were obtained by atomic layer deposition (ALD) and PVD. Thus, the Al doping can be an important method for TiN EWF control.

The third and last goal of this work is the development and fabrication of a FinFET device using TiN as a metal gate electrode. This resulted in the fabrication of the first entire FinFET using Brazilian facilities only.

1.2 Motivation

1.2.1 Scaling of MOS devices

Switching speed and power consumption are the main reasons for the scaling of CMOS devices, although cost reduction and complexity are also associated with decrease of the

dimensions of those devices. The power dissipation is related to the switching frequency (clock), device capacitance and power supply. In addition, the device's switching speed is related to the amount of charge delivered at the gate of a MOS device, and this charge is usually delivered via source-drain current (I_{DS}) from another MOS device. So, the performance of a MOSFET (metal-oxide-semiconductor field effective transistor) device (schematic view is presented in Figure 1) is related to I_{DS} value, which is related with the gate channel dimensions (W: width and L: length), charge-carrier effective mobility (μ), gate applied voltage (V_G), drain applied voltage (V_D), threshold voltage (V_T) and the gate oxide capacitance per unit area (C_{oxinv}). The drain-source current can be expressed as [1,2]:

$$I_{DS} = \frac{W}{L}\mu C_{oxinv}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \quad (1)$$

When $V_{D,sat} = V_G - V_T$ (saturation or active mode), equation 1 can be written as:

$$I_{DS,sat} = \frac{W}{L}\mu C_{oxinv}\frac{(V_G - V_T)^2}{2} \quad (2)$$

With this, the device performance can be enhanced by an increase on the effective charge-carrier mobility (μ); this can be obtained using strained silicon method, i.e. SiGe channels (as shown in Table 1). Also, a decrease in threshold voltage (V_T) values can improve the device performance. Besides an increase of $I_{DS,sat}$ the transistor switches on faster. Disadvantage is the sub-threshold leakage or the transistor off current (I_{OFF}). This value sets the limits on the reduction of V_T values. Furthermore, drain-source current can be increased by shrinking down the channel length (L), which is possible to achieve with smaller gate transistors and three-dimensional devices (such as FinFET), as presented in Table 1. In addition, the use of high-k material as gate dielectric increases the gate oxide capacitance and so, the MOSFET performance can be improved. Thus, with the implementation of high-k based dielectrics, the replacement of poly Si based electrodes is mandatory to enhance the device performance, as previously discussed. Low electrical resistivity

values, thermal stability, compatible with high temperature processes, chemical etching resistance and compatibility with high-k dielectrics and MOS technology are some requirements for the materials to replace the poly-Si based electrodes [3-16]. Additionally, in order to enhance the device performance, adequate effective work function (EWF) values, both for pMOS and nMOS applications, are desirable properties for metal gate materials.

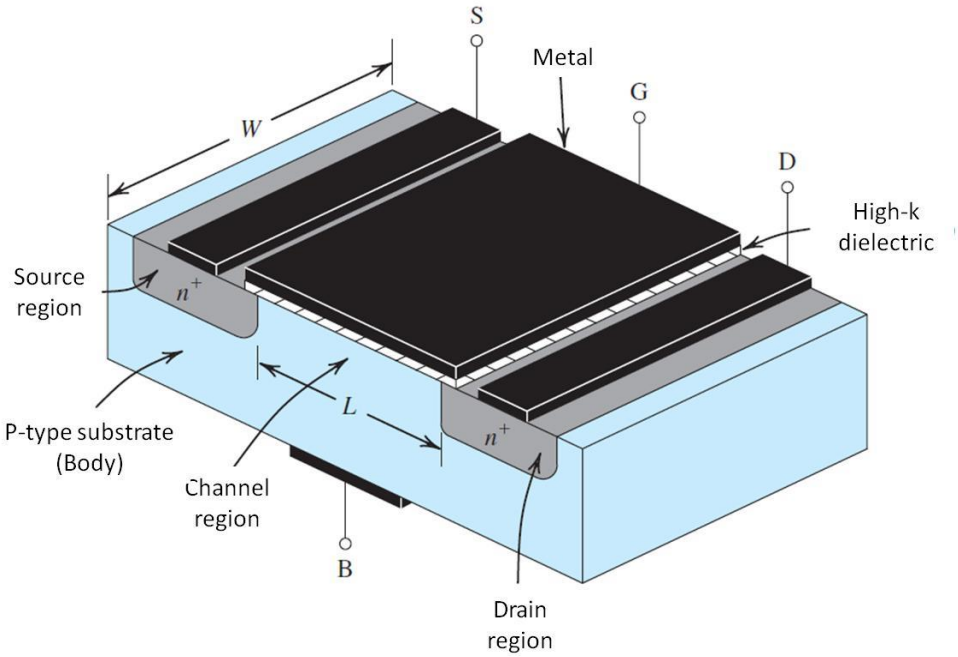
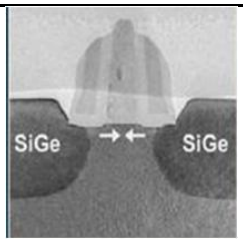
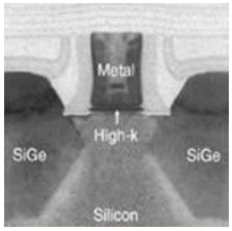
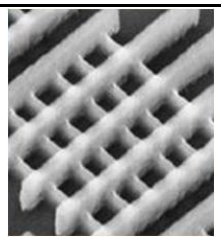


Figure 1 – Schematic view of a conventional MOSFET – extracted from reference 2.

Table 1 - MOS technology scaling.[*]

Technology node	90 nm – 65 nm	45 nm – 32 nm	22 nm and below

[*] *Adapted from: Intel: "22nm-Announcement Presentation". (2011)*

MOSFET Structure			
	SiGe technology	Gate-Last	Tri-Gate
	Strained Silicon	Strained Silicon with High-K and Metal Gate	Strained Silicon and High-K/Metal Ga te with 3D gate

1.2.2 High-K dielectrics and poly-Si based electrodes

High-k dielectrics and metal gate electrodes have been introduced for complementary metal oxide semiconductor (CMOS) devices with technology nodes below 100 nm, as shown in Table 1 [3-6]. Materials with high dielectric constant (called high-k dielectrics) have been used as a gate dielectric on complementary metal oxide semiconductor (CMOS) devices with technology nodes below 100 nm [3-6]. In order to enhance the MOS device performance, the capacitance scaling is needed to increase the source-drain current when the device is in the “on” state, while avoiding small current leakage when the device is in the “off” state. This can be achieved by reducing the gate dielectric thickness. Unfortunately, the scaling of conventional SiO_2 as gate dielectric results in excessive leakage current tunneling through the gate dielectric. So, the employment of high-k dielectric reduces the leakage tunneling current, and therefore, the MOS device performance is increased. Due to the high relative dielectric constant (k) of ~20 and other beneficial properties in the compatibility with CMOS technology, hafnium oxide (HfO_2) has been extensively used as a high-k dielectric on MOS devices. However, this dielectric has a low quality interface with poly Si based gate electrodes, due to their poor adhesion and the defects at this interface [7].

Additionally, poly Si electrodes suffer from poly-depletion effects, which, consequently, decreases the gate capacitance and drain-source current (I_{DS}), and increases the threshold voltage (V_T) on MOS device, as presented in Figure 2 [1]. So, replacement of poly Si based electrodes is needed to improve the device performance. Moreover, section 1.3 discusses the impact of the work function on CMOS devices.

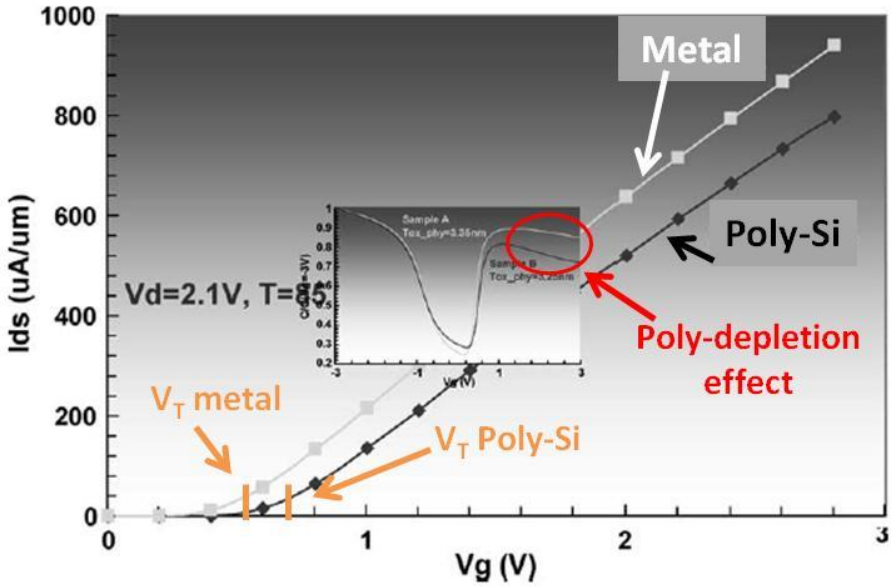


Figure 2 – I_{DS} – V_{GS} and C-V measurements of MOSFET devices with poly-Si and metal gate based electrodes – extracted from reference 7.

1.3 Appropriate Work Function Values

As shown in Figure 3, work function values between 4.95 eV and 5.15 eV are suitable for pMOS application, while values around 4.15 eV and 4.45 eV are compatible with nMOS devices.

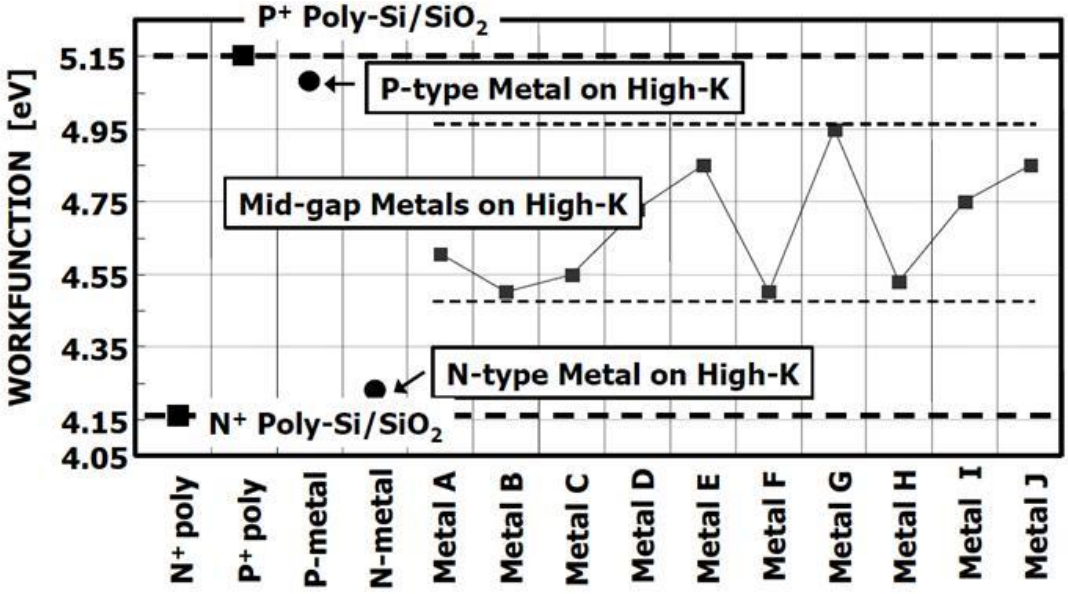


Figure 3 – Work function values appropriated for pMOS, nMOS and mid-gap application – extracted from reference 8.

If the density of charges trapped in the interface between dielectric and substrate is neglected, the effective charge density (Q_0/q) in MOS structures can be written as function of the flat-band voltage (V_{FB}) and the difference between the work function of the gate electrode material and substrate (ϕ_{MS}):

$$\frac{Q_0}{q} = (V_{FB} - \phi_{MS})\frac{C_{oxinv}}{qA} \quad (3)$$

Where q = $1.6\text{x}10^{-19}$C, A is the gate area [9,10]. Also, the ϕ_{MS} can be expressed as:

$$q\phi_{MS} = W_F - \left(X_{Si} + \frac{E_{GSi}}{2} \pm \phi_F\right) \quad (4)$$

Where X_{Si} = 4.05 eV, E_{GSi} is the width of Silicon's forbidden band (E_{GSi} = 1.12 eV), ϕ_F is the semiconductor Fermi potential and W_F is the work function value of metal electrode.

The threshold voltage (V_T) can be defined as the voltage value where the channel region is formed. That point is given by formula (5).

$$V_T = V_{FB} \pm 2\phi_F \pm \left(\frac{A}{C_{oxinv}}\right)\sqrt{Aq\varepsilon_0\varepsilon_{Si}N_{A,D}\phi_F} \quad (5)$$

Where $N_{A,D}$ is the substrate net doping, ε_0 is vacuum dielectric constant and ε_{Si} is silicon dielectric constant. So, for MOSFET if the gate voltage (V_G) value exceeds the V_T value (which is higher than zero for nMOS and lower than zero for pMOS) the channel region is formed and the device starts to conduct (on state). Therefore, low threshold voltage values are desirable, otherwise higher V_G values will be needed for switching the MOS device (turn on). From equation (5) it is possible to conclude that V_T is related to V_{FB} value. In order to minimize the effective charge density on MOS structure (given by equation 3), the V_{FB} and ϕ_{MS} difference must be approximately zero, then [9]:

$$\frac{Q_0}{q} \to 0 \Rightarrow (V_{FB} - \phi_{MS}) \to 0 \Rightarrow V_{FB} = \phi_{MS} \quad (6)$$

This equation is valid for small effective charge density values, lower than 10^{10} cm^{-2}, and at flat band condition [9]. From equations (5) and (6) the following can be derived:

$$V_T = \phi_{MS} \pm 2\phi_F \pm \alpha \quad (7)$$

Where $\alpha = \left(\frac{A}{C_{oxinv}}\right)\sqrt{Aq\varepsilon_0\varepsilon_{Si}N_{A,D}\phi_F}$. So, from equation (7) it is possible to see that V_T is proportional to ϕ_{MS}. Considering the metal work function values presented in Figure 3, it is possible to estimate the ϕ_{MS} values for pMOS, nMOS and mid-gap applications as demonstrated in Table 2.

Table 2 – Estimation of V_T values for pMOS, nMOS and mig-gap application.

For pMOS applications	For nMOS applications	For Mid-gap applications
From eq. (4) **and** W_{FpMOS}**=4.1eV** $q\phi_{MSpMOS} = 0.55eV - \phi_F$ **From eq.** (7)**:** $V_{TpMOS} = 0.55eV - \phi_F - \alpha$	**From eq.** (4) **and** W_{FnMOS}**=5.2eV** $q\phi_{MSnMOS} = -0.55eV - \phi_F$ **From eq.** (7)**:** $V_{TnMOS} = -0.55eV + \phi_F + \alpha$	**From eq.** (4) **and** $W_{Fmidgap}$**=4.65eV** $q\phi_{MSmidgap} = \mp\phi_F$ **From eq.** (7)**:** $V_{TpMOS} = \pm\phi_F \pm \alpha$

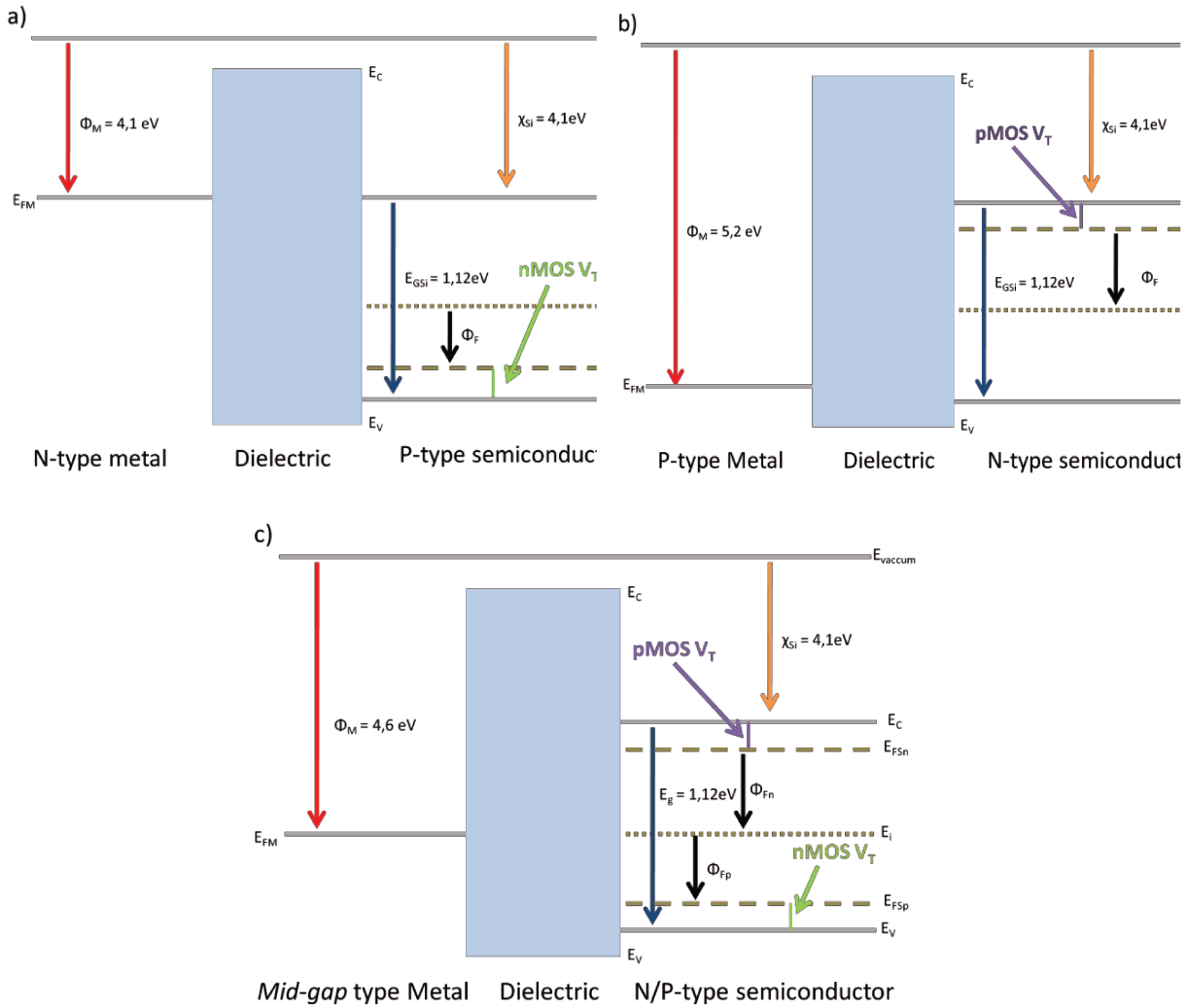


Figure 4 – Energy band diagrams for MOS structures with metal electrodes for a) nMOS, b) pMOS and c) mid-gap applications. Those diagrams shows the idealized case and no interaction between metal and semiconductor were considered.

In the past, ion implantation procedure for source and drain formation was done with the poly-Si gate electrode already formed (gate first method). With this, the poly-Si gates were implanted as well, shifting the Fermi level in the poly-Si, obtaining appropriate work function values for pMOS or nMOS applications. Since the poly-Si as gate electrode has been replaced by metal materials, work function modulation cannot be obtained by the method of implantation.

Nowadays, the substrate net doping ($N_{A,D}$) is between 10^{18} cm^{-3} and 10^{19} cm^{-3}, and consequently the semiconductor Fermi level (ϕ_F) is approximately 0.5 V [20]. So, V_T values between 0.1V and 0.2V can be achieved for substrate net doping around 10^{18} cm^{-3}, even for nMOS or pMOS metal gate electrodes [20]. However, for mid-gap electrodes, V_T values around 0.5 V and 0.8 V can be expected, which results in less leakage current, but slower devices. So, it is necessary to adjust the channel doping to decrease the V_T for values near 0.1V and 0.2V. Nevertheless, fewer lithography and etching steps are needed during the device fabrication process using mid-gap electrodes, because the same electrode will be used for pMOS and nMOS transistors; and consequently, those devices are easier to fabricate [20].

For high switching speed, low V_T is required, implicating that CMOS technology has to rely on two types of gate metals, each with an appropriate work function. The first order approach towards the choice of material is the work function of the metal as such. This is generally defined as the energy needed to extract electrons from the material. In the case of a gate capacitor, band bending is causing shifts of this value [21-24]. In addition, the effect of dipole variations on the interface between the metal gate electrode and high-k dielectric ($\Delta_{MG/HK}$), due to chemical reactions between those two materials, must be considered. As defined by T.W. Hickmott, the dipole layer in a dielectric film is basically: *"a sheet of positive charge of density σ/cm^2 separated by a distance t from a sheet of negative charge of equal magnitude*" [22]. Furthermore, no

additional net charges are introduced to the metal-dielectric interface. However, this effect influences V_{FB} and W_F values and consequently, the V_T value. Moreover, additional dipole term is needed to be considered due to the chemical reactions between the high-k dielectric and substrate ($\Delta_{HK/semiconductor}$) [23,24]. Figure 5 presents a schematic of different dipole moments for two interfaces: SiO_2/Si, HfO_2/Si and La_2O_3/Si [23]. For the SiO_2/Si interface, there is no resultant dipole moment, since the bonding Si-O presents the same dipole magnitude (see Figure 5) [23]. However, for HfO_2/Si and La_2O_3/Si interfaces a residual dipole moment arises from the difference between the Hf-O-Si and La-O-Si bonds, respectively, resulting in an additional dipole moment [23].

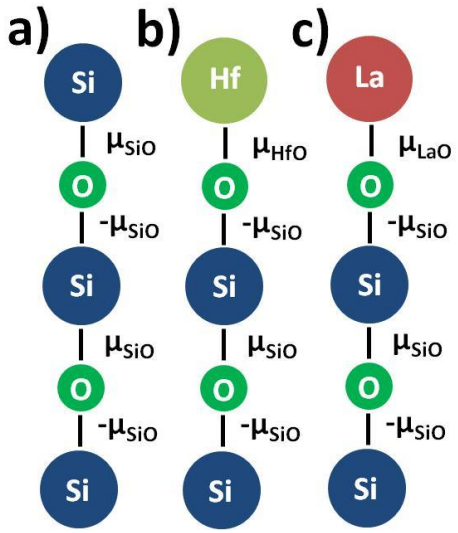


Figure 5 – Schematic of different dipole moments (represented by μ) for a) SiO_2/Si, b) HfO_2/Si and c) La_2O_3/Si interfaces.

So, re-writing equation (3) with the dipole terms (combined with equation (4)):

$$V_{FB} = \left(\frac{Q_0 A}{C_{oxinv}} + X_{Si} + \frac{E_{GSi}}{2} \pm \phi_b\right) - W_F + q\Delta_{MG/HK} + q\Delta_{HK/semiconductor} \qquad (8)$$

In this context, the effect of dipole variations terms (presented above) must be considered for a correct estimation of the metal gate work function value. Since this value will deviate from the original definition (the energy needed to extract an electron from the free metal), one refers to this

value as the effective work function (EWF). Literature reports that variations on metal EWF values around ±0.2 eV can be expected due the dipole variations on MOS structure [19,23,24]. Also, positive values for V_{FB} and negative effective charge densities can be achieved due the dipole effects [23,24]. So, considering the dipole effects, the challenge is to adjust the metal EWF, V_{FB} and V_T for appropriate values regarding the technology node and application.

1.3.1 Thermal budget: Gate First and Gate Last Processing

Basically, there are two different methods for CMOS transistors fabrication: gate first and gate last. The gate first approach is based on the formation of the gate structure, meaning gate dielectric and electrode, before the construction of source and drain. Figure 6a describes the gate first process flow for a CMOS device. The gate structure comprises that the high-k dielectric and metal gate electrode are prepared before the source/drain formation. Usually, the source and drain regions are prepared using ion implantation method, followed by a high temperature annealing for dopant activation. So, it is mandatory that the gate structure (especially the metal gate) supports high temperature processes.

The gate last method (or replacement gate) is based on the formation of a "dummy" gate structure for source/drain construction (Figure 6b). So, a sacrificial gate structure is defined before the drain and source formation. Then, drain/source formation can be done, even using high temperature, using the "dummy" gate structure. Typically, only the metal gate layer is used as sacrificial layer, since most of the dielectric layers are suitable for high temperature processes. After the formation of source and drain regions, the sacrificial gate structure is removed and replaced by a new gate structure. By this way, the metal gate electrode is not exposed to high temperatures processes.

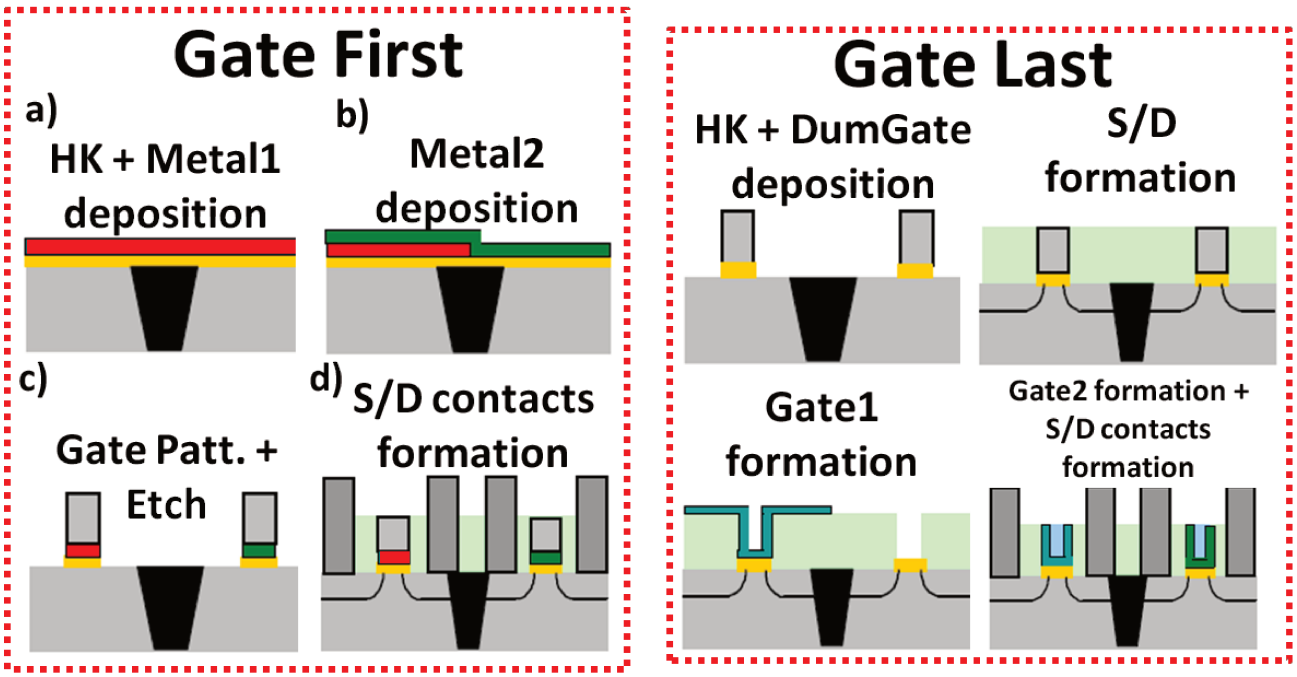


Figure 6 – Gate first and last processes flow. For gate first: a) high-k and n-type metal electrode depositions; b) p-type metal electrode deposition; c) gate patterning and etching – definition of both gate structures; d) formation source and drain and contacts depositions. For gate last: e) definition of the dummy/sacrificial gate structure; f) source and drain formation; g) formation of nMOS gate structure (after the removal of sacrificial gate structure); h) formation of pMOS gate structure and source/drain contacts deposition.

Although the gate first technology presents reduced complexity and cost, the semiconductor industry is currently using gate last technology, because the implemented gate structure (high-k and metal gate) does not keep the thermal stability during high temperature processes. As a result, additional dipoles and/or chemical reactions can occur during the high temperature processes and often the EWF is shifted towards mid-gap. So, it is desirable to use a metal gate electrode with good thermal stability with high-k dielectrics and a low thermal budget once the gate metals are deposited.

1.4 Titanium Nitride as a Promising Metal Gate Electrode

Some materials and compounds, such as titanium nitride (TiN) and tantalum nitride (TaN), appeared as promising candidates for metal gate electrodes on CMOS devices. Due to thermo dynamical stability with HfO_2, conductivity, wear resistance, favorable melting point and appropriate work function value, TiN has been widely studied and used as a gate metal electrode on CMOS technology [3-5,12-14,29-34]. Chemical vapor deposition (CVD), physical vapor deposition (PVD) and atomic layer deposition (ALD) have been frequently used for TiN layers deposition. The knowledge of each deposition process is essential to achieve TiN layers with desirable properties, and so, it is important to understand and control the process parameters during the deposition procedure [12,25,30]. Literature reports that stoichometric TiN films present pMOS work function values [25,30]. However, TiN effective work function values can be adjusted for nMOS, pMOS or mid-gap applications by changing the chemical composition of the metal film. Nitrogen-rich TiN layers present work function suitable for pMOS applications, while nMOS work function values can be achieved with Ti-rich films [25,30].

In this work, two different systems were used for TiN deposition: Sputtering (which is PVD) and ALD. The deposition process of two techniques will be discussed in chapter 2. Different TiN composition and phase can be obtained by Sputtering process; however, ALD metal layer usually presents stoichiometric formation [31-33].

1.4.1 TiN Work Function Tuning

Titanium nitride (TiN) effective work function values for films deposited by ALD have been frequently reported as suitable for pMOS applications, however, literature also reports TiN as a

mid-gap work function material and even for nMOS applications [3-5,12,14-19,25-27,35]. On the other hand, for employments on nMOS devices, the challenge is to obtain a gate electrode material with sufficient low EWF with an equivalent toughness as TiN. Physical and electrical properties of TiN films are highly related to film composition [12,25-27,30]. In addition, due the requirement of conformal layers for 3D channel structures, such as FinFET's and tri-gate transistors, ALD system is commonly being used for TiN deposition [3-5]. Furthermore, TiN films obtained by ALD typically have a stoichiometric composition according to their crystallographic phase, and consequently, the EWF values of these films are between 4.7 eV and 5.1 eV, which is suitable for pMOS technology. Solutions for the nMOS EWF in the range of 4.1 – 4.4 eV can be obtained by doping the TiN film with different elements (such as Al and N) [5,25,36,37]. Literature reports significantly change of EWF by addition of Al ions into TiN layer [5,38-40]. Moreover, the metal gate EWF shift can be related to formation of different dipoles at the interface between metal gate and high-k due to Al diffusion (see Figure 7) [5,21-25,37]. The Al incorporation into TiN film could result in additional dipole formation at the interface between the TiN and HfO_2 layers [25]. Figure 7b shows the band alignment in a HfO_2/TiN interface. $E_{vac,m}$ is the vacuum reference and E_F is the Fermi level of the TiN. $E_{vac,o}$ is vacuum level, CBM is the conduction band minimum, VBM is the valence band maximum, E_g is the band gap of the HfO_2. The valence band offset (VBO) is the energy difference between the TiN Fermi level and the HfO_2 VBM. The dipole moment influence of the defect-free and defected HfO_2/TiN interface, and induced dipole moment (for example by Al presence at the interface) is represented by the resultant dipole moment D_x at the HfO_2/TiN interface. Φ is the vacuum work function of defect-free TiN free surface, and Φ_{eff} is the effective work function of TiN deposited on top of the HfO_2. The Φ_{eff} can be expressed as [25]:

$$\Phi_{eff} = \Phi + \frac{4\pi D_x}{A} \qquad (9)$$

Where A is the area of the dipole interface. In general, the adsorption of an atom changes the resultant dipole moment magnitude, due to its electronegativity value, and therefore, modifies the EWF value. The Al presence at the HfO_2/TiN interface decreases the interface dipole moment magnitude due to Al electronegativity value [25]. Therefore, the TiN EWF is reduced with Al presence at the HfO_2/TiN interface [25].

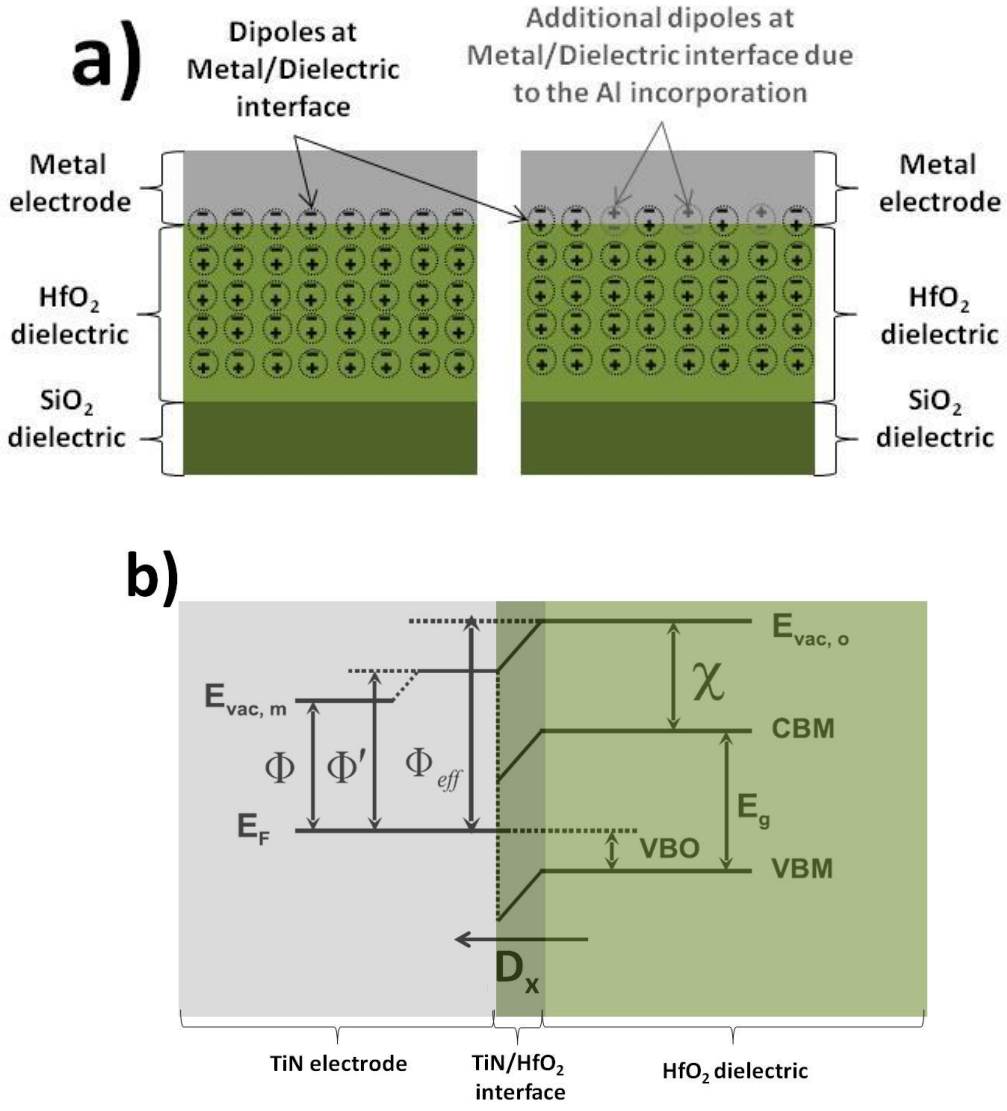


Figure 7 – a) Diagram of additional dipole formation due to Al incorporation; b) Schematic band diagram in a HfO_2/TiN interface – adapted from reference 25.

In this context, the metal gate work function shift is induced by annealing TiN with Al on top and leads to a decrease of 0.60 eV on TiN EWF. This effect is attributed to the diffusion of Al into TiN [25,37]. Also, the Al diffusion technique for lowering the metal gate EWF deviates from the "*gate last*" method due to high temperatures (more than 400ºC) process for Al diffusion [35,37,43,44]. In this sense, the Al diffusion is often used for a *"gate first*" approach. Aluminum and TiAl films have been used as an Al diffusion source for tuning the metal gate electrode work function [5,38-40]. Alternatively, the usage of AlN to control the metal gate EWF has been reported as a promising approach for work function engineering for CMOS technology [35,43,44]. In addition, it is known that an HfO_2/AlN stack is thermally stable at high temperatures [46]. Furthermore, the metal gate EWF is highly dependent on the AlN structure and composition [47]; stoichiometric AlN is dielectric and it could increase the resistance. Low metal gate EWF values can be expected with an increase of Al concentration in AlN layers, and high metal gate EWF can be achieved by increasing the amount of N in the AlN layer [47,48]. Aluminum nitride films are usually obtained by PVD and ALD depositions [47-49]. So, Al incorporation into TiN film is a promising method to adjust the TiN work function [37].

1.4.2 TiN as Metal Gate Electrode for 3D devices

FinFET and 3D MOSFET devices recently have gained much attention in micro- and nano-technology industries. The basic advantage of using a FinFET device is reduced short-channel effects and high output resistance values [50]. Figure 8 shows a schematic view of traditional planar MOSFET and FinFET (3D device). The gate of FinFET devices consist of a thin piece of Si semiconductor (also called *fin*) and then, the top and side wall of this *fin* are used to control the channel; and consequently, a better control of the channel current flow is achieved. So, the drain-source current (I_{DS}) is around three times higher on 3D devices than in conventional planar

MOSFET, due to side wall conduction. Another advantage of a good channel current control is the reduction on the short channel effects (SCE). Figure 9 shows the channel length modulation (CLM), which is mainly related to the width of the depletion layer at the drain region in a MOSFET device. As a result, the channel length is decreased and drain current is increased, respectively. Moreover, SCE influences the threshold voltage (V_T) and it can be expressed as follow:

$$V_{TSCE} = V_{T0} - \left\{[f(C_{ox}, N_A, \phi_F, \varepsilon_{Si})]\frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)\right]\right\} \quad (10)$$

Where x_{dD} is the depth of depletion region of drain, x_{dS} is the depth of depletion region of source, x_j is the drain/source well depth and L is the channel length. Table 3 presents some effects related to the SCE. Those effects are related to the decrease on the channel length (L) dimension on a MOSFET and consequently, different values for I_{DS} and V_T can be expected due those short channel effects (SCE). Therefore, lowering the short channel effects will improve the device performance.

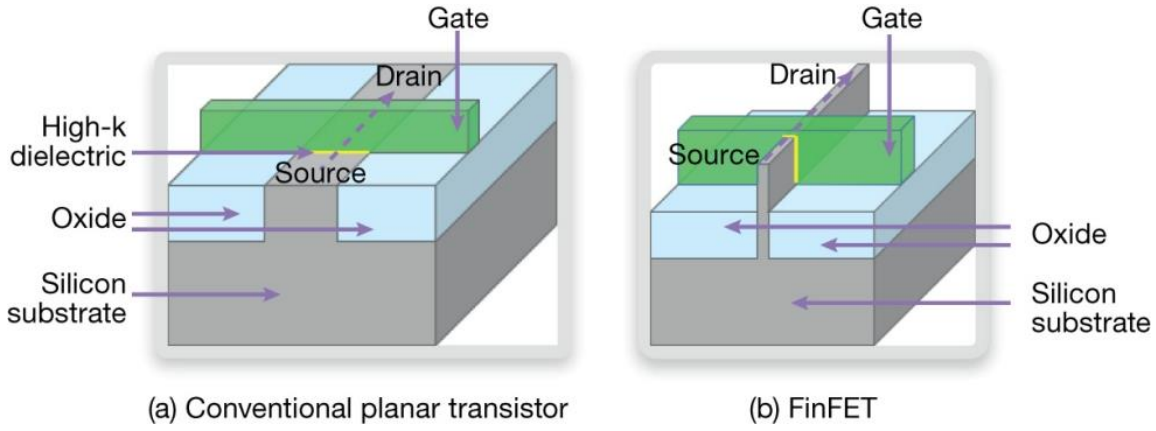


Figure 8 – Planar MOSFET and FinFET (3D device).

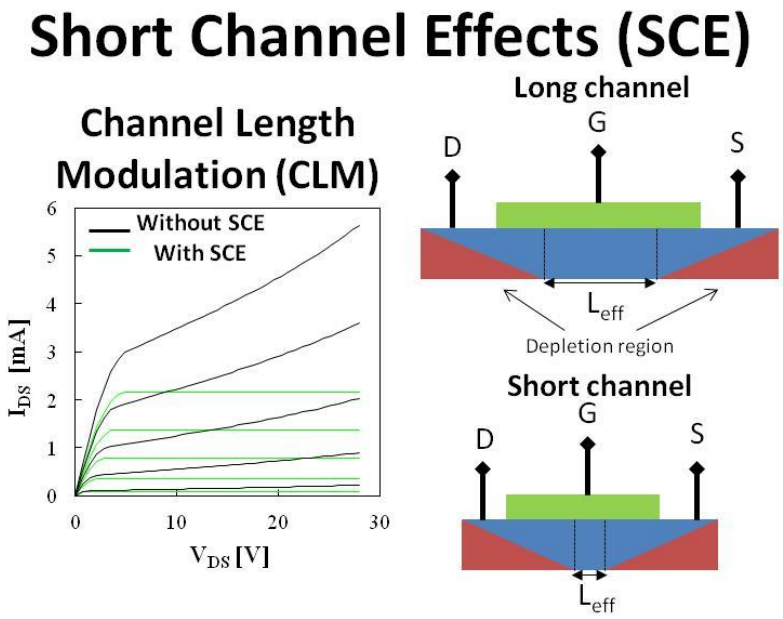


Figure 9 – Short channel effects (SCE) on MOSFET devices. The influence of channel length modulation on I_{ds} x V_{ds} characteristics is shown.

Table 3 – Examples of effect related to the SCE on MOSFET devices.

Effect	**Consequence**
Punchthrough is the depletion layer formed by the overlap of drain and source depletion layers.	A drastically increase on I_{DS} with V_{DS}, leads to a gain on output conductance.
The V_{DS} effect on the output conductance and V_T is related to the the drain induced barrier lowering (DIBL).	A reduction on the effective channel length (L_{eff}) – by CLM – results on changes in V_T value (due to the increase on I_{DS} value).
The increase of sub-threshold current (related to the carrier induction through the channel before the strong inversion) is one effect of short L_{eff} devices.	For short L_{eff} devices, the sub-threshold current increases the DIBL effect and consequently, increases the carrier injection from the source to drain (hard to *turn off* the devices).

Nowadays, high-k dielectric and metal gate electrodes are employed on FinFET devices (as shown in Table 1). Literature reports the usage of TiN films as metal gate electrodes for 3D devices [3-6,12-15]. In addition, when compared to planar MOSFET, FinFET-based devices require smaller effective work function (EWF) shifts (approximately 200 meV) from mid-gap for low V_T

applications [5,51] The classical model for V_T is valid for wide *fins* and high doping level (equation 7), but for narrow *fin* and low doping level the V_T is expressed as [51] :

$$V_T = \phi_{MS} + 2\phi_F + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{inv} \quad ; \quad Q_D = q\frac{1}{2}W_{fin}N_a \tag{11}$$

Where Q_{SS} is the charges in the gate dielectric, C_{ox} is the gate capacitance, ϕ_F is the Fermi potential, ϕ_{MS} is the work function difference between the semiconductor and gate electrode [51]. Basically, V_{inv} is the additional surface potential to $2\phi_F$, that is needed to bring enough inversion charge into the channel for the transistor to reach the threshold condition [51]. Also, V_{inv} is a function of *fin* width and doping concentration [51]. Additionally, the Q_D is negligible for low doping concentrations. Furthermore, high performance CMOS devices require low V_T value and two work function metal gate structures: for N-channel: EWF ≈ 200 meV below mid-gap; and for P-channel: EWF ≈ 200 meV above mid-gap. For low power CMOS a single work function metal gate structure is needed and consequently, symmetrical V_T values are achieved (for both N-channel/P-channel: EWF ≈ 350 meV below/above mid-gap). Moreover, for low doping concentration, the V_T is mainly determined by the EWF of the gate stack.

Ultimately, the goal is to apply the knowledge on EWF tuning of TiN into FinFET devices. Therefore, besides the investigation on EWF tuning of TiN, the aim of this thesis was to realize a FinFET device which can be applied as a test platform for further demonstration of V_T tuning by EWF modulation of TiN. As previously mentioned (see section 1.1), this resulted in the fabrication of the first FinFET device fabricated entirely in Brazil. Several fabrication processes were developed to allow this device construction. Figure 10 shows the time-line for both the development of TiN gate metal and the Brazilian FinFET device, which resulted in the integration of both approaches. To evaluate the electrical properties of silicon nanowire (Si NW), used as *fin* structure later on FinFET devices, Junctionless (JL) transistors were fabricated using focused ion

beam (FIB) milling process. Electrical characterization of JL devices were carried out to investigate the SiNW electrical properties. Furthermore, the development of TiN metal gate structure was done simultaneously with the SiNW study. The TiN metal gate structure was obtained by PVD. Raman spectroscopy, XPS and 4 probe measurements were taken to characterize the metal gate electrode structure. In addition, MOS capacitor and Schottky diodes were fabricated to study the electrical behavior of the metal gate stack. Moreover, the FinFET device was fabricated employing the developed TiN-based metal gate structure and SiNW processes. The *fin* width was defined using dry etching (using RIE) and Si milling (using FIB system). The FinFET gate structure was composed by SiO_2 and Al/TiN (obtained by PVD) stack as gate dielectric and electrode, respectively.

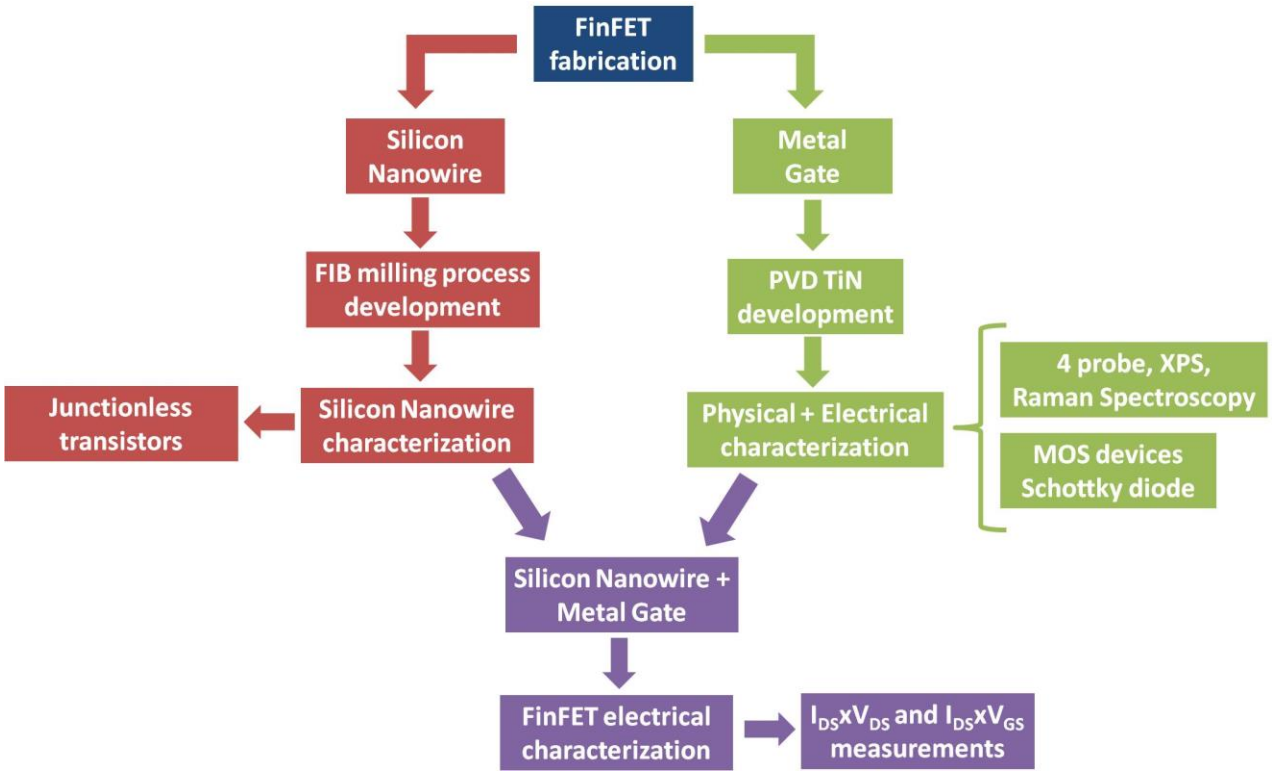


Figure 10 – FinFET fabrication: simultaneously development of metal gate and SiNW structures.

As discussed in section 1.4.1, the TiN EWF can be tuned using Al incorporation into this metal layer. In this work, the Al diffusion influence into TiN layer was investigated using MOS capacitors with high-k dielectric (HfO_2 layer). Figure 11 shows a schematic of the process flow for this study. Different TiN/AlN, TiN/TiAl and TiN/AlN laminate structures (obtained by ALD) were used to evaluate the effect of Al incorporation on TiN film. XRR measurements were done to extract the layers thicknesses, and the Al diffusion profile was investigated using XPS and SIMS measurements. The TiN EWF value was evaluated from electrical measurements of MOS capacitors.

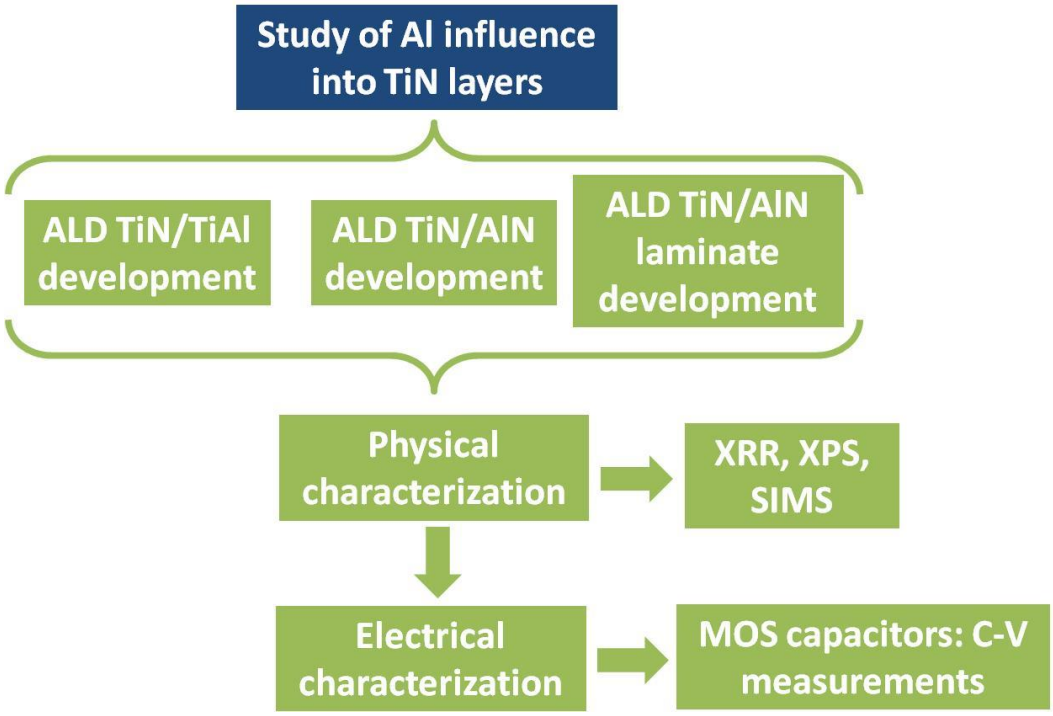


Figure 11 – Schematic for the study of Al influence on TiN EWF value.

1.5 Thesis Outline

This thesis is organized as follow.

Chapter 2 reviews the TiN ALD and PVD deposition techniques. A brief comparison between the physical and electrical properties of TiN obtained by ALD and PVD process are also presented in this chapter.

Chapter 3 describes the development of silicon nanowire (SiNW) using focused ion beam (FIB) system for Si milling. The Brazilian applied process flow for 3-dimentional devices (such as FinFET and Junctionless) fabrication is explained in this chapter. In addition, section 3.3 describes the experimental procedure for the TiN and Al/TiN film structures obtained by *sputtering* deposition (PVD) at University of Campinas - Unicamp (Campinas, Brazil). Moreover, section 3.4 presents the development of TiN/AlN and TiN/AlN laminate structures obtained by ALD system at Interuniversity Microelectronics Centre - IMEC (Leuven, Belgium). Also, the fabrication steps for MOS capacitors and Schottky diodes construction are also presented in this chapter.

Chapter 4 presents the SiNW characterization using Junctionless transistors. Also this chapter presents the study of electrical performance of the fabricated FinFET device (with TiN as metal gate electrode). In addition, the physical and electrical characterizations of TiN, Al/TiN, TiN/AlN film structures are also presented in this chapter. Film composition, electrical resistivity and thickness were extracted from TiN layers using Raman spectroscopy, XPS, SIMS, XRR and four-probe techniques. Electrical properties (such as work function) were extracted from MOS capacitors and Schottky diodes and evaluated with TiN physical characteristic.

Finally, chapter 5 presents the main conclusions from this work, and an outlook on possible future developments is given.

CHAPTER 2

TiN DEPOSITION TECHNIQUES AND PROPERTIES

2.1 Introduction

Titanium nitride (TiN) films can be obtained by several deposition methods, such as: atomic layer deposition (ALD), chemical vapor deposition (CVD) and sputtering (physical vapor deposition - PVD). A brief description of ALD and sputtering deposition methods and TiN properties will be introduced in this chapter.

2.2 Atomic Layer Deposition (ALD)

The atomic layer deposition is derived from chemical vapor deposition (CVD) [52-56]. Basically, one of the differences between those two techniques is how the reactants are inserted in the deposition chamber and therefore, resulting in different chemical reactions processes. In general, the reactants are continuously inserted in CVD chamber and the chemical reactions might happen on the substrate surface or in the gas phase [52-57]. On the other hand, the reactants are sequentially inserted in ALD chamber, usually divided into four steps composing an ALD cycle

[52-57]. With this, in ALD processes the precursors reactions occur on the substrate surface and the gas phase reactions are negligible [52-57].

The ALD method allows the layer-by-layer deposition and the process is done step-by-step using gas precursor pulses (short pulses between milliseconds and seconds). This deposition technique is widely used for binary oxide and nitride compound deposition, such as TiN and HfO_2, however, two different gas precursors are needed. For ALD in which a single element is deposited, two precursors are needed, one to deliver the element and a second one to remove the ligand of the delivering molecule (reduction process). Additionally pure element layer (such as W) and ternary (i.e. $HfSiO_x$) compounds can be also obtained by ALD method. Furthermore, as previously mentioned, the chemical reactions in the vapor phase are minimized when the gas precursors are pulsed and sequentially injected, repeated by a purge with inert gas, maximizing the chemical reactions near the substrate surface [52-56].

A schematic of ALD process is presented in Figure 12. Figure 12a shows the first gas precursor pulse inside the ALD chamber. The gas precursor will be chemisorbed at the substrate surface, meaning that the reactant is absorbed and forms a chemical bond with the surface atoms of the substrate [52-56]. However, the chemical reactions between the substrate and gas precursors are dependent on the number of available sites on the substrate surface [52-56]. After the first gas precursor pulse, a purge step is carried out to remove reaction residue and precursor that is not absorbed on the substrate surface (Figure 12b). Then, a pulse of second gas precursor is done, and so, a chemical reaction with the first precursor on the surface can occur, which consequently creates a thin layer on the top of the substrate surface (Figure 12c). Since the amount of first precursor on the surface is limited, this reaction is saturating. Afterwards, a purge step is done to remove the precursor and reaction products again (Figure 12d). Thus, at the end of these 4 steps,

also called the first cycle, a thin layer composed from the two precursors is formed on top of the substrate surface. The number of cycles determines the film thickness. In this way, ALD technique provides a layer-by-layer deposition with an excellent control on film thickness even for high aspect ratio structures, step coverage and, due to the fact that precursors are saturatively reacted, conformality all over the substrate surface area [52-56]. Furthermore, another advantage of ALD method is the possibility of mixing oxides and nanolaminates layers [52-56]. In spite of that some disadvantages of ALD method are low deposition rate, difficulty to change the film stoichiometry and the limitation of materials since not all the elements presented on the periodic table are available as ALD precursors [52-56]. Moreover, since the gas precursors are composed by molecules with the desired element and ligands, some ligand contamination can be expected on the deposited layer (for example: ALD TiN layers can contain small concentrations of Cl, H or C, provided by the gas precursor). However, plasma-enhanced ALD (PEALD) technique can increase the deposition rate and the film quality.

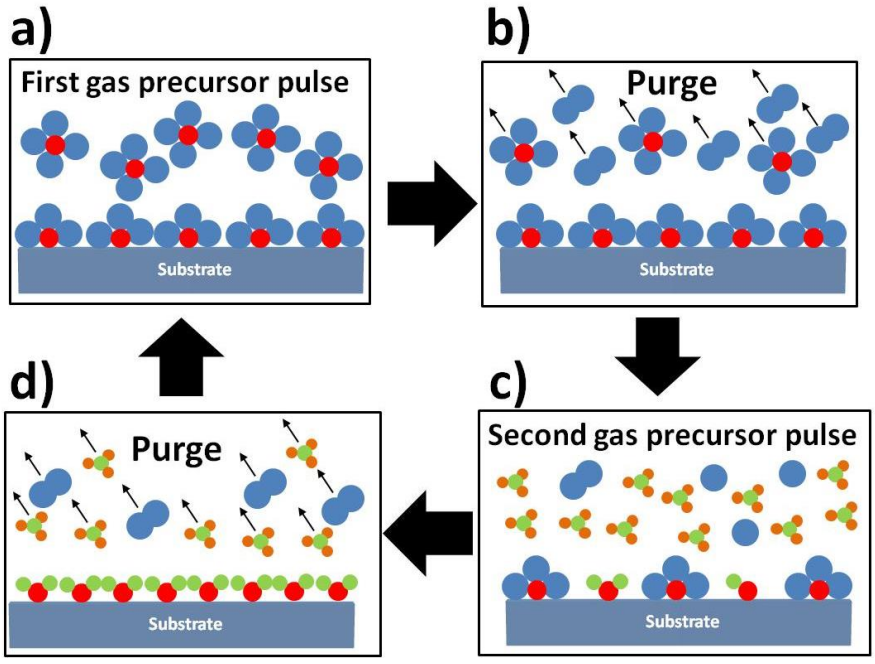


Figure 12 – Schematic of ALD process.

Hafnium oxide (HfO_2), hafnium oxynitride (HfON), hafnium silicate ($HfSiO_2$), aluminum oxide (Al_2O_3), aluminum nitride (AlN) and zirconium oxide (ZrO_2) are some examples of dielectric layers that can be obtained by ALD method. For AlN and Al_2O_3 depositions, TMA (*TriMethylAluminium* – $Al(CH_3)_3$) is commonly used as first gas precursor combined with NH_3 pulses or N_2 plasma; and with N_2 plasma combined with O_2 or H_2O, respectively. TEMAHf (*Tetrakis[EthylMethylAmino]Hafnium* – $Hf[(C_2H_5)(CH_3)N]_4$) and $HfCl_4$ are usually used as first gas precursor for HfO_2 depositions, combined with H_2O or O_3 pulses. Furthermore, metal layers such as titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), copper (Cu), tungsten (W) and ruthenium (Ru), can also be obtained by ALD method. *Tetrakis(dimethylamino)titanium* (TDMAT – $Ti[N(CH_3)_2]_4$) and $TiCl_4$ are often used as first gas precursor for TiN depositions, while $TaCl_5$ is suitable for TaN depositions.

As an example, the surface reactions of an ALD process using $TiCl_4$ and NH_3 as first and second precursors, respectively, is presented in Figure 12. The ideal surface reactions will occur between the gas precursor and the available sites on the substrate surface, meaning that $TiCl_4$ will react with the substrate surface sites [52-56]. Considering that the substrate is a SiO_2 layer, which presents surface sites mainly composed by hydroxyl groups (OH^-) related to the H_2O absorption due to air exposure [52-56]. So, during the first gas precursor pulse, the $TiCl_4$ will react with the hydroxyl groups as follows [52-56]:

$$-OH + TiCl_4 \rightarrow -OTiCl_3 + HCl \quad (12)$$

Thus, the nucleation regime is dependent on the density of available -OH at the SiO_2 surface [52-56]. The reaction is finalized when all the available -OH sites have reacted with $TiCl_4$ [52-56]. As a result, the reaction products are the HCl gas and the SiO_2 surface termination changes from -OH to $-TiCl_3$ groups [52-56]. In addition, the formation of $–TiCl_3$ groups on the SiO_2 surface

reduce and stops the $TiCl_4$ reaction with SiO_2 layer [52-56]. Then, the excess of gas precursor, meaning non-reacted $TiCl_4$, and HCl product are removed during the purge step. Then, the second gas precursor is inserted in the ALD chamber and the reaction between $-TiCl_3$ and NH_3 can occur as follows [52-56] :

$$-TiCl_3 + NH_3 \rightarrow TiNH_2 + HCl \quad (13)$$

As as result, this reaction generates Ti-N bonds and the surface is now with -NH groups [52]. Furthermore, the reaction of NH_3 with the layer surface is dependent on the amount of -TiCl [52-56]. In addition, the resultant layer presents now -NH groups at the surface and these groups prevents further reactions with NH_3 [52-56]. The excess of NH_3 and HCl product are removed during the purge step. During the next ALD cycle, the $TiCl_4$ will react with the H-terminated sites on the layer surface [52-56].

Another example is the ALD TiN layers reported in reference 43. Those films were obtained using cycles of gas precursors $TiCl_4$ and N_2/H_2. First, two consecutive $TiCl_4$ pulses (40 milliseconds each pulse) were done inside the ALD chamber, followed by a 10 seconds N_2/H_2 pulse (gas flow: 68 sccm and N_2/H_2 ratio: 1:8). In this work, TMA and NH_3 pulses were used for AlN deposition; while TiN layers were obtained using $TiCl_4$ and NH_3 pulses at 400ºC. More details about the experimental flow used in this work for ALD processes will be given in section 3.4. Physical and electrical properties of the deposited layers are related to film composition. In general, films obtained by ALD present stoichometric composition. Some film properties of TiN layers obtained by ALD will be presented in section 2.4.

2.3 Sputtering (Physical Vapor Deposition – PVD)

A schematic of a DC sputtering deposition process is presented in Figure 13. First of all, high energy Ar^+ ions inside the PVD chamber hit the target surface (made from the desirable material)

as shown in Figure 13a and Figure 13b. Then, with the impact of these Ar^+ ions, some target atoms are ejected from the material surface and some electrons as well (Figure 13c). The sputtered target atoms are directed towards the substrate surface and then, a layer on the top of the substrate is grown (Figure 13d). The released electrons can collide with Ar atoms creating, therefore, more Ar^+ ions. Argon gas (noble material and inert gas) is commonly used for plasma generation inside the PVD chamber. In addition, the sputtering depositions are usually done at room temperature, but literature reports some depositions with temperatures around 400ºC. Moreover, magnetic field can be used to increase the efficiency of target sputtering process. This technique is called *Magnetron sputtering*. Also, it is possible to engage a DC (direct current) or RF (radio-frequency) power supply to assist the deposition process. Furthermore, other gases, such as nitrogen (N_2) and oxygen (O_2), can be inserted inside the sputtering chamber (*reactive sputtering* method), and as a result the obtained layer will be a compound of the target material and the reactive plasma gases.

Sputtering systems have been widely used for metal layer depositions, but it also has been employed for dielectrics deposition. Aluminum (Al), aluminum alloys, titanium (Ti), titanium nitride (TiN), platinum (Pt), gold (Au), tungsten (W), tungsten alloys, tantalum (Ta) and tantalum nitride (TaN) can be obtained by sputtering deposition. For example, reference 41 reports a TiN films obtained by DC reactive magnetron sputtering in N_2/Ar (gas flow: N_2: 17 sccm and Ar: 100 sccm) with DC power of 800 W. Additionally, RF reactive sputtering system allows the deposition of dielectric layers, such as SiO_2 and SiN. In this PhD work, a titanium target (with purity around 99.95%) and N_2/Ar ambient was used for TiN film reactive sputtering deposition; and the process flow will be discussed in section 3.3.

As previously mentioned, physical and electrical properties of the deposited layer is highly related to film composition. So, a good control of gas flow (Ar and N_2) is needed to manage the

TiN properties. As an example, literature reports that nitrogen-rich TiN films are suitable for pMOS applications, while titanium-rich TiN layers are appropriate for nMOS devices [25,30].

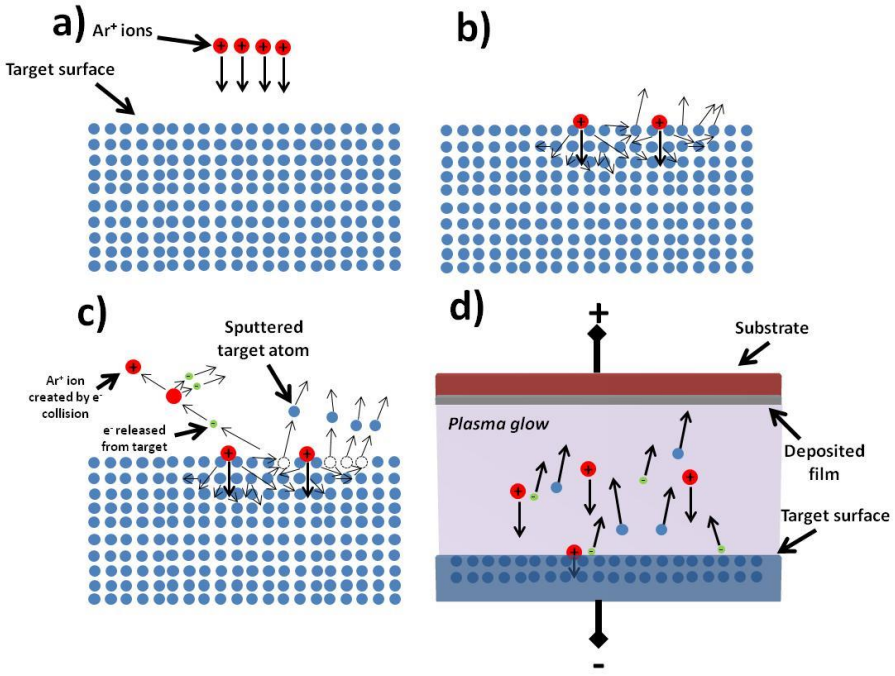


Figure 13 – Schematic of a DC sputtering process.

2.4 TiN Physical and Electrical Properties

In summary, TiN films can be obtained by ALD and PVD methods. With physical vapor deposition method, thicker layers can be obtained, but the growth rate and film conformality can be limited by mass transport of gases inside the plasma glow. On the other hand, atomic layer deposition allows the formation of a thin layer (thickness controlled by number of cycles) with good conformality on the substrate surface, but changing the film composition is not easily done just like for sputtering depositions and film contamination can occur due to ligands from the precursor (such as presence of H or Cl into ALD TiN films).

Literature reports different TiN electrical properties for films obtained by ALD and PVD, shown in Table 4. As an example, for a 5-nm-thick TiN layer obtained by ALD process presented

work function values between 4.8 eV and 5.0 eV were reported [43]. On the other hand, TiN work function values between 4.3 eV and 5.2 eV films can be achieved using sputtering deposition [41].

Table 4 – ALD versus PVD TiN properties.

Film property	**ALD**[34,38,39,40]	**PVD**[39,41]
Electrical resistance	**230 – 275 μΩ.cm**	**210 – 1210 μΩ.cm**
Thickness	**1.7 – 30 nm**	**100 – 1250 nm**
TiN work function	**4.7 – 5.1 eV**	**4.3 – 5.2 eV**

As previously mentioned, sputtering method allows the deposition of TiN layers with different chemical composition, for example, Ti-rich or N-rich films, and therefore, TiN work function can be adjusted for nMOS, pMOS and mid-gap values. Titanium nitride films obtained by ALD usually present stoichometric formation and pMOS work function values. Thus, additional methods are required for ALD TiN work function adjustment for nMOS and mid-gap values. In this PhD work, Al diffusion technique was used to adjust the TiN effective work function value for mid-gap and nMOS values.

CHAPTER 3

EXPERIMENTAL PROCEDURE

3.1 Introduction

Titanium nitride (TiN) films were obtained by atomic layer deposition (ALD) and DC reactive magnetron sputtering processes. An ULVAC ICOT9000 DC Magnetron Sputtering system was used for Al and PVD TiN depositions, while an ASM Polygon 8300 system was used for HfO_2, AlN and ALD TiN. Test samples were prepared for physical characterization of both PVD and ALD TiN layers. N-type FinFET, MOS capacitors and Schottky diodes were fabricated with these metal layers as upper electrode to study the electrical properties of both PVD and ALD TiN films. The process deposition parameters, fabrication steps and characterization methods will be presented in this chapter.

3.2 Fabrication of 3D devices

3.2.1 Introduction

The FinFET device presented in this PhD thesis is the first FinFET fabricated entirely in Brazil; therefore, some experimental procedures were developed for this transistor fabrication. The study and comprehension of Si nanowire (SiNW) properties were necessary before the FinFET

construction, since the SiNW would be used as gate MESA structure. The SiNW structures were prepared using UV lithography, Reactive Ion Etching (RIE) and Focused Ion Beam (FIB) Si milling.

FIB system has been used for sample preparation in transmission electron microscopy (TEM) and also for micro and nanofabrication as application in circuit editing and prototype nanomachining [80-82]. One advantage of using FIB system is that it does not require lithography for milling (for example, Si milling) and has nanometric resolution [83]. Although, some surface damage or ion incorporation on substrate surface can occur due to Ga^+ FIB, which leads to changes on substrate optical and electrical properties [84,85]. However, this effect is desirable in some cases and FIB system can be also used for ion implantation [86-93].

To study the SiNW electrical properties, Junctionless (JL) transistors were fabricated using FIB system and with this, the effect of Ga^+ incorporation and damage on SiNW structures could also be evaluated. JL devices have gained much attention of microelectronics industry, because it is compatible with CMOS technology and can be useful for 3D devices [77,78]. Also, these devices present low leakage current, good subthreshold slope, and, at high temperature, present high mobility and little diffusion of impurities [77,78]. E-beam lithography [78], UV lithography [77], reactive ion etching (RIE) and inductively coupled plasma (ICP) [79] have been used for JL device fabrication.

In this PhD work, nMOS and pMOS JL devices were fabricated using FIB system for SiNW definition, gate dielectric and gate, drain and source electrodes. Afterwards, nMOS FinFET devices were fabricated using Al/TiN/SiO_2/Si as gate structure.

3.2.2 pMOS Junctionless devices fabrication†

Figure 14 show the fabrication steps of pMOS JL devices, which were fabricated on SOI wafers (samples 1, 2, 3 and 4). The SOI samples presented 340 nm-thick of top (100) Si layer (active region), with electrical resistivity between 1 and 10 Ω.cm, and 400 nm-thick SiO_2 buried oxide (BOX) layer. Those samples were cleaned with a standard cleaning (see Table 5). 150 nm Al layers were deposited by DC sputtering, using argon flow of 60 sccm and power of 1000W on four SOI substrates. The substrate doping was achieved by the diffusion of those Al layers. For Al diffusion, four different processes were done on SOI samples, as shown in Table 6. The silicon nanowire structure was defined by Ga+ ion milling using a FIB system, and this tool was also used for SiO_2 gate dielectric and Pt gate, source and drain electrodes of pMOS JL devices. Then, a forming gas anneal (FGA – 8% H_2 and 92%N_2) was performed on JL transistors at 450ºC for 5 and 10 minutes. Drain-source current versus drain-source voltage (I_{ds} x V_{ds}) measurements were carried out to characterize of JL devices.

†[103]L.P.B. Lima, M.V.P. dos Santos, F.H. Cioldin, J.A. Diniz, I. Doi, J. Godoy Fo, ECS Trans., 49, p. 367 (2012).

Table 5 – Standard cleaning steps.

Cleaning solution	Temperature and Time	Purpose
H_2SO_4/H_2O_2 (4:1)	@ 80ºC for 10 minutes	Organic compounds removal
18MΩ.cm H_2O DI rinse	@ RT* for 1 minute	Residual solution removal
HF/H_2O (1:10)	@ RT* for 10 seconds	Native SiO_2 removal
18MΩ.cm H_2O DI rinse	@ RT* for 1 minute	Residual solution removal
$NH_4OH/H_2O_2/H_2O$ (1:1:5)	@ 80ºC for 10 minutes	Organic compounds and metal alloys (from IB and IIIB groups on periodic table) removal
18MΩ.cm H_2O DI rinse	@ RT* for 1 minute	Residual solution removal
$HCl/H_2O_2/H_2O$ (1:1:5)	@ 80ºC for 10 minutes	Alkaline ions and Fe, Al and Mg alloys removal
18MΩ.cm H_2O DI rinse	@ RT* for 1 minute	Residual solution removal
HF/H_2O (1:10)	@ RT* for 10 seconds	Residual oxide removal
18MΩ.cm H_2O DI rinse	@ RT*‡ for 1 minute	Residual solution removal

Table 6 – Al diffusion processes of JL devices.

Sample	First Step – N_2 anneal @ 450ºC	Second Step – residual Al removal using H_3PO_4 and HNO_3	Third Step – N_2 anneal
1	60 min		30 min @ 1000ºC
2	60 min		30 min @ 800ºC
3	30 min		30 min @ 1000ºC
4	30 min		30 min @ 800ºC

* RT – room temperature.

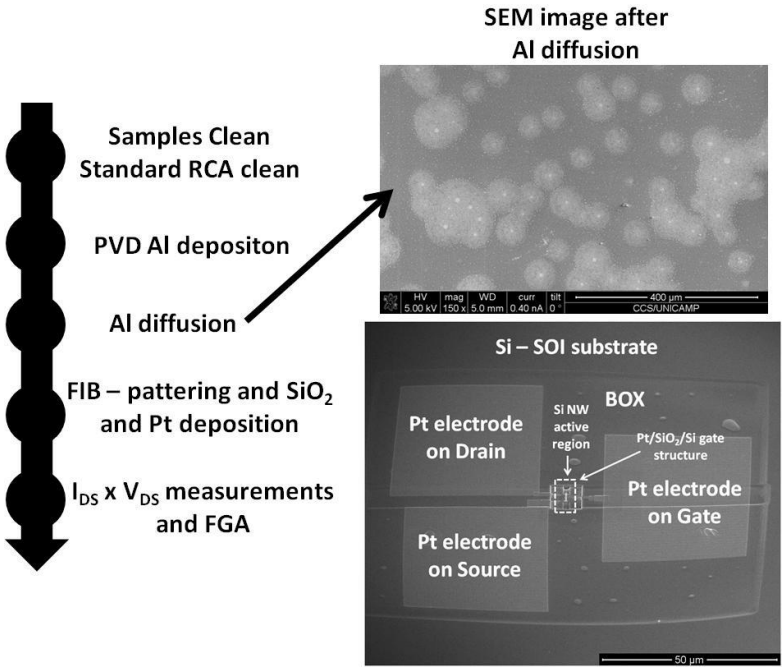


Figure 14 – Schematic for pMOS JL fabrication.[103]

3.2.3 nMOS Junctionless devices fabrication[§]

Silicon-On-Insulator (SOI) wafers were used for JL fabrication. The SOI samples presented 340 nm-thick of top (100) Si layer (active region), with electrical resistivity between 1 and 10 Ω.cm, and 400 nm-thick SiO_2 buried oxide (BOX) layer. The samples were cleaned with standard cleaning (see Table 5). To achieve the sample doping, phosphorus ions were implanted on SOI samples, with dose of 10^{16} cm^{-3} and ion energy of 30 keV (Figure 15-I). After this, rapid thermal annealing (RTA) was applied to induce the activation of dopant and to get n^+ active region with dopant concentration higher than 10^{19} cm^{-3}. A 600 nm thick SiO_2 layer was grown on top of Si layer by wet thermal oxidation in order to thin the Si layer down. Next, the thermal SiO_2 layer was etched in a buffered hydrofluoric acid solution (BHF), resulting in n^+ Si active region with

[§]L.P.B. Lima, M.V.P. dos Santos, M.A. Keiler, H.F.W. Dekkers, S. De Gendt, J.A. Diniz, ECS Trans., 66, 61 (2015).

thickness of 80 nm (Figure 15-II). The nMOS JL devices were fabricated by two different fabrication processes:

i) Using optical lithography, reactive ion etching (RIE) and Ga^+ FIB milling – this sample was labeled JLRFIB;

ii) Using only the Ga^+ FIB milling only – this sample was labeled JLFIB.

For JLRFIB devices a 50 nm thick aluminum layer was deposited to avoid damage on silicon layer. Optical lithography and RIE plasma (Figure 15-III) were taken to define the MESA structure (width of 25μm). Al wet etching (by H_3PO_4 solution) was used to remove the Al layer after the MESA structure definition. Then, the silicon nanowire (SiNW) was defined by Si milling using Ga^+ FIB to shrink the MESA structure from width of 25 μm to 80 nm, resulting in SiNW with width, length and height dimensions of 80 nm, 4 μm and 80 nm, respectively (Figure 15-VI). Moreover, for JLFIB devices the samples were entirely processed by Ga^+ FIB (for SiNW definition) with the same width, length and height dimensions as for JLRFIB devices.

Gas Injection System (GIS) (Figure 15-VII) is an available feature with the Ga^+ FIB system that allows the deposition of metallic and insulator materials, such as Pt and SiO_2, respectively, using ion or electron beams. The precursor gases introduced on the sample by the GIS are adsorbed on the substrate surface and the molecules are activated by the ion or electron beam scanning over the defined area [93]. Thus, volatile components of the process leave the surface and are pumped away by the vacuum system. The precursors for SiO_2 and Pt are, respectively, the Tetraethyl Orthosilicate (TEOS, $Si(OC_2H_5)_4$) and a platinum-based organometallic compound ($(CH_3)_3PtCpCH_3$) [93]. On Si NW, 10 nm thick SiO_2 was deposited by Ga^+ FIB to be used as gate dielectric and 50 nm thick Pt was deposited by Ga^+ FIB to be used as gate, source and drain electrodes (Figure 15-IV and Figure 15-V). Finally 150 nm-thick Pt layer was deposited by Ga^+

FIB for pad contacts. Figure 16 present the scanning electron microscopy (SEM) top views of JLFIB and JLRFIB devices, respectively, after the Pt pad deposition. Then these devices were annealed in a conventional furnace in forming gas (8% H_2 and 92%N_2) at 450ºC. Drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) measurements were carried out for both devices.

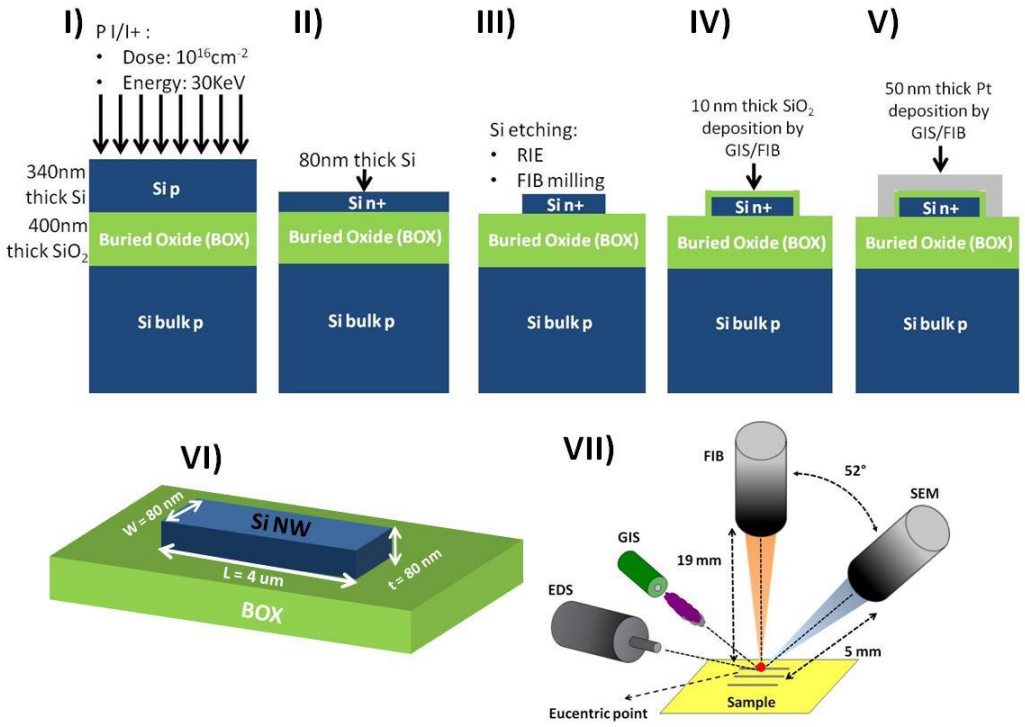


Figure 15 – Schematic of JL fabrication steps (lateral view): i) phosphorus ion implantation; ii) Si layer shrink by oxidation; iii) MESA structure definition; iv) SiO_2 deposition by FIB; v) Pt deposition by FIB; vi) JL dimensions (3-dimensional view); vii) schematic of FIB system.[§]

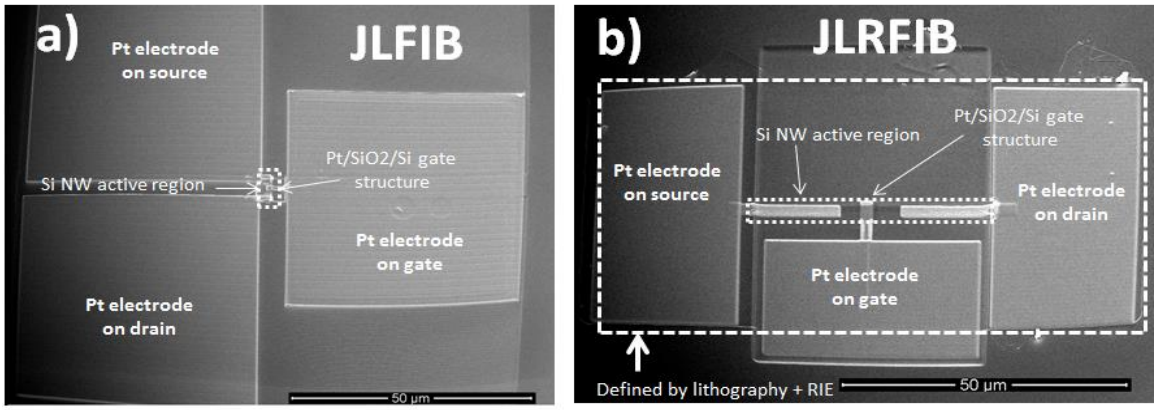


Figure 16 – SEM images of final device (top view): a) JLFIB; b) JLRFIB. [§]

3.2.4 nMOS FinFET devices fabrication**

Figure 17 shows the process fabrication for nMOS FinFET devices. These transistors were fabricated on a SOI (*Silicon On Insulator*) wafer with a Si (340 nm) and SiO_2 (400 nm). The sample was cleaned with a standard cleaning (see Table 5). Then, 10-nm-thick Al layer was deposited by *ULVAC ICOT900 DC Magnetron sputtering* on the Si substrate. After, lithography was performed to achieve MESA structures patterning (see parameters on Table 7).

Table 7 – Lithography parameters for lift-off, The MESA structure was defined using this lift-off process.

Lithography step	Temperature and Time	Tool
AZ5214 resist application	**spin 40 seconds @ 4000 RPM**	**Conventional Spinner**
Bake	**4 minutes @ 90ºC**	**Conventional Hot plate**
Exposure	**Exposure with mask for 6 seconds**	**Karl Suss MJB3**
Post-bake	**1 minute and 45 seconds @ 110ºC**	**Conventional Hot plate**
Flood	**Exposure without mask for 40 seconds**	**Karl Suss MJB3**
Development	**Reveal for 15 seconds using MIF300**	**Wet bench**
Hard-bake	**30 minutes @ 110ºC**	**Conventional Hot plate**

A reactive ion etching (RIE) system was used to etch the Si (Figure 17); and the process parameters were: power of 900 W, process pressure of 50 mTorr, Ar flow of 35 sccm and SF_6 flow of 125 sccm. After Si MESA definition, SiNW structures with width between 100 and 200 nm were defined using a Ga^+ FIB as shown in Figure 17. The Al layer was removed by wet etching (H_3PO_4 and HNO_3 solution) and 10 nm of SiO_2 was grown by dry oxidation in a conventional furnace at 1000ºC.

**[93]L.P.B. Lima, J.A. Diniz, C. Radtke, M.V.P. dos Santos, I. Doi, J. Godoy Fo, J. Vac. Sci. Technol. B, 31, 5 (2013).

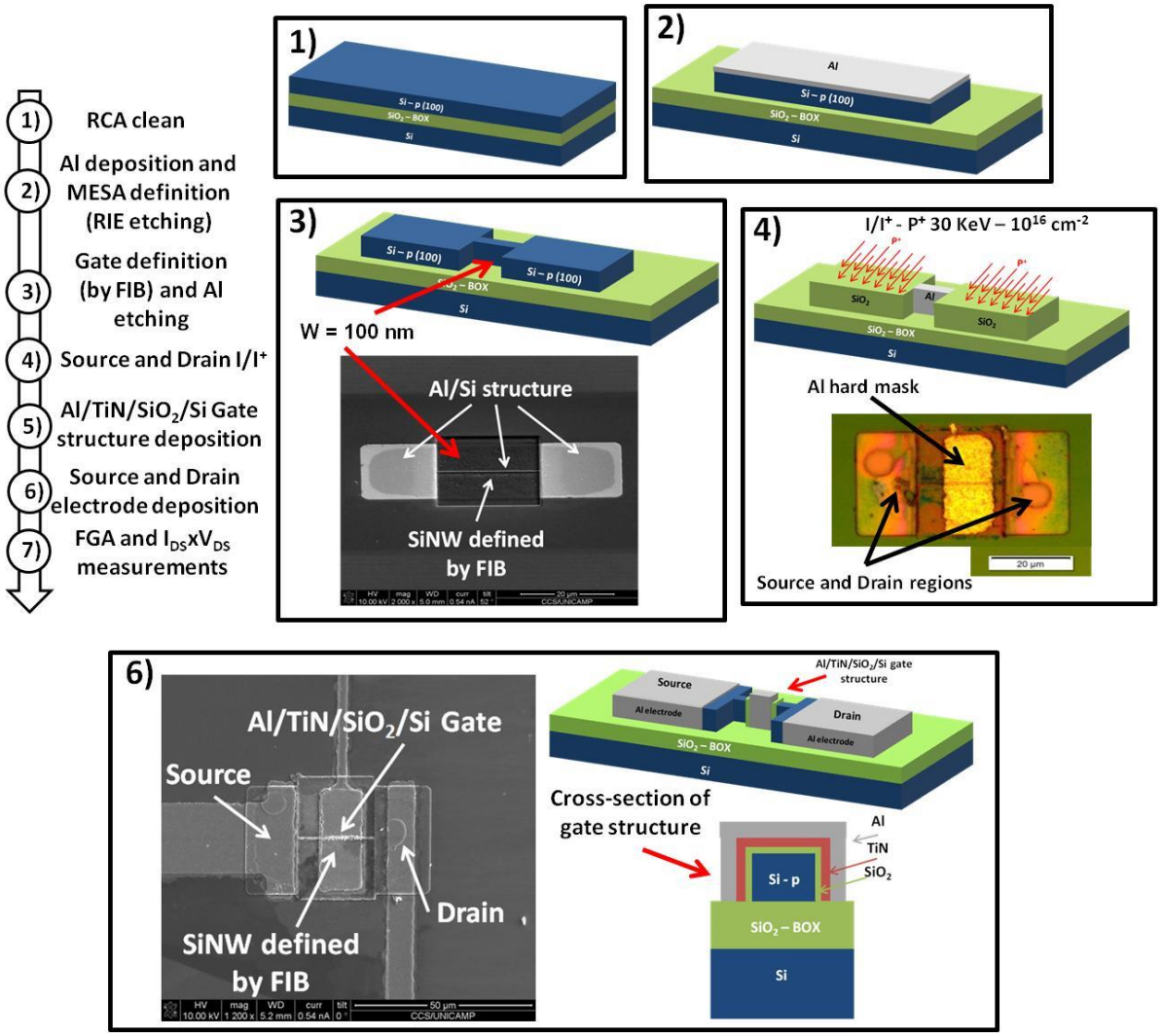


Figure 17 – Schematic of fabrication steps for FinFET device. 1) Standard RCA cleaning of SOI substrate; 2) Al deposition (by sputtering) and MESA structure definition (by RIE etching); 3) Gate definition (using FIB for Si milling) and Al layer wet etching; 4) Ion implantation for source/drain formation; 5) Al/TiN/SiO₂/Si gate structure formation; 6) SEM image of fabricated FinFET device and cross-section of gate structure.[93]

A 300-nm-thick Al layer was deposited by *DC magnetron sputtering* and used as a hard mask, followed by lithography to achieve gate step definition (Figure 17). Phosphorus ion implantation, with energy of 30 keV and dose 10^{16} cm^{-3}, was conducted for drain and source well formation. After this, the Al was etched using wet etch (H_3PO_4 and HNO_3 solution), followed by a rapid thermal annealing (RTA) at 1000ºC for 60 seconds in a pure N_2 ambient. SiO_2 was removed by

HF etching and the samples were inserted on a conventional furnace for dry oxidation to obtain the 10 nm SiO_2 gate dielectric. Gate lithography was done for "lift-off" and TiN/Al layers to obtain the gate structure (Table 8).

Table 8 – Lithography and TiN/Al deposition parameters for gate structure.

Lithography parameters for gate definition		
AZ5214 resist application	**spin 40 seconds @ 4000 RPM**	**Conventional Spinner**
Bake	**4 minutes @ 90ºC**	**Conventional Hot plate**
Exposure	**Exposure with mask for 16 second**	**Karl Suss MJB3**
Post-bake	**1 minute and 45 seconds @ 110ºC**	**Conventional Hot plate**
Flood	**Exposure without mask for 40 second**	**Karl Suss MJB3**
Development	**Reveal for 30 seconds using MIF300**	**Wet bench**
Hard-bake	**30 minutes @ 110ºC**	**Conventional Hot plate**
TiN/Al *in situ* deposition for metal gate electrode		
TiN/Al *in situ* deposition	**N2: 10 sccm Ar: 80 sccm 1000 W @ RT**	**DC reactive magnetron Sputtering**
	Ar: 60 sccm 1000 W @ RT	

20-nm-thick TiN and 200-nm-thick Al films were used as metal gate electrode. These films were deposited *in situ* by *DC reactive sputtering* depositions and are the same as used on MOS capacitors and Schottky diodes presented in section 3.3.2.2. Finally, lithography was performed for "lift-off" of drain and source contacts. For source and drain contacts, a 200-nm-thick Al layers were deposited by *DC reactive Magnetron sputtering* process. The characterization of these devices can be found in chapter 4.

3.3 TiN Films Obtained by Sputtering (PVD)[§§]

3.3.1 TiN/Si samples for structural characterization

In order to study the PVD TiN film composition and structure, X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy measurements were done. Additionally, TiN electrical resistivity was extracted by four probe measurements.

The PVD TiN depositions were performed by *ULVAC ICOT900 DC magnetron reactive sputtering* system using a Titanium target (99.95% purity). The depositions were done with Ar/N_2 about 6:1 (Ar flow: 60 sccm and N_2 flow: 10 sccm), DC power of 1000 W and process pressure fixed at 10^{-6} Pa. These deposition parameters were based on previous published work [13,14]. Test samples were fabricated following the procedure presented in Figure 18. The films were deposited on p-type Si (100) wafers with electrical resistivity between 1 and 10 Ω.cm. The substrates were cleaned with a standard cleaning as described in Table 5. TiN surface composition was extracted by XPS measurements, while the crystalline structure was studied using Raman spectroscopy. The films thicknesses were obtained by a scan profiler. The electrical resistivity of TiN film was extracted by four probe technique.

[§§]L.P.B. Lima, J.A. Diniz, C. Radtke, M.V.P. dos Santos, I. Doi, J. Godoy Fo, J. Vac. Sci. Technol. B, 31, 5 (2013).
L.P.B. Lima, M.A. Moreira, J.A. Diniz, I. Doi, Phys. Status Solidi, 9, p. 1427 (2012).

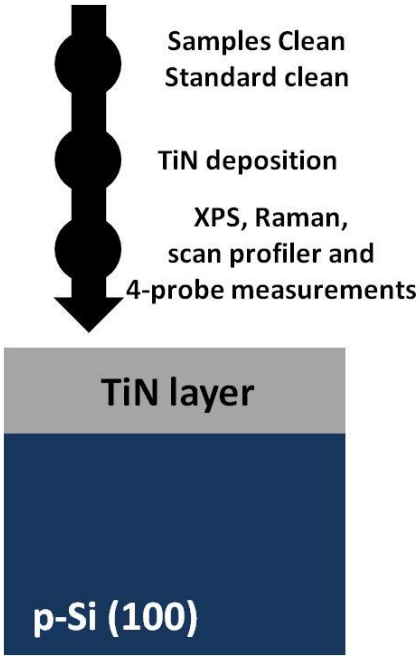


Figure 18 – Schematic of TiN/Si structure sample for structural characterization.

3.3.2 MOS capacitors and Schottky diodes fabrication

3.3.2.1 TiN/SiO_xN_y/Si MOS capacitors

Figure 19a show the fabrication steps for MOS capacitors fabrication with SiO_xN_y as a dielectric. For those devices, p-type Si (100) wafers with electrical resistivity between 1-10Ω.cm were used. These substrates were cleaned with a standard cleaning (as described in Table 5). Electron Cyclotron Resonance (ECR) plasma oxynitridation process was used to obtain a 8-nm-thick SiN_xO_y film, which was carried out at room temperature, with process pressure at 5mTorr, 2.45 GHz ECR power fixed at 750W and O_2:N_2:Ar flow ratio of 3:10:20 sccm. Then, lithography for lift-off process was carried out (described in Table 7), using a mask composed of an array of 200-µm-diameter dots. A 300-nm-thick TiN layer deposited by *ULVAC ICOT900 DC reactive magnetron sputtering* system using a Ti (99,95% purity) target, an N_2/Ar ambient (with flow ratio of 10/60 sccm, respectively) and DC power of 1000 W, was used as electrode in the MOS

capacitors fabricated. The backside substrate electrode was made by 300-nm-thick Al layer deposited by *DC magnetron sputtering* using Al target (99.95% putity), power of 1000 W in pure argon ambient (argon flow of 60 sccm). The devices were annealed by conventional furnace in forming gas (8% H_2 and 92%N_2) at 450ºC during 10, 20 and 30 minutes. These MOS capacitors were used to obtain 1MHz capacitance-voltage (C-V) measurements to extract MOS charge density, flat-band voltage and TiN work function.

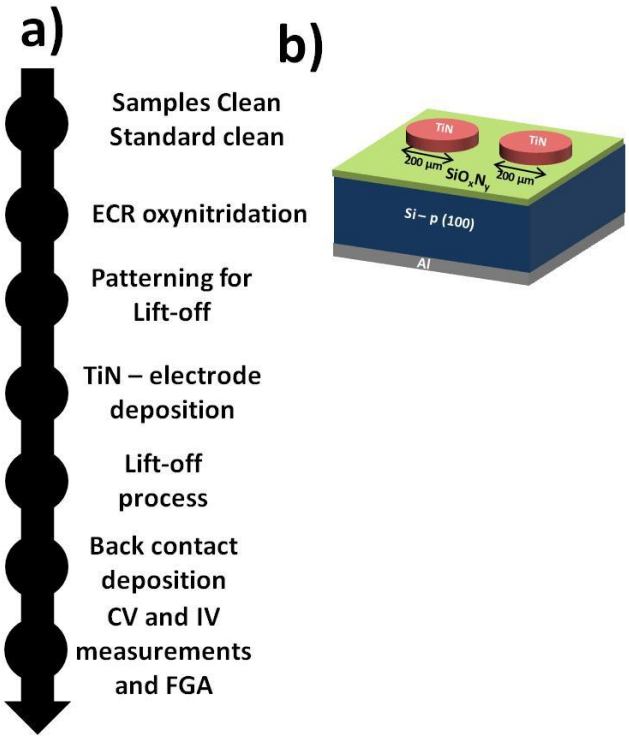


Figure 19 – Fabrication steps for TiN/SiO_xN_y/Si devices.

3.3.2.2 MOS capacitors and Schottky diodes on the same wafer

Figure 20a shows the process fabrication for MOS capacitors and Schottky diodes on the same wafer. These devices were fabricated on n-epi-layer (4 µm)/n+-type Si (100) wafers with electrical resistivity values of 0.008 and 0.020 Ω.cm/1.1 Ω.cm, respectively. The substrates were cleaned with a standard cleaning (as shown in Table 5). Using dry thermal oxidation at 1000ºC for 2

minutes, an 8-nm-thick SiO_2 was obtained to be used as dielectric on MOS capacitor. Sub sequentially, lithography and SiO_2 etching (using HF buffered solution) were done to define the MOS capacitor and Schottky diode areas. Then, lithography for lift-off process was carried out (as presented in Table 7), using a mask composed of an array of 200-µm-diameter dots. TiN films were used as electrode on MOS capacitor and Schottky diode and were deposited by *ULVAC ICOT900 DC reactive magnetron sputtering* system using a Ti (99,95% purity) target, an N_2/Ar ambient (with flow ratio of 10/60 sccm, respectively), a DC power of 1000 W. To get Al/TiN/SiO_2/Si and Al/TiN/Si structures presented on Figure 20c, 200-nm aluminum (Al) layer was deposited *in*-situ on the top of TiN layers by *DC magnetron sputtering* using an Al target (99.95% putity), power of 1000 W in pure argon ambient (argon flow of 60 sccm). For backside contact electrode, 300-nm-thick Al layer was used and the film was obtained by *DC magnetron sputtering* with the same DC power and Ar flow previously mentioned.

Figure 20b presents a schematic of the MOS capacitor with TiN/SiO_2/Si and Schottky diodes with TiN/Si, while Figure 20c shows the devices with Al/TiN/SiO_2/Si and Al/TiN/Si structures. Then, the devices with structures composed of Al/TiN/SiO_2/Si (devices named MOS capacitors with Al), TiN/SiO_2/Si (devices named MOS capacitors without Al), Al/TiN/Si (devices named Schottky with Al), and TiN/Si (devices named Schottky without Al) were sintered in a conventional furnace in forming gas (8% H_2 and 92%N_2) at 450°C for different times, between 0 and 30 minutes.

Capacitance-voltage (C-V) measurements were done on MOS capacitors in order to extract TiN work function, effective charge density and flat-band voltage. Current-voltage (I-V) measurements were carried out on Schottky diodes for ideality factor and TiN work function

extraction [12,13]. These parameters were related to the oxygen incorporation on the TiN surface, the dipole variation at the TiN/SiO_2 interface and Ti and N vacancies in the TiN films.

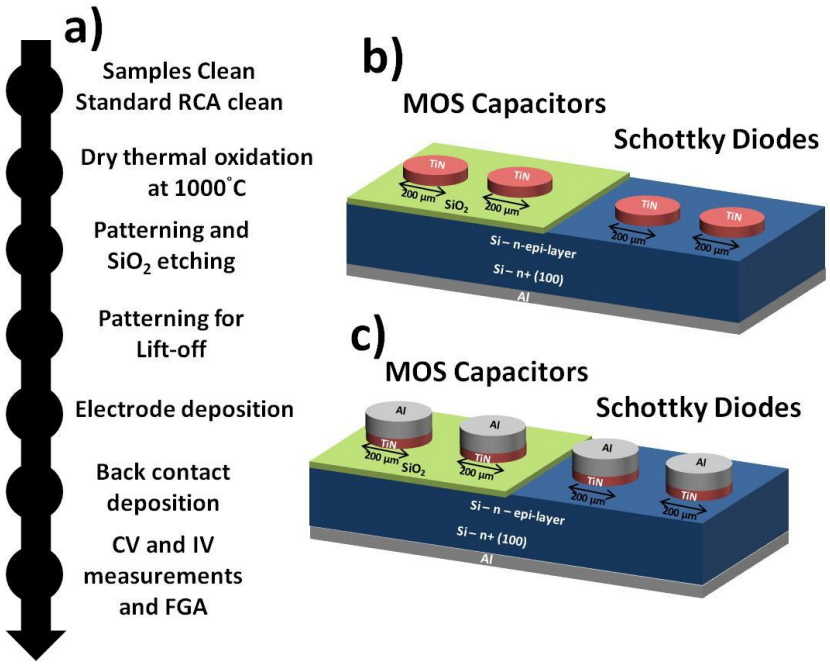


Figure 20 - Schematic view of MOS capacitor and Schottky diode fabricated on the same Si substrate.

3.4 TiN Films Obtaines by Atomic Layer Deposition (ALD)‡‡

3.4.1 TiN/Si samples for structural characterization

Atomic layer deposition (ALD) was used to obtain *in situ* layers of HfO_2, AlN and TiN on Si (100) p-type substrate. The samples were cleaned using Stantard IMEC clean as described in Table 9 [87]. The final step is the Marangoni drying method, which dries a hydrophobic-hydrophilic surface without 'watermarks' [87,88]. This can be achieved with IPA vapour and spin/rinse dry process [87,88].

‡‡ L.P.B. Lima, H.F.W. Dekkers, J.G. Lisoni, J.A. Diniz, S. Van Elshocht, S. De Gendt, J. App. Phys., 115, p.074504 (2014).

Table 9 – IMEC Clean step procedures[84]

Cleaning solution	Temperature and Time	Purpose
H_2SO_4/O_3	@ 90ºC for 5 minutes	Organic compounds removal
H_2O/O_3 rinse	@ 60ºC and 20ºC for 8 minutes	Residual solution removal
HF (0.5%) / HCl (0.5M)	@ RT* for 2 minutes	Chemical SiO_2, particle and metal contamination removal
H_2O rinse	@ RT* for 10 minutes	Residual solution removal
Marangoni drying	@ RT* for 8 minutes	Residual solution removal

To avoid and minimize the oxygen contamination by air exposure, the HfO_2, AlN and TiN layers were deposited sequentially without leavin the ALD process chamber. As shown in Figure 21, the ALD AlN films were obtained using separate pulses of trimethyl aluminum (TMA) and NH_3 precursors at 400ºC. TiN ALD films were done using $TiCl_4$ and NH_3 gas pulses at 400ºC. The TMA and NH_3 flows were 60 sccm and 40 sccm, respectively, for all the AlN depositions. For TiN depositions, the $TiCl_4$ and NH_3 flows were 50 sccm and 40 sccm, respectively. The gas precursor pulse and purge times are presented in Table 10.

Table 10 – Gas precursor pulse and purge time for ALD depositions.

Deposition step	Time (ms)
AlN depositions	
TMA pulse / N_2 purge	500 / 3000
NH_3 pulse / N_2 purge	4000 / 3000
TiN depositions	
$TiCl_4$ pulse / N_2 purge	2000 / 3000
NH_3 pulse / N_2 purge	4000 / 3000

Also, AlN/TiN (first layer is AlN then TiN film) and TiN/AlN (first layer is TiN then AlN film) laminate samples were obtained by switching the gas precursors (TMA and $TiCl_4$) on ALD chamber for several loops, as shown in Figure 21.

X-ray reflection (XRR) measurements were performed on samples with AlN layers deposited directly on the top of HfO_2 and TiN films to examine the impact of growth inhibition on AlN. In addition, XRR were done on samples with TiN on the top of AlN films to study the titanium nitride metal layer growth. To investigate the Al incorporation in the TiN layer and film chemical composition, secondary ion mass spectroscopy (SIMS) and XPS measurements were carried out.

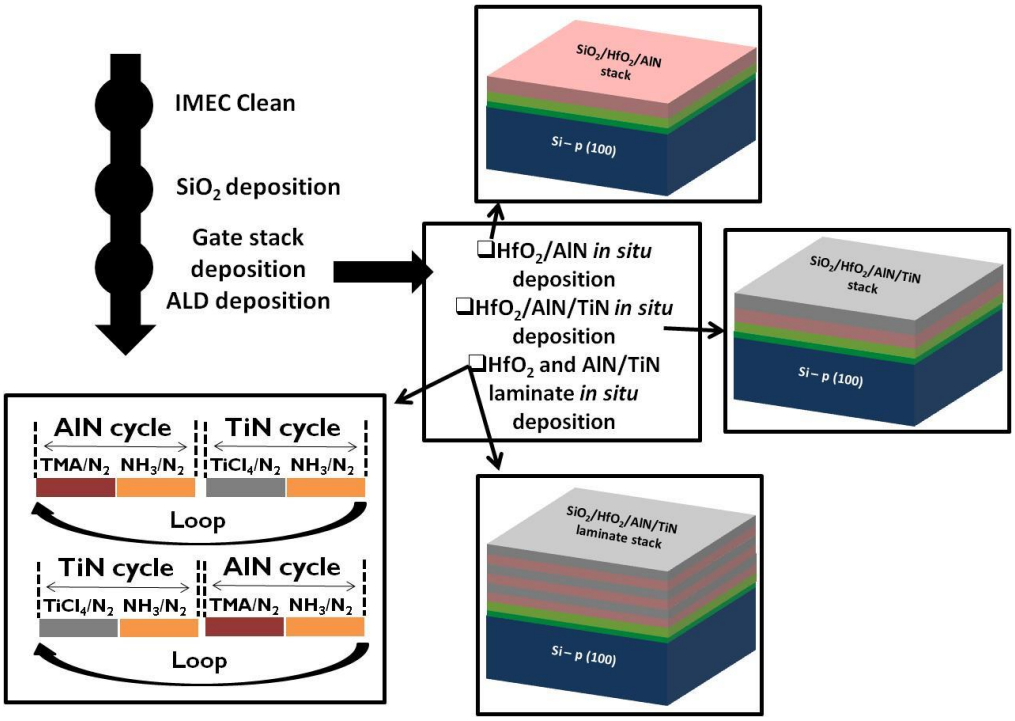


Figure 21 - The fabrication steps for HfO_2/AlN, HfO_2/AlN/TiN (with and without laminate) structures.[‡‡]

3.4.2 MOS capacitors for electrical characterization

For electrical characterization and TiN effective work function value extraction, metal-oxide-semiconductor (MOS) capacitors were fabricated on p-type Si (100) with SiO_2 and a 2-nm-thick HfO_2 as an interfacial layer and dielectric, respectively. Various SiO_2 thicknesses, between 1.4 and 5.7 nm, were achieved using the slant etch procedure [49]. MOS capacitors fabrication steps are

shown in Figure 22. The AlN and TiN films were obtained using ALD deposition as described in the previous section.

C-V measurements were performed on those devices for metal effective work function extraction. Capacitors with Pt/HfO_2/SiO_2/Si structure capacitors (with Pt electrodes obtained by sputtering deposition) were used as a reference for calibration of C-V and EWF extraction. To study the influence of Al incorporation on TiN layer capacitors with different metal electrode structures were fabricated, as presented in Table 11. For Al diffusion reference sample (see Table 11), 10 nm of TiN and 2 nm of TaN were deposited in situ by ALD. The Al layer was deposited on the top of TaN film, followed by a FGA (8% H_2 and 92%N_2) step at 420ºC for 20 minutes (which corresponds to the standard annealing time for CMOS devices in back end of line (BEOL) process) for Al diffusion into TiN film. The TaN layer was used as a diffusion barrier to control the amount of Al into TiN layer and also to prevent excessive gate leakage (due to high Al concentration at the interface between TiN and HfO_2). After Al layer etching, 70nm of Pt layer was deposited on top of TaN. For devices with TiN/TiAl/TiN/HfO_2 stack, the TiN and TiAl were deposited by ALD and PVD respectively. Forming gas anneal was performed after the deposition of this stack. Then, 70nm of Pt layer was deposited by PVD on top of TiN.

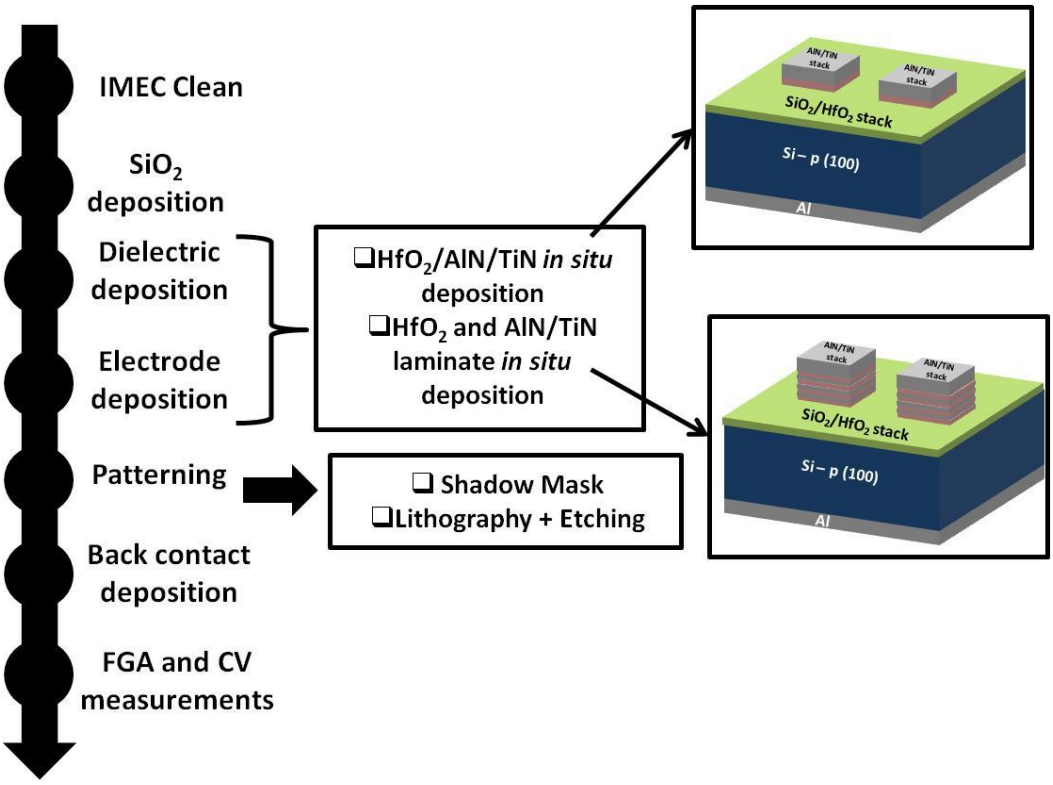


Figure 22 – The fabrication steps for MOS devices.[‡‡]

Table 11 – Sample name, structure, sample purpose and gate stack deposition.

Sample name	Structure	Purpose	Gate Stack Deposition
Pt ref	Pt/HfO_2/SiO_2/Si	Reference sample for EWF extraction	HfO_2 deposition
TiN ref	Pt/TiN/HfO_2/SiO_2/Si	TiN EWF for reference	HfO_2/TiN deposition
Al dif.	Pt/TaN/TiN/HfO_2/SiO_2/Si	TiN EWF with Al diffusion	HfO_2/TiN/TaN deposition
TiN/TiAl	Pt/TiN/TiAl/TiN/HfO_2/SiO_2/Si	TiN EWF using TiAl as a Al diffusion source	HfO_2/TiN/TiAl/TiN deposition
TiN/AlN	TiN/AlN/HfO_2/SiO_2/Si	TiN EWF using AlN as a Al diffusion source	HfO_2/AlN/TiN deposition
Laminate	TiN/AlN/HfO_2/SiO_2/Si - laminate	TiN EWF using AlN laminate as a Al diffusion source	HfO_2/AlN/TiN laminate deposition

To obtain Al diffusion from a dual TiN/AlN layer or TiN/AlN laminate capacitor devices (see Table 11), AlN and TiN depositions were done in situ with the HfO_2 deposition, to minimize the oxygen contamination, as previously discussed. In order to increase the TiN thickness for C-V

measurements, 10 nm TiN was deposited on the top of ALD TiN using physical vapor deposition. After that, a thermal annealing step was performed using forming gas at 420ºC for 20 minutes. Separate capacitors, with sizes of 2500 μm^2, 10000 μm^2 and 78400 μm^2, were obtained by etching the TiN and AlN after lithographic patterning. Finally, following the SiO_2 removal from the backside of the silicon wafer, 500 nm Al was deposited by PVD on the backside of the silicon wafer. TiN effective work function (EWF) was extracted using C-V measurements performed on MOS capacitors. C-V measurements were taken from TiN/AlN devices, with and without the laminate deposition, at a frequency of 100 kHz using a Keithley analyzer 4200 SCS model. TiN work function was determined using Hauser's CVC program [67].

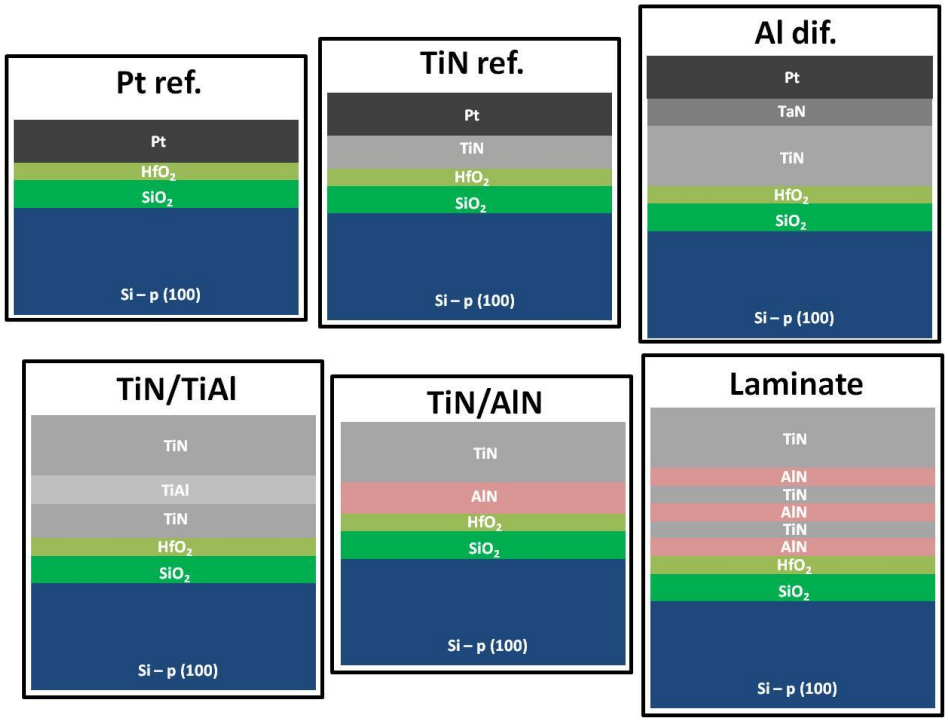


Figure 23 – Schematic cross-section view of devices presented in Table 11. The thickness of TiN, Pt, AlN, TiAl, TaN, HfO_2, SiO_2 and Si layers are not in scale.

CHAPTER 4

TiN FILM CHARACTERIZATION AND DISCUSSIONS

4.1 Introduction

This chapter presents the electrical characterization of Junctionless devices, to study the SiNW properties. Moreover, the electrical characterization of nMOS FinFET with Al/TiN as metal gate electrode is also presented in this chapter (section 4.2). In addition, the characterization of TiN films obtained by *DC reactive magnetron sputtering* is also described in this chapter (section 4.3). Samples for physical and electrical characterization were prepared as described in chapter 3. Scan profiler, four-probe technique, Raman spectroscopy and X-ray photoelectron spectroscopy (XPS) were used to study the physical properties from PVD TiN layer. Electrical characterization of PVD TiN was done by capacitance-voltage (C-V) and current-voltage (I-V) measurements from MOS capacitors and Schottky diodes. The metal layer surface oxidation effect was evaluated from electrical characterization on fabricated devices. Additionally, dipole variation (at the TiN/dielectric interface) contributions on PVD TiN EWF value was estimated using both C-V and I-V measurements. Furthermore, this chapter presents the study of AlN and TiN layers deposited *in situ* by an ALD system (section 4.4) in order to understand the influence of Al diffusion at the

interface between high-k dielectric (in this case, HfO_2 also deposited *in situ* with AlN and TiN layers) and TiN to lower the metal gate EWF (see chapter 3). The advantages of using ALD system for obtaining HfO_2/AlN/TiN stack are layer conformality and the thermal stability control of Al diffusion into TiN. In contrast, TiAl is today only reported to be deposited using PVD, which lacks conformal deposition in trenches and fin structures. Therefore, the usage of AlN/TiN stack is more suitable for 3D technology, such as FinFET's.

4.2 3D devices characterization

4.2.1 pMOS Junctionless devices[§§]

As mentioned in section 3.2.1, junctionless (JL) transistors were fabricated to study the SiNW properties. Focused ion beam (FIB) system was used for those devices fabrication. The gate dielectric (SiO_2) and gate, drain and source metal electrodes (Pt) were deposited *in situ* using the GIS-FIB system. The chemical composition of SiNW and deposited materials were evaluated using energy dispersive X-ray spectroscopy (EDS) measurements. The electrical properties were investigated using drain-source current (I_{ds}) *versus* drain-source voltage (V_{ds}) and drain-source current (I_{ds}) *versus* gate-source voltage (V_{gs}) measurements.

The Al diffusion into Si substrate was confirmed by EDS measurements. Figure 24 shows the obtained EDS spectra of samples 1, 2, 3 and 4 (fabrication procedure described on section 3.2.2). The presence of Al peak, related to K_α emissions, evidences this element diffusion into Si substrate [97]. In addition, the EDS tool is sensitive to elements with atom concentration higher than 10^{16} cm^{-2}. So, sample 1 presents the highest Al concentration into Si layer and this sample was used for JL device fabrication.

[§§103]L.P.B. Lima, M.V.P. dos Santos, F.H. Cioldin, J.A. Diniz, I. Doi, J. Godoy Fo, ECS Trans., 49, p. 367 (2012).

Cross-section schematic view of the JL device is shown in Figure 25a. The JL fabrication steps, using FIB system, are shown in Figure 25b, 25c, and 25d. First of all, to obtain the Si nanowire (shown in Figure 25b), a Ga^+ ion beam with energy of 30 keV and ion current of 7 nA was used. Width, length and height dimensions of Si nanowire were about 100~300 nm, 4 µm and 200 nm, respectively. Figure 25c shows the deposition of 10 nm SiO_2 layer as gate dielectric on Si nanowire, using Ga^+ ion beam with energy of 30 keV and ion current of 10 pA. Figure 25d shows top view schematic of JL device after the Pt definition contacts of Gate, Drain and Source electrodes, where 100 nm Pt layer was deposited using Ga^+ ion beam with energy of 30 keV and ion current of 10 pA on SiO_2 and Si nanowire, respectively.

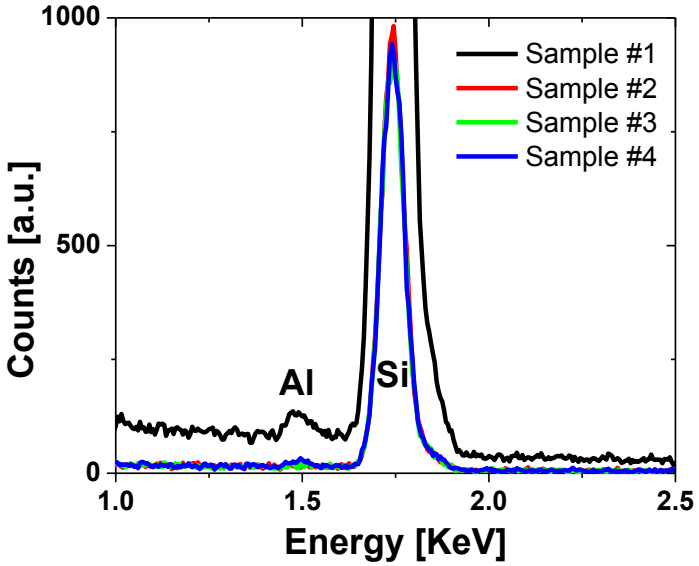


Figure 24 – EDS spectra after the Al diffusion of samples (diffusion steps): #1; #2; #3 and # 4.[103]

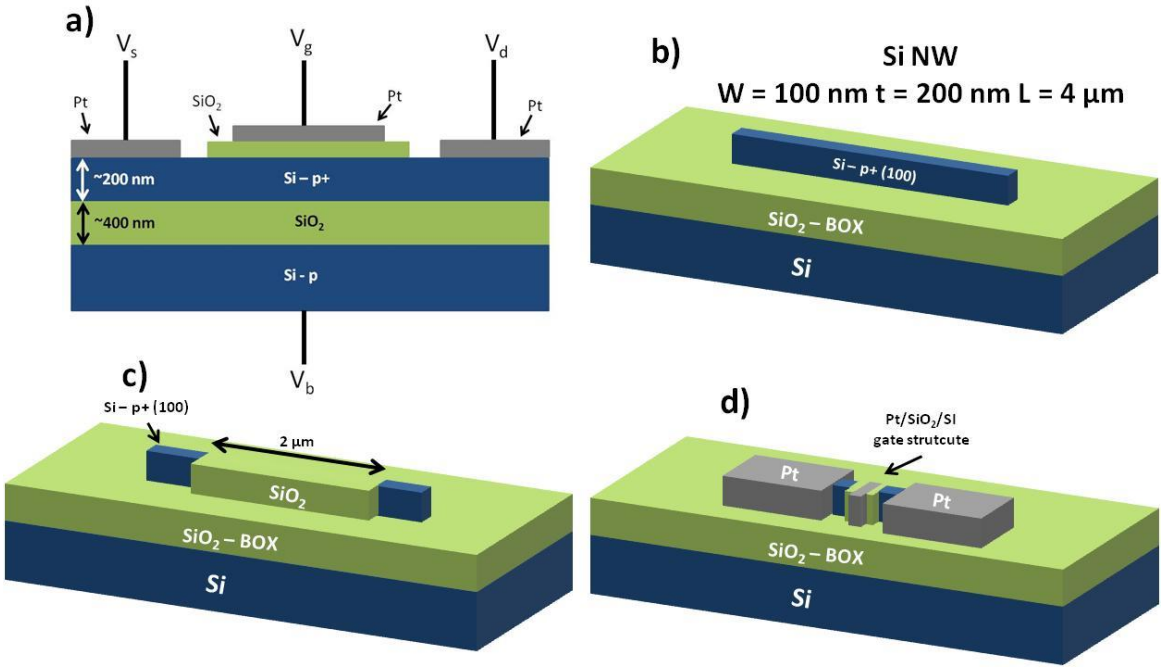


Figure 25 – Schematics of: a) cross-section of JL device on SOI substrate; b) Si p+ nanowire after Al diffusion and FIB milling on SOI substrate; c) gate SiO_2 deposited by FIB on Si p+ nanowire; d) Pt gate, source and drain electrodes deposited by FIB.[103]

SEM and EDS measurements (Figure 26) were carried out in all samples after the Si nanowire definition and SiO_2 deposition (using Ga^+ FIB). The oxygen presence in EDS spectra is from SiO_2 on SOI structure (Buried Oxide of SOI wafer) or SiO_2 deposited by FIB. The gallium and aluminum presences are from Ga^+ ion beam and Al diffusion into Si nanowire. Furthermore, from Figure 26a, 26b and 26c, it is possible to conclude that Al and O peaks correspond to K_α emissions, while Si, Ga and Pt peaks correspond to $K_{\alpha 1}$, L_α, $M_{\alpha 1}$ emissions, respectively [97]. Figure 27a shows a JL device top view by SEM analysis. Figure 27b presents EDS measurements on Pt pads of JL device. Pt peak presence in the EDS spectrum confirms the formation of pads.

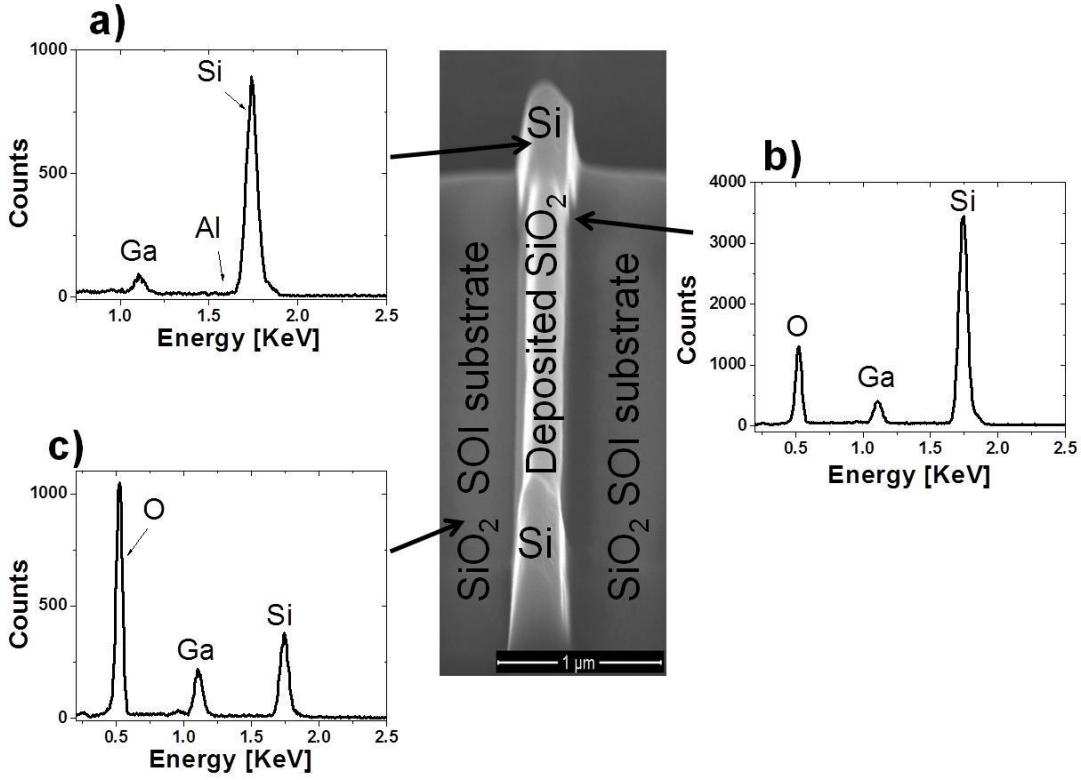


Figure 26 – SEM image (in the center) of Si nanowire with SiO_2 deposited on the gate region (step 3 – c). EDS measurements of a) Si nanowire region; b) SiO_2 of SOI substrate and c) SiO_2 deposited by FIB system.[103]

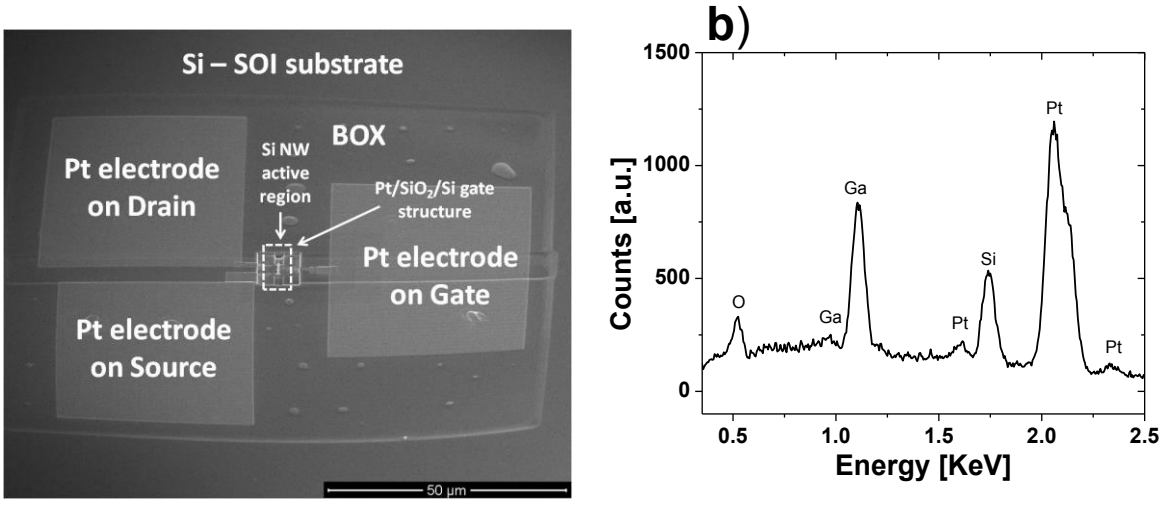


Figure 27 – a) Final JL device (step 4 – d); b) EDS measurements of Pt pad deposited by FIB system.[103]

I_{ds} x V_{ds} measurements were carried out in order to study the characteristics of JL device, which was fabricated on SOI substrate of the sample 1. This sample presented the highest Al concentration into Si nanowire (see EDS measurement in Figure 24a). These I_{ds} x V_{ds} measurements were obtained using Keithley model 4200 SCS analyzers. Pt contacts were sintered in conventional furnace in forming gas at 450ºC for 10 minutes. The applied gate voltages (V_{gs}) were between 0 and -2V, with step of -0.5 V. Figure 28a and Figure 28b show the I_{ds} x V_{ds} and log(I_{ds}) x V_{gs} measurements, respectively. From I_{ds} x V_{ds} curves, high values of contact resistances of about 300 kΩ between Pt and Si p+ were extracted, which result in distortions, such as:

i) the presence of a non-ohmic contact region with V_{ds} values between 0 and -3.0 V;

ii) the slope of curves, because all curves would be in parallel with V_{ds}-axis in the ideal case.

These distortions can be avoided with Si nanowire height and width of JL devices lower than 50 nm, instead of 200 nm used in our devices (Figure 25a), which can give better control of bulk current in Si nanowire, and sintering process of the contacts with longer times (between 15 and 30 minutes) to reduce the contact resistance values of up to 100 Ω [78,79]. Otherwise, from I_{ds} x V_{ds} curves (Figure 28a), it can be observed that the device is working, with gate voltage (V_g) control the I_d current conduction like a gated resistor or JL transistor [78,79]. Furthermore, for the same JL transistor, log(I_{ds}) x V_{gs} curve (Figure 28b) for V_{gs} =V_{ds} and V_{bs} =0V (voltage between bulk (V_b) and source (V_s)) was extracted, resulting in off current I_{off} = 12 nA (for V_{gs} = 0V), leak current I_{leak} = 178 nA (for V_{gs} = =5V), and slope = 236 mV/decade. The off and leak currents are high and in agreement with extracted slope value, which is high when it compared with results present in references 79 and 104, and also confirms the results extracted from I_{ds} x V_{ds} curves (Figure 28a).

These results indicate that our method the fabrication of JL device, using FIB process steps and Al diffusion, can be used to get prototypes of devices based on Si nanowire.

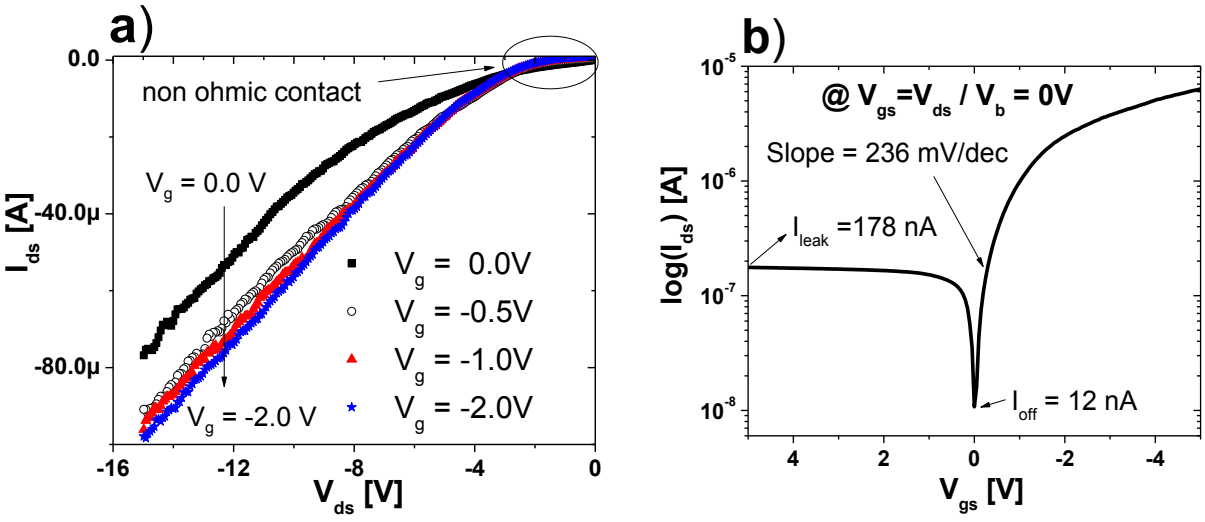


Figure 28 – a) I_{ds} x V_{ds} curves and b) log(I_{ds}) x V_{gs} curves of JL device with 10 minutes of sintering time.[103]

4.2.2 nMOS Junctionless devices***

EDS measurements were carried out in order to study the chemical composition of Si NW after the Si milling and SiO_2 deposition by Ga^+ FIB. Figure 29 presents the EDS measurements on Si NW. Figure 29a present a SEM image from Si NW after the SiO_2 deposition by Ga^+ FIB. EDS spectra at the Si NW (Figure 29b) shows the presence of Si $K\alpha_2$ peak (with energy of 1.73 keV) which indicates that the SiNW composition is essentially Si [97]. However, during the Si NW definition by the Si milling using the Ga^+ FIB, some Ga ions could be incorporated into SiNW surface. The presence of Ga Lα peak (with energy of 1.09 keV) on Si NW EDS spectra confirms the Ga incorporation on Si NW [97]. Furthermore, the Si NW surface could be damaged or even

***L.P.B. Lima, M.V.P. dos Santos, M.A. Keiler, H.F.W. Dekkers, S. De Gendt, J.A. Diniz, ECS Trans., 66, 61 (2015).

amorphized during the Si milling process by the Ga^+ FIB. In this way, the Ga incorporation on SiNW could lead to distortions on electrical measurements of the final JL device. In order to reduce the Ga^+ incorporation on Si NW, the MESA structure (width of 25 μm) definition on JLRFIB devices was obtained by optical lithography and RIE; and the Si milling by Ga^+ FIB was used to shrink the MESA structure from width of 25 μm to 80 nm, resulting in SiNW. With this, the Ga^+ incorporation on Si NW is reduced (exposure to Ga^+ FIB is less than in JLFIB devices).

Figure 29c presents the EDS spectrum after the SiO_2 deposition by the Ga^+ FIB. The presence of O Kα peak (with energy 0.52 keV) and the presence of Si $K\alpha_2$ peak may indicate the SiO_2 formation [97]. However, the presence of Ga Lα peak on that EDS spectrum indicates some Ga incorporation on SiO_2 layer, due to the usage of Ga^+ FIB to assist the SiO_2 deposition. EDS spectrum from buried oxide layer from SOI wafer is shown in Figure 29d and it is possible to notice the presence of Si, Ga and O peaks. The Si and O peaks are related with SiO_2 formation on buried oxide layer and the Ga peak is related with the Ga^+ incorporation during the Si milling process, as previously discussed. Moreover, the EDS spectrum obtained on Pt contact electrode (Figure 29e) presents the Ga Lα (with energy of 1.09 keV) and Pt Mα (with energy of 2.05 keV) peaks, which confirms the Pt deposition by the Ga^+ FIB [97]. Still this spectrum presents the C $K\alpha_1$ peak (energy 277 eV) that indicates some C incorporation into Pt electrodes from organometallic precursor gas (GIS), thus decreasing pure Pt work-function and conductivity [97].

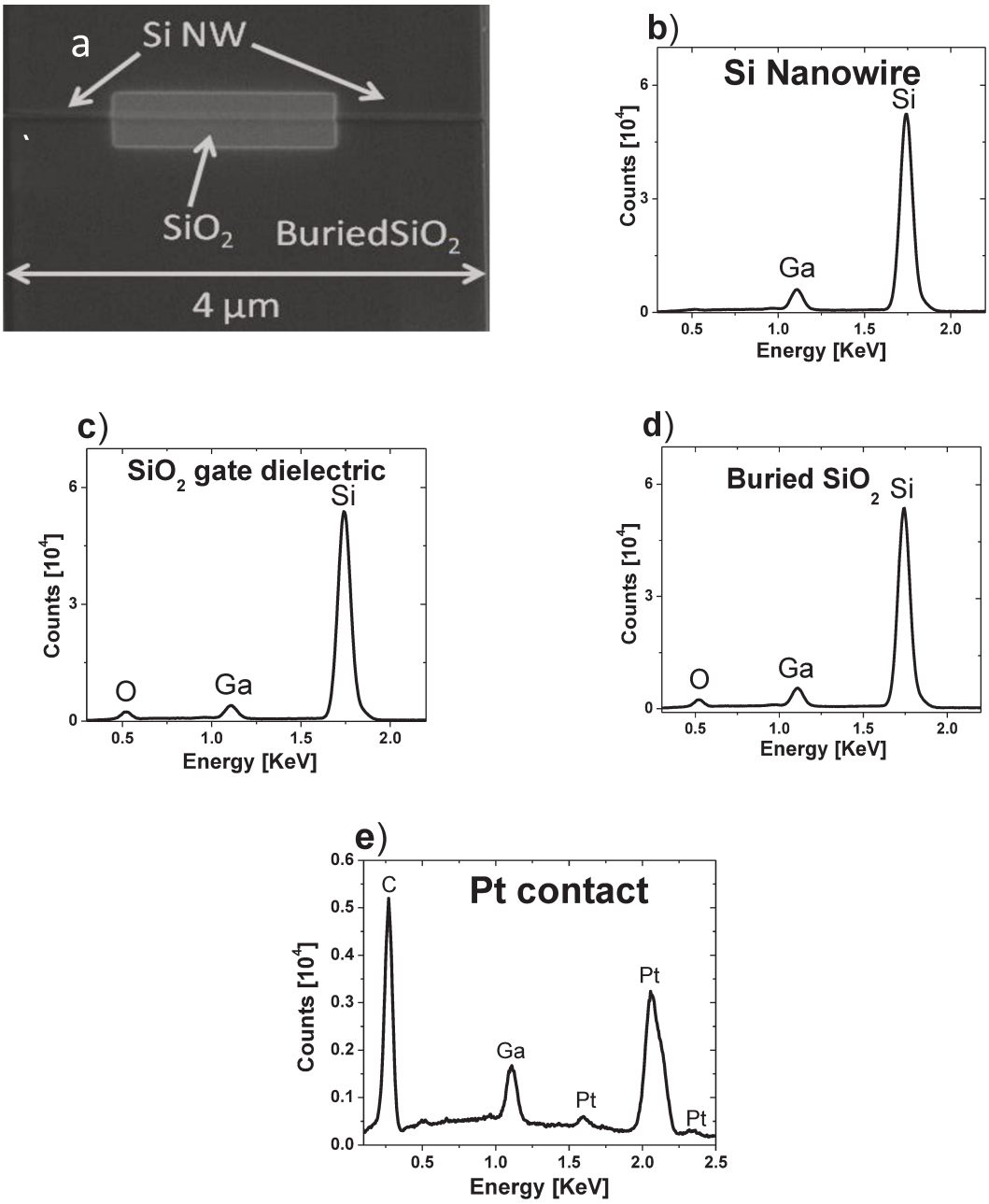


Figure 29 – a) Si nanowire with gate SiO_2 deposited. EDS measurements of b) Si fin (nanowire); c) gate SiO_2 deposited by FIB system; d) buried SiO_2 of SOI wafers; and e) Pt electrode contact.[***]

After the JL device fabrication, the devices were annealed in forming gas ambient at 450ºC for 10 and 20 minutes. Drain-source current (I_{ds}) by drain-source voltage (V_{ds}) measurements were carried out on JLFIB and JLRFIB devices by using Keithley model 4200 SCS analyzers. Figure

30a shows a cross-section of a JL device. The applied gate voltages (V_g) were between -2 V and 2 V, with step of 1 V. It is well know that the current conduction occurs inside the nanowire region of the JL devices, which means that the electron concentration is higher on Si NW bulk substrate [98-101]. So, the current flow can be controlled by V_g. With this, on an n-type JL device negative values of V_g will increase the current flow through Si NW bulk and positive values of V_g will decrease the current flow [98-101]. As shown in Figure 30b and 30c, the JLFIB and JLRFIB devices are working like a gated resistor or JL device, with high Pt source and drain contact resistances (about 300 KΩ between Pt and Si n^+), which leads to distortions on I_{ds} x V_{ds} curves [79]. However, these distortions are mainly related to the contact resistance and bulk current control. The contact resistance can be decreased with longer times of sintering process, and consequently, distortions on I_{ds} x V_{ds} characteristics can be reduced. The gate channel depletion of Si NW can be better controlled with smaller Si NW width and height [78,79,99-101]. So, the control of the channel bulk current is improved for thinner Si NW, due to the better control of channel depletion by applied V_g, and therefore, the distortions on I_{ds} x V_{ds} characteristic can be reduced.

Moreover, the structure of Si NW is important to achieve better control of the bulk current. Thus, damages, defects and impurity incorporation on Si NW could result in poor control of bulk current. As mentioned in the experimental procedure, the JLRFIB devices were fabricated using optical lithography and RIE to define the MESA structure and after, Ga^+ FIB was used to thin down the gate width dimensions, while the JLFIB devices were fabricated entirely using the Ga^+ FIB. In this way, it is expected that JLRFIB would present better bulk current control than JLFIB devices. The reason is that for JLFIB devices the Si milling process is longer than in JLRFIB, so the damage on Si NW surface and Ga^+ ions incorporation could be higher than in JLRFIB devices.

Hence, the distortions on I_{ds} x V_{ds} curves will be higher on JLFIB devices than on JLRFIB devices as shown in Figure 30b and 30c. Figure 30d presents the drain-source current (I_{ds}) by gate-source voltage (V_{gs}) curves for JLRFIB devices. The extracted values for sub threshold slope (SS) are lower than 100 mV/decade and were obtained for different bias from bulk polarization (V_{bulk}). For V_{bulk}=0 V the SS=64 mV/decade was extracted and for V_{bulk}=-1 V and V_{bulk}=1 V the SS=79 mV/decade were extracted. These values are near to the ideal value of 60 mV/decade and are in good agreement with the literature [98].

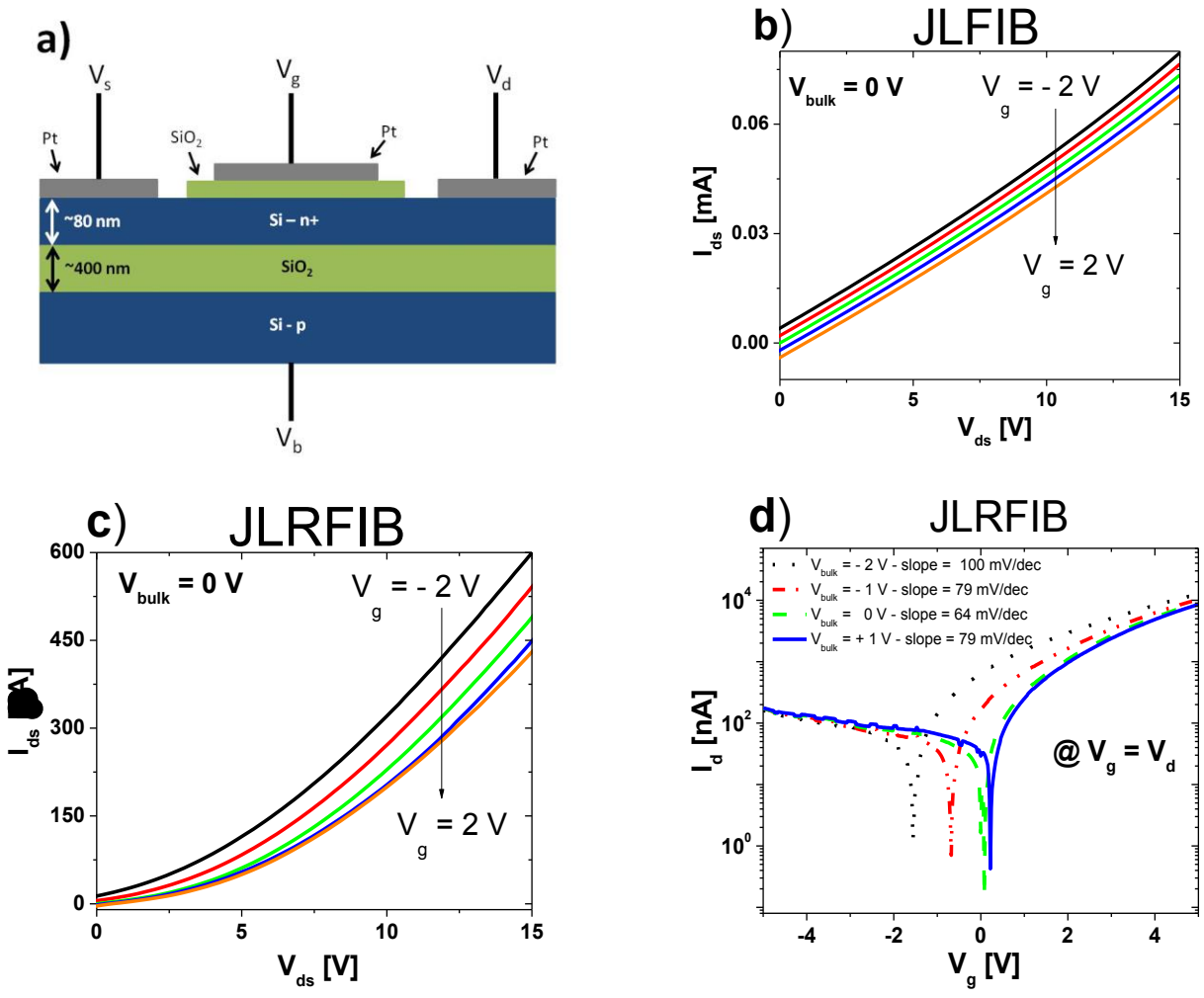


Figure 30 - a) Schematics of cross-section of JL device on SOI substrate. I_{ds} x V_{ds} measurements of b) JLFIB with 10 minutes of sintering time; c) JLRFIB with 20 minutes of sintering time; d) I_{ds} x V_{gs} measurements of JLRFIB with 20 minutes of sintering time. [***]

In order to understand the effect of Ga incorporation on Si, three dimensional (3D) junctionless transistor simulations were done using TCAD SILVACO software with the same width, length and Si height of JLRFIB device (Figure 31a) [102]. As the SiO_2 gate dielectric was deposited by GIS on FIB system, the charge density at the interface between Si/SiO_2 might be high, so we considered it around 10^{12} cm^{-2} for SILVACO processing. Net doping concentrations about $5x10^{18}$, $1x10^{19}$ and $5x10^{19}$ cm^{-3} were investigated. It is well known that SiNW structure can be damaged during the Si milling by Ga^+ FIB, resulting in some Ga^+ incorporation into Si and even Si surface amorphization [85-92]. For the same net doping (about $5x10^{18}$, $1x10^{19}$ and $5x10^{19}$ cm^{-3}), the effect of Ga^+ incorporation into Si decreases the maximum I_{ds} (see in Figures 31c, 31d and 31e) values (for V_{ds} = 15 V) from 40 μA to 1.3μA, from 101 μA to 10 μA, and from 723 μA to 481 μA, respectively. Moreover, the effect of Ga^+ incorporation into Si could change the area of depletion region inside the Si NW, which will modify the off state of JL device. Devices with net doping lower than $5x10^{19}$ cm^{-3} presents $I_{ds}xV_{ds}$ characteristic similar to the traditional planar MOSFET (Figures 31c and 31d), because transistors can achieve the saturation region, where the I_{ds} current is constant in relation to V_{ds}. However, devices with high Si NW channel net doping will not operate on saturation mode (the I_{ds} will not be constant), so distortions on $I_{ds}xV_{ds}$ characteristic can be expected (as shown in Figure 31e). Furthermore, as previously mentioned, the Ga^+ incorporation in JLRFIB is lower than in JLFIB devices. According to the JL simulations, higher I_{ds} levels in on-state can be achieved increasing the dopant concentration in SiNW, as shown in Figures 31c, 31d, 31e and 31f. This is related to the fact that residual Ga^+ are incorporated onto SiNW during the milling process. As a result, a dopant gradient region between the Si NW channel and source/drain will be formed, which conducts to a non-linear behavior (like a p-n junction) in the $I_{ds}xV_{ds}$ characteristic (Figures 31c, 31d, 31e and 31f) [93,103]. The effect of Ga^+ incorporation

can also be observed on the fabricated devices, where the current level on JLFIB (Figure 30b) in on-state is higher than on JLRFIB devices (Figure 30c). In addition, the carbon concentration (from the organometallic) in the Pt source/drain electrodes (Figure 29e) deposited by Ga^+ FIB decreases the electrodes workfunction and conducts to a Schottky-like electrical contact in source/drain regions (Figure 31f), or leading to that mentioned non-linear curves [93,103]. Replacing the Pt organometallic electrodes by PVD Al electrodes might reduce the non-ohmic contact for source and drain [12]. In summary, it can be concluded that:

i) $I_{ds}xV_{ds}$ characteristics showed that the nMOS JL devices are working like gated resistors;

ii) The comparison of the fabricated and simulated JL devices demonstrated that the Ga^+ incorporation during the SiNW formation process affects the $I_{ds}xV_{ds}$ characteristics. This results in an decrease on the net doping at the Si NW channel, which leads to distortions in $I_{ds}xV_{ds}$ characteristics;

iii) Non-ohmic contacts are related to carbon contamination (from the Pt organometallic) and results in an increase in $I_{ds}xV_{ds}$ distortions;

Finally, these results indicate that our fabrication method using Ga^+ FIB system can be used to obtain prototypes of JL devices. However, a good control of net doping level and Ga^+ incorporation into SiNW are the keys to improve the JL device performance.

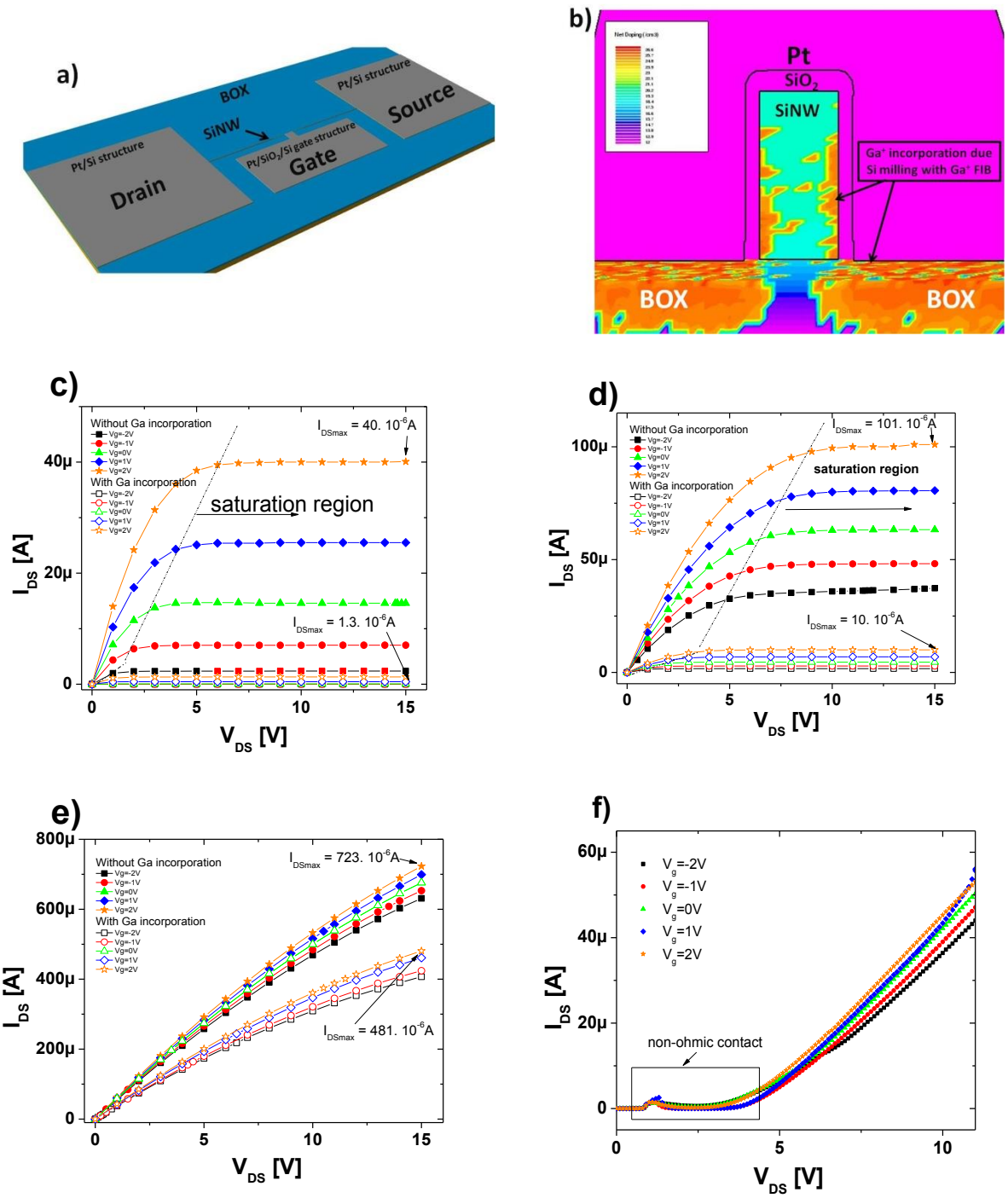


Figure 31 - a) 3D schematic of simulated JL transistor; b) cross-section of simulated gate structure showing with Ga^+ incorporation after Si milling by FIB; $I_{ds}xV_{ds}$ curves with: c) doping of $5x10^{18}$ cm^{-3}; d) doping of $1x10^{19}$ cm^{-3}; doping of $1x10^{19}$ cm^{-3} e) Ohmic contact and f) Schottky contact and Ga^+ incorporation.[***]

4.2.3 nMOS FinFET devices[†††]

FinFET and 3D MOSFET devices recently have gained much attention in micro- and nano-technology industries. The basic advantage of using a FinFET device is reduced short-channel effects and high output resistance values [109]. Also, FinFET devices are compatible with the CMOS fabrication process because of the potential for using high-k dielectrics and metal gate electrodes [28,29,45]. To fabricate the FinFET device, a focused ion beam (FIB) system was used to etch Si on the gate area in order to obtain widths in the range of 100 to 200 nm. SiO_2 was used as the gate dielectric, and 20 nm thick TiN and 200 nm thick Al were used as metal gate, drain and source electrodes.

Drain-source voltage (V_{ds}) by drain-source current (I_{ds}) and gate-source voltage (V_{gs}) by drain-source current (I_{ds}) curves were extracted using a Keithley analyzer 4200 SCS model. The measured drain characteristics (I_{ds} x V_{ds}) of the FinFET device indicates that the device works like a conventional nMOSFET transistor (Figure 32a). Also, the Early voltage (V_A) value of -14 V was extracted from Figure 32a, which indicates that the output resistance (r_{out}) is relatively high (since r_{out} is given by V_A/I_{ds}).

The gate-source voltage (V_{gs}) by drain-source current (I_{ds}) measurements are presented in Figures 32b and 32c. The threshold voltage (V_T) value of 0.5 V was extracted from gate characteristics (I_{ds} x V_{gs}) measurements, with drain-source voltage of 0.1V (FinFET in triode region). This V_T value corresponds to a metal work function of 4.2 eV (estimated using equation 7), which is suitable for nMOS applications. Furthermore, the extracted TiN EWF values from capacitors with Al/TiN/SiO_2/Si (will be presented in section 4.3.3) are between 4.0 eV and 4.3 eV,

[†††12]L.P.B. Lima, J.A. Diniz, C. Radtke, M.V.P. dos Santos, I. Doi, J. Godoy Fo, J. Vac. Sci. Technol. B, 31, 5 (2013).

which indicates that the extracted V_T value is in good agreement with the metal work function extracted from MOS capacitors. In addition, the threshold voltage is affected by the channel doping, the thickness of gate dielectric and defect at the TiN/SiO_2 and SiO_2/Si interfaces, as shown in equation (5). As mentioned in section 3.2.4, the SiNW width of the FinFET devices were defined by Ga^+ FIB milling and consequently, Ga incorporation into SiNW can be expected. However, ion implantation and rapid thermal annealing (RTA) processes were performed on FinFET samples after the FIB milling step. So, in the Si channel, the Ga ions can behave as:

i) Active dopant: Ga element is placed in group III of periodic table and therefore, is a p-type dopant in Si. Thus, in this case, the incorporated Ga ions will increase the channel doping, which increase the V_T value and reduce the channel mobility (μ). A reduction in μ decreases the transconductance (g_m) value; and

ii) Interstitial: in this case, the Ga incorporation will increase the defect at the SiNW surface.

Also, Figure 32c shows the transconductance (g_m) by gate-source voltage (V_{gs}). The transconductance (g_m) can be extracted from I_{ds} x V_{gs} measurements, since g_m is the relation between the channel current and the applied gate voltage: $g_m=\partial I_{ds}/\partial V_{gs}$. Literature reports that the g_m values for a FinFET device with width of 100 nm is between 200 μS and 300 μS [108]. The maximum g_m value of 0.193 μS was extracted from g_m x V_{gs} curve presented in Figure 32c. This extracted g_m value is three orders of magnitude lower than the g_m values presented by literature [108]. Thus, as discussed above, the Ga incorporation into SiNW can decrease the channel mobility and consequently, a reduction in g_m can occur. Therefore, the extracted low g_m value is related to the Ga incorporation into SiNW, as discussed above. In addition, it is possible to determine the subthreshold slope (SS) from the I_{ds} x V_{gs} measurements presented in Figure 32c. The ideal MOS

device presents a SS value of 60 mV/dec indicates low leakage current value and reduced interface states, mainly related with interface trapped charges. The extracted SS value was 580 mV/dec from Figure 32c, which is far from the ideal slope value. In general, SS values higher than the ideal case are mainly related to the defect at the SiO_2/Si interface [23,105-108]. As previously discussed, the Ga incorporation can increase the defect at the SiNW surface, which increases the SS value. So, the SS value of 580 mV/dec suggests that the gate MOS structure presents high defect density at the SiO_2/Si interface [105-108]. Moreover, lower values of SS can be achieved using thinner Si height and buried oxide layers [107]. Also, it is possible to evaluate the device performance through the g_m/I_{ds} x I_{ds} curve [110,111]. Basically, the g_m/I_{ds} ratio indicates how efficient is the current conversion into transconductance; meaning that high g_m/I_{ds} value results in high voltage gain [110,111]. Additionally, the channel inversion condition can be extracted from the g_m/I_{ds} x I_{ds} curve [110]. So, the g_m/I_{ds} maximum value of 5.8 V^{-1} was extracted from Figure 32d and indicates that the channel is at the moderate to strong inversion condition. Figure 32e presents the g_m/I_{ds} by $(V_{gs} - V_t)$ curves for V_{ds} values between 0.02 V and 2.0 V. Literature reports that below threshold voltage, the performance of a FinFET device is improved comparing to conventional planar MOSFET devices [105-112]. As discussed previously in section 1.4.2, short channel effects (SCE) are reduced on FinFET devices and therefore, the device performance is improved [112]. However, the maximum g_m/I_{ds} value of 17 V^{-1} was extracted for V_{ds} = 1.0 V (Figure 32e). This relatively low g_m/I_{ds} value indicates that our FinFET efficient is not high as expected [112]. This is related to the high serie resistance value, since large series resistance can degrade the g_m/I_{ds} value [112].

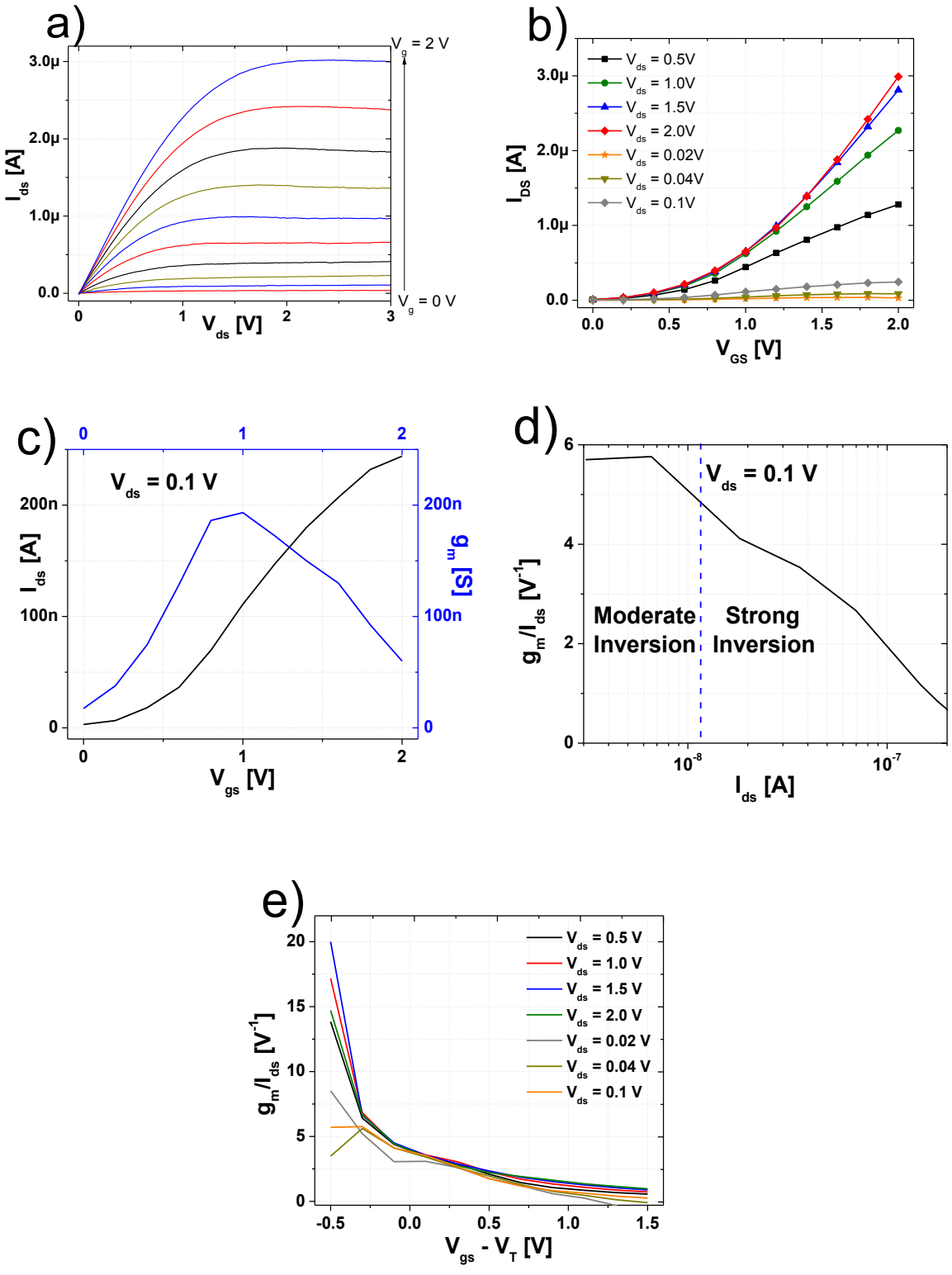


Figure 32 - a) I_{ds} x V_{ds}, b) I_{ds} x V_{gs}, c) I_{ds} x V_{gs} – g_m x I_{ds}, d) g_m/I_{ds} x I_{ds} and e) g_m/I_{ds} x (V_{gs} – V_t) measurements from FinFET device.[12]

In summary, from the transistor characteristics curve we can conclude that the nMOS FinFET device is working like a traditional MOSFET device. The Ga incorporation into SiNW affects the electrical parameters of the FinFET device. In addition, the extracted V_T value of 0.5 V corresponds to the metal work function of 4.2 eV for Al/TiN stack, which is suitable for nMOS applications. Therefore, we can conclude that the Al/TiN structure (obtained by PVD) is compatible with three dimensional CMOS technology.

4.3 Sputtering TiN Films‡‡‡

4.3.1 Introduction

As discussed previously in chapter 1, TiN films have been studied as gate electrodes in FinFETs and memory devices for 20 nm technology nodes and beyond [3-6,28,29,45]. TiN films can be obtained by several techniques, such as ALD and PVD. This section presents the detailed characterization of TiN layers obtained by sputtering (PVD). The process conditions are known to alter the electrical and structural properties of the film (resistivity, composition, dipole formation and metal work function). As these properties are interdependent, a reliable method to extract the metal work function is required, which would allow a detailed understanding of the effect processing conditions have on TiN film characteristics. So, the TiN effective work function was extracted from current-voltage (I-V) and capacitance-voltage (C-V) measurements from Schottky diodes and MOS capacitors, respectively. To characterize the TiN film composition, X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy were used. Electrical resistivity was extracted using four-probe technique.

‡‡‡[12]L.P.B. Lima, J.A. Diniz, C. Radtke, M.V.P. dos Santos, I. Doi, J. Godoy Fo, J. Vac. Sci. Technol. B, 31, 5 (2013).
[14]L.P.B. Lima, M.A. Moreira, J.A. Diniz, I. Doi, Phys. Status Solidi, 9, p. 1427 (2012).

4.3.2 TiN/Si samples for structural characterization

The electrical resistivity (ρ) value of 324 μΩ.cm was extracted from a 20-nm-thick TiN layer. Electrical resistivity values between 20 μΩ.cm and 600 μΩ.cm have been reported for TiN layers [12-14,39-57]. Film composition, stoichiometry and thickness of TiN layer can influence the electrical resistivity values [41]. The extracted ρ of 324 μΩ.cm indicates that the TiN layer is metallic; therefore, the TiN should be suitable for metal gate electrode applications on CMOS technology.

TiN layers crystalline structure was investigated by Raman spectroscopy analyses. Raman spectroscopy were performed in a NT MDT Integra Spectra system using the 633 nm lase line, from 50 cm^{-1} to 900 cm^{-1} with acquisition time of 3 seconds. Figure 33a presents the Raman spectra for TiN film. The peaks between 150 cm^{-1} and 350 cm^{-1} indicate the presence of transversal acoustic (TA) mode and longitudinal acoustic (LA) mode, which are related to Ti atoms vibrations near N vacancies [58-63]. In addition, peaks between 400 and 600 cm^{-1} are related to transversal optical (TO) and longitudinal optical (LO) modes, which are related to the N atoms vibrations near Ti vacancies [59-61]. So, the presence of acoustical and optical modes suggest the presence of Ti and N vacancies in the TiN film.

TiN chemical composition was investigated by XPS measurements. XPS was performed in an Omicron-SPHERA station using Al Kα radiation (1486.6 eV), the anode was operated at 225W (15 kV, 15 mA) and survey spectra were recorded with a 50 eV pass energy, although the Ti 2p region was recorded with a higher resolution (pass energy of 10 eV). The C 1s signal at 285 eV originating from adventitious carbon was used as an internal energy reference. All spectra were fitted assuming a Shirley background and lines were fitted using 70% Gaussian + 30% Lorentzian functions with set values of full width at half maximum for each line.

The Ti 2p region of the XPS spectra for a 20-nm thick TiN sample is shown in Figure 33b. Carbon 1s region is shown in Figure 33c, and Figure 33d shows the N 1s region of XPS spectra. The formation of TiO_2 and TiO_xN_y compounds on the sample surface were evidenced by the analysis of Ti 2p region [64,66]. As the TiN layers were deposited by DC sputtering in a N_2:Ar ambient, the formation of TiO_2 and TiO_xN_y compounds are not expected. Thus, exposing the TiN films to air can be responsible for the surface oxidation. Moreover, an N 1s region analysis confirms the TiN formation, component around 397 eV, however, a higher binding energy component is related to oxygen contamination [66]. Examination of the C 1s region also confirms higher binding energy components (the peak at 285 eV is related to adventitious carbon). They could be related to adsorbed species incorporated during sample preparation (C-O bonding) and/or to C incorporated in the TiN film during the deposition (C-N bonding) [66]. So, despite the superficial oxide formation, the XPS analyses evidence the clear formation of TiN.

In summary, the TiN film underwent surface oxidation due to air exposure (evidenced by XPS measurements) and presents Ti and N vacancies (as shown by Raman spectroscopy). However, the low electrical resistivity value (324 μΩ.cm) indicates that the TiN film should be metallic.

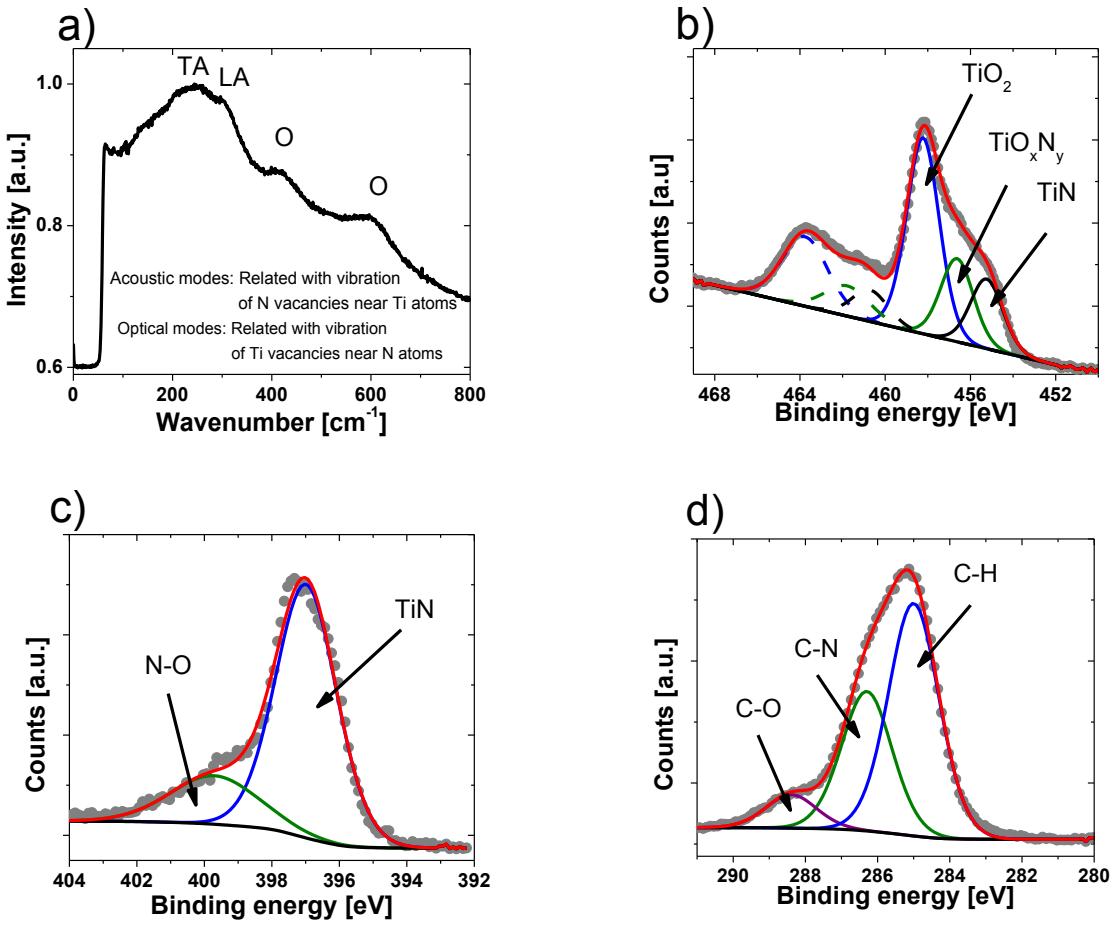


Figure 33 - a) Raman spectrum. Acoustic and optical modes are related to N and Ti vacancies, respectively. b) Ti 2p, c) N 1s, and d) C 1s regions of the XPS spectrum of the TiN film. Ti $2_{p3/2}$ components related to TiO_2, TiN_xO_y and TiN are indicated. N 1s and C 1s components assignment is discussed in the text. a.u. stands for arbitrary units.[12]

4.3.3 MOS capacitor electrical characterization

4.3.3.1 SiO_xN_y – MOS capacitor

The SiO_xN_y MOS capacitors were done with TiN/SiO_xN_y/Si structure, with 300-nm-thick TiN, 8-nm-thick SiO_xN_y and 300-nm-thick Al, following the procedure described in section 3.3.2.1. 1 MHz Capacitance-voltage (C-V) measurements were performed on TiN/SiO_xN_y/Si devices using a Keithley model 590 C-V and 4200 SCS analyzers. $1/C^2$ method was used for flat-band extraction from C-V data (see appendix 7.5) [65]. CVC, software develop by Hauser, was used for effective

charge density and TiN effective work function extraction (see appendix 7.5) [67]. Figure 34 presents the C-V characteristic of the MOS capacitor. Additionally, in Figure 34 it is possible to distinguish the accumulation (from -1.5 V until -1.1 V), depletion (from -1.1 V until -0.2 V) and inversion (from -0.2 V until 1.0 V) regions indicating that the device operates like a MOS capacitor, see appendix 7.5 [2,9,10]. From C-V data, effective charge densities between 10^{10} and 10^{12} cm^{-2} and flat-band voltages between -0.29 ± 0.01 V and -5.08 ± 0.01 V were extracted. For 20 minutes of FGA, the flat-band voltage of -0.29 ± 0.01 V, effective charge densities of about $6x10^{10}$ cm^{-2} and TiN effective work function about 4.65 ± 0.01 eV were extracted from C-V measurement shown in Figure 34. This value of TiN work function indicates that this film is suitable for nMOS applications on CMOS technology [8,68].

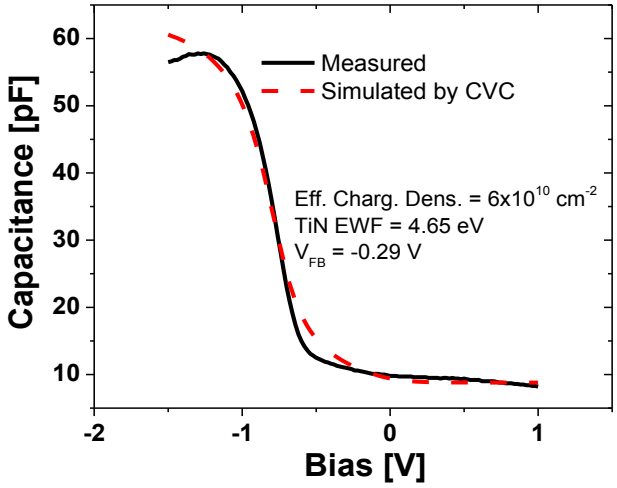


Figure 34 - 1MHz C-V characteristics of TiN/SiN_xO_y/Si specimens with 20 minutes of annealing.[14]

4.3.3.2 SiO_2 – MOS capacitor

MOS capacitors were fabricated with Al/TiN (200nm/20nm) or TiN (20nm) films as electrodes and 8-nm-thick SiO_2 as dielectric (see Figure 20 and section 3.3.2.2). These devices were sintered by a conventional furnace in forming gas at 450°C for 5, 10, 15, 20 and 30 minutes.

1 MHz Capacitance-voltage (C-V) measurements were performed on TiN/SiO_xN_y/Si devices using a Keithley model 590 C-V and 4200 SCS analyzers. $1/C^2$ method was used for flat-band extraction from C-V data (see appendix 7.5) [65]. CVC, software develop by Hauser, was used for effective charge density and TiN effective work function extraction (see appendix 7.5) [67].

C-V measurements of TiN/SiO_2/Si devices are shown in Figure 35a. Flat-band voltage values between -0.17 ± 0.02 V and -0.01 ± 0.01 V, effective charge densities between -1x10^{11} and -6x10^{11} cm^{-2}, and TiN effective work function values between 4.01 ± 0.01 and 4.21 ± 0.01 eV were extracted from TiN/SiO_2/Si capacitors. Figure 35b presents MOS capacitor C-V characteristics for Al/TiN/SiO_2/Si structures. For those devices the flat-band voltage, effective charge density and TiN effective work function values were about -0.18 ± 0.02 V and 0.04 ± 0.01 V, -3x10^{11} and -8x10^{11} cm^{-2}, 4.02 ± 0.02 and 4.31 ± 0.01 eV, respectively. Furthermore, in Figure 35 it is possible to recognize the accumulation, depletion and inversion regions for MOS capacitors with different times FGA. Also, the presences of those three regions indicate that the devices are working like a MOS capacitor, see appendix 7.5 [2,9,10].

In general, the extracted positive values of flat-band voltage and estimated negative values of effective charge densities indicate dipole variations between chemical bonds, such as Ti-O and Ti-N-O, at the TiN/SiO_2 interface. In addition, a reduction on TiN EWF value can be expected with the oxygen vacancy at the TiN/SiO_2 interface [19,25]. The O vacancy formation is explained by the fact that some O from the SiO_2 closer to the interface migrates to the TiN side and oxidizes it. The resulting SiO_2 near the interface is therefore further reduced with the creation of an O vacancy [19]. The extracted TiN EWF values from both MOS structures are lower than 4.40 – 4.50 eV (extracted from Schottky diodes, will be presented in section 4.3.4), indicating that the dipole at the metal/dielectric interface is being affected by the oxygen presence at the TiN/SiO_2 interface.

As a result lower TiN EWF values will be achieved on TiN/SiO_2/Si and Al/TiN/SiO_2/Si structures. Furthermore, since the TiN effective work function and effective charge density values were nearly the same on devices with and without the Al layer, it can be concluded that the oxygen surface contamination on TiN films does not affect much the electrical behavior of MOS capacitors. Moreover, the Al incorporation from Al cap layer on the TiN film could be related to the changes on TiN effective work function values [69]. However, a decrease on TiN work function is expected when there is Al diffusion into the TiN film (as discussed in section 1.4.1). The extracted TiN work function values for devices with and without an Al cap layer presented approximately the same shift, which indicates that, the thermal budget during FGA process, in this case, is not sufficient to diffuse Al through the TiN layer and reach the TiN/SiO_2 interface [69]. Thus, the dipole variation on the interface between TiN electrode and SiO_2 layer (due to chemical reactions between the metal and dielectric layers) could be responsible for the changes on flat-band voltage and TiN effective work function values. The extracted TiN effective work function values (between 4.02 ± 0.02 eV and 4.31 ± 0.01 eV), therefore, are suitable for nMOS applications on CMOS technology [8,68].

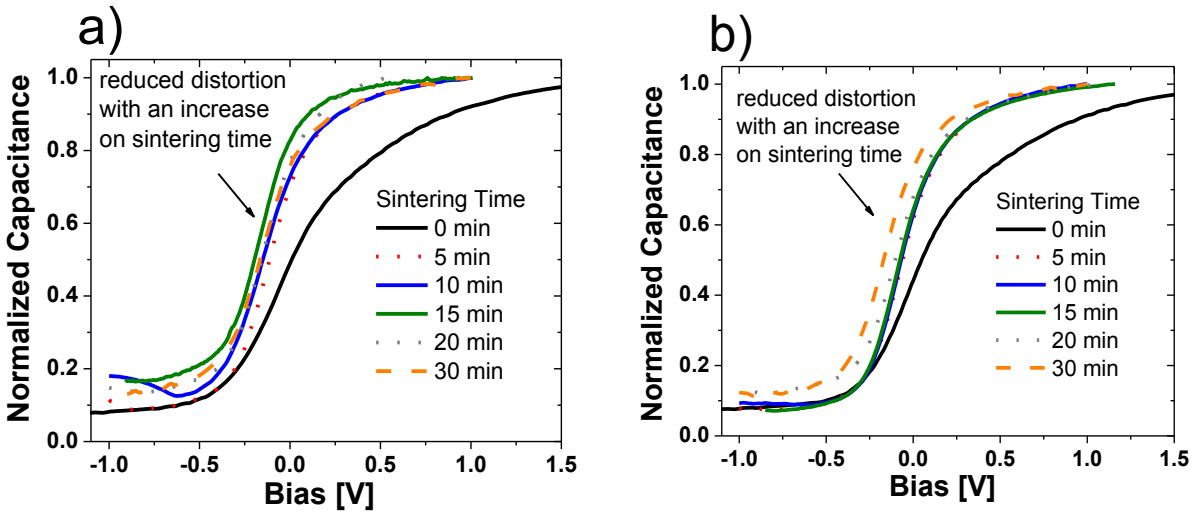


Figure 35 - 1 MHz C-V characteristics of a) TiN/SiO2/Si and b) Al/TiN/SiO2/Si structure, with a 20 nm thick TiN layer.[12]

4.3.4 Schottky diodes fabrication

Figure 36 presents the I-V measurements from Schottky diodes fabricated with structures Al/TiN/Si and TiN/Si. These devices were annealed in forming gas ambient at 450ºC for 5, 10, 15, 20 and 30 minutes. From I-V curves, the ideality factor (η) and TiN EWF values (Table 12) were extracted and the devices present the rectifier behavior, such as Schottky diodes [2,72]. The η and EWF parameters were extracted following the procedure discussed in appendix 7.4. Ideality factor values between 1.2 ± 0.1 and 2.2 ± 0.1 and TiN EWF values between 4.40 ± 0.01 eV and 4.50 ± 0.01 eV were extracted from Al/TiN/Si devices. For TiN/Si devices, the extracted η and TiN EWF values were between 1.0 ± 0.1 and 3.1 ± 0.1, and 4.40 ± 0.01 eV and 4.50 ± 0.01 eV, respectively. In general, variation in ideality factor values can be attributed to contact resistance, film composition and interface between the metal and semiconductor [13,70,71]. Also, as previously discussed, changes in TiN EWF are mainly related to the interface between TiN and Si. Thereby, from the comparison of the TiN EWF and η values extracted from Al/TiN/Si and TiN/Si devices

is it possible to estimate the influence of each effect on those parameters. Table 12 and Figure 37 show the extracted TiN work function values and the ideality factors for Schottky diodes.

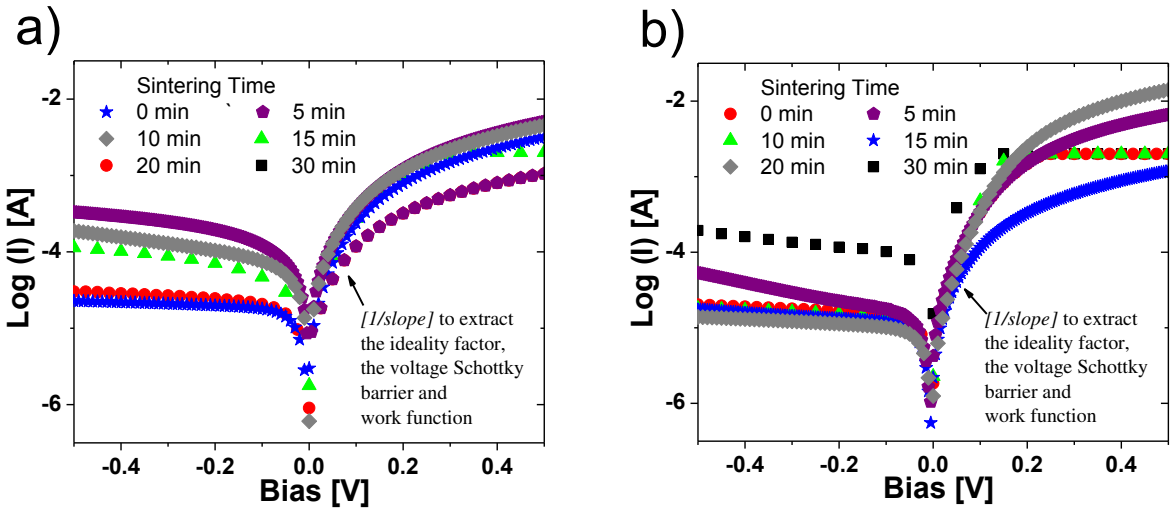


Figure 36 - I-V characteristics of (a) TiN/Si and (b) Al/TiN/ Si structure, with a 20 nm thick TiN layer.[12]

These results can be explained as follow:

i) Schottky diodes with TiN/Si structure presented wide ideality factor range, between 1.0 and 3.1; while for devices with Al/TiN/Si structures showed lower changes in η values, between 1.2 and 2.2. In general, the extracted ideality factors of 1.0 indicate the fabrication of an ideal devices [13,70-72]. However, η values higher than 1.0 indicate that the contact resistance of the diodes is high, even higher than 100 Ω [13,70-72];

ii) The high contact resistance for diodes without the Al cap layer can be related to the TiN surface oxidation, such as evidenced by XPS analyses (see Figure 33). As discussed in section 3.3.1 , the XPS analyses indicate, due to surface oxidation, the formation of TiO_xN_y, which presents dielectric characteristics. Thus, the contact resistance can be increased. In fact, devices with TiN/Si structure presented the highest

ideality factor values (η = 3.1 – Table 12), which confirms that the TiN surface oxidation increases the η values;

iii) On the other hand, no TiN oxidation occurs on Al/TiN/Si devices and consequently, lower contact resistance values can be achieved. So, ideality factor values lower (η = 2.2 – Table 12) can be expected for devices with Al cap layer (Figure 37);

iv) In addition, as previously mentioned, the film composition can affect the ideality factor value resulting in different η values [13,70,71]. The TiN film has Ti and N vacancies, as demonstrated by Raman spectroscopy measurement (Figure 33). Thus, during the FGA process, a rearrangement of Ti and N vacancies can occur, leading into different ideality factor values. This effect occurs on both devices, with and without Al cap layer; however, it is more evidenced on devices with Al cap layer (see Figure 37), since no TiN surface oxidation occurred on these devices. As a result, changes in ideality factor value are mainly related to Ti and N vacancies rearrangement;

v) Moreover, the Ti and N vacancies rearrangement can also modify the TiN/Si interface composition and therefore, affects the TiN EWF value [13,70,71]. Literature reports that a Ti-rich interface decreases the EWF to nMOS values, while N-rich interface increases the EWF to pMOS values [25,30]. The extracted TiN EWF values were between 4.40 eV and 4.50 eV, which suggests that the rearrangement of Ti and N vacancies are occurring during the sintering process. An example that clearly confirms this effect of Ti and N on TiN EWF value is for Al/TiN/Si structure with 20 and 30 minutes of FGA. For this case, the values of η = 1.2 and 4.40 eV, and η = 1.2 and 4.50 eV, were extracted for 20 and 30 minutes of FGA, respectively. Those values indicate that the vacancies rearrangement are occurring resulting mainly in changes of TiN/Si

interface, since the η values are the same for both devices. Therefore, various TiN EWF values are expected, due to different TiN/Si interfaces;

vi) In addition, for Al/TiN/Si devices different η values were extracted for approximately the same TiN EWF, meaning that the Ti and N vacancies rearrangement is occurring mainly in the bulk of TiN layer and the TiN/Si interface is slightly being affected. The same effect is observed for devices without Al cap layer.

Table 12 – Ideality factor and TiN EWF values extracted from Schottky diodes.

TiN/Si structures			**Al/TiN/Si structures**		
FGA [min]	**Ideality Factor**	**TiN EWF [eV]**	**FGA [min]**	**Ideality Factor**	**TiN EWF [eV]**
0	3.1 ± 0.1	4.50 ± 0.06	0	2.2 ± 0.1	4.46 ± 0.02
5	1.6 ± 0.1	4.49 ± 0.03	5	1.8 ± 0.1	4.50 ± 0.03
10	1.3 ± 0.1	4.48 ± 0.01	10	1.7 ± 0.1	4.47 ± 0.01
15	1.2 ± 0.1	4.48± 0.02	15	1.3 ± 0.1	4.48 ± 0.03
20	1.1 ± 0.1	4.48 ± 0.02	20	1.2 ± 0.1	4.40 ± 0.01
30	1.0 ± 0.1	4.49 ± 0.03	30	1.2 ± 0.1	4.50 ± 0.01

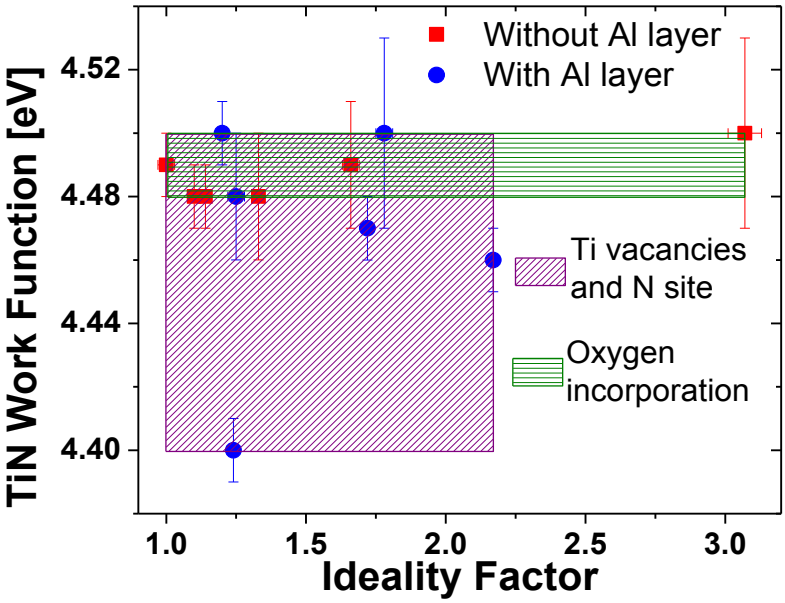


Figure 37 - TiN effective work function and ideality factor values for devices with structures Al/TiN/Si and TiN/Si from Schottky diodes.[12]

In summary, Ti and N vacancies rearrangement on the TiN layer can influence TiN work function values, mainly for electrodes with an Al cap layer. Also, TiN surface oxidation can cause the high amplitude variability of ideality factor, mainly for electrodes without an Al cap layer. Additionally, the extracted TiN effective work function values from Schottky diodes had demonstrated that these films are suitable for CMOS technology applications [8,68].

4.3.5 Effect of dipole variations

A schematic view of MOS capacitors and Schottky diodes, with and without Al cap layer, fabricated in the same wafer is shown in Figure 38. As discussed previously (see section 1.1), the traditional method to extract the gate metal work function is based on C-V measurements of MOS capacitors with different thickness of gate dielectric in different samples, which can incorporate

different charge densities at dielectric/semiconductor interface. With this an additional error can induce in the work function extraction. So, we propose an alternative method for work function extraction based on current-voltage I-V and C-V measurements on Schottky diode and MOS capacitors, respectively, fabricated on the same substrate. One advantage of our method is that the same parameter, in this case TiN EWF, is extracted from two different methods: MOS capacitors (see appendix 7.5) and Schottky diodes (see appendix 7.4). Another advantage is that the both devices were fabricated on the same substrate, which can reduce the defect incorporation on Si surface. Thus, with one substrate, it can be possible to extract the work function with two different measurements. Therefore, this method can be used to study the influence of dipole at metal/dielectric interface and film composition on TiN EWF. Figure 38a presents a schematic cross-section view of MOS capacitors and Schottky diodes without Al cap layer and it indicates the oxygen incorporation on the TiN film surface. The presence of Ti and N vacancies in bulk TiN electrode and dipole variations at the TiN/SiO_2 interface are shown in Figure 38a [73-75]. For devices with the Al cap layer, the TiN surface oxidation was prevented, as shown in Figure 38b, because the Al is used to avoid the oxygen contamination. Moreover, the dipole variations at the TiN/SiO_2 interface are included in the MOS capacitor schematics (Figure 38b).

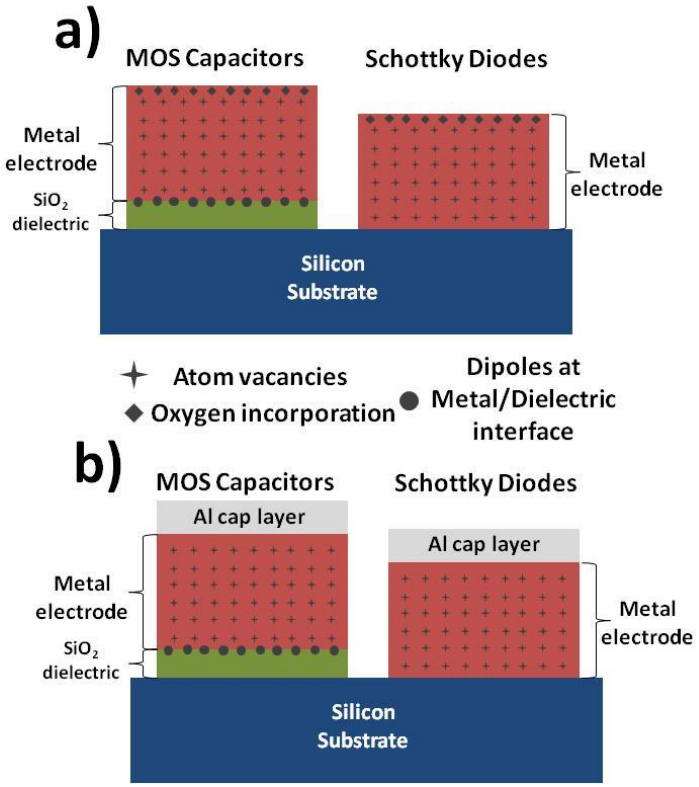


Figure 38 - The schematic views of MOS capacitors and Schottky diodes, without Al cap layer, respectively, and with Al cap layer.

As discussed previously, positive values of flat-band voltage and negative values of effective charge density indicate that dipole variation at the TiN/SiO_2 interface can occur [73-75]. On Schottky diodes there are no effect of dipole moment variation related to the TiN/SiO_2 interface, since there is no dielectric on diodes. Then, with the comparison between the TiN work function extracted from MOS capacitors ($WF_{capacitor}$) and Schottky diodes (WF_{diode}), is possible to estimate the dipole effect at the TiN/SiO_2 interface [13]. Equation (14) presents the formula to estimate the variation of the dipole moment at the TiN/SiO_2 interface, qΔTiN/SiO_2 term:

$$q\Delta_{TiN/SiO2} = W_{Fdiode} - W_{Fcapacitor} \quad (14)$$

This method allows us to estimate the effect of dipole variation, providing an effective tool for work function engineering [13]. The effect of Ti and N vacancies rearrangement during the sintering process is considered on both devices (MOS capacitors and Schottky diodes – see Figure

38) [13]. Additionally, the effect of oxygen surface contamination on TiN layer can also be compared with devices with and without the Al cap layer (see Figure 38).

Figure 39 presents the $q\Delta_{TiN/SiO2}$ term values (calculated by Eq. (14)) for devices with TiN electrodes as related to annealing times. Devices with and without an Al cap layer follow the same trend, but devices with Al cap layer lowers the dipole variation $q\Delta_{TiN/SiO2}$ by 0.1 eV. So, TiN surface oxidation may influence the dipole variations at the TiN/SiO_2 interface, and consequently, the TiN effective work function values. In addition, oxygen incorporation onto the TiN film surface could increase the distortion of C-V characteristics (see Figure 35) and the series resistance on MOS capacitors. Thus, these effects are related to:

i) For sintering times between 0 and 20 minutes, one higher dipole variation between chemical bonds, such as Ti-O and Ti-N-O, at the TiN/SiO_2 interfaces can occur, because the chemical reactions between Ti, O and N atoms at the TiN/SiO_2 interface can be occurring during this period [73-75]. Furthermore, previously discussed, the presence of O vacancy at the TiN/SiO_2 interface decreases the TiN EWF value [19,25]. With this, lower TiN EWF values can be expected on MOS capacitors, which increases the $q\Delta_{TiN/SiO2}$; and

ii) For a sintering time of 30 minutes, it can be assumed that chemical reactions are complete and changes of $q\Delta_{TiN/SiO2}$ are saturated, leading to a better adjustment at the interface region with minimal variation in dipoles between chemical bonds.

In summary, the dipole variations at the TiN/SiO_2 interface are occurring during the sintering process on both devices, with and without an Al cap layer. At the end of the sintering process, dipole variation can be decreased.

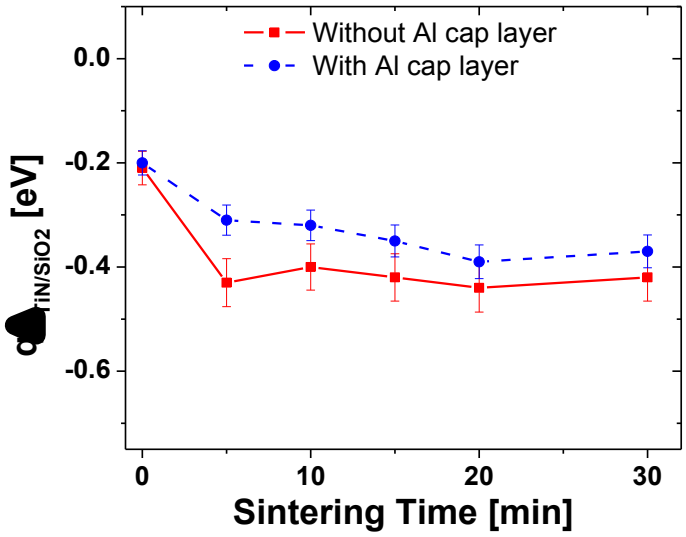


Figure 39 - $q\Delta_{TiN/SiO2}$ term calculated by Eq. (9) for devices with TiN electrodes with and without an Al cap layer.[12]

4.4 Atomic Layer Deposition TiN Films§§§

4.4.1 Introduction

As mentioned in chapter 1, current MOSFET devices are using TiN as metal gate electrode. TiN film properties, such as conductivity and work function are important elements in CMOS technology [13,28,29,34,35,45]. Literature reports TiN work function values between pMOS and mid-gap values [3-6,13,29]. Atomic layer deposition (ALD) and physical vapor deposition (PVD) can be used for TiN deposition. This section presents the characterization of TiN films obtained by ALD. Nowadays ALD system is being widely used for TiN deposition due to the requirement of conformal layers for 3D channel structures, like tri-gates and FinFET's. As discussed previously in section 1.4, TiN films obtained by ALD usually present stoichiometric composition and

§§§ L.P.B. Lima, H.F.W. Dekkers, J.G. Lisoni, J.A. Diniz, S. Van Elshocht, S. De Gendt, J. App. Phys., 115, p.074504 (2014).

therefore, EWF values between 4.7 eV and 5.1 eV (adequate for pMOS applications). However, nMOS EWF values (between 4.1 eV and 4.4 eV) can be achieved by doping the TiN film with different elements (such as Al and N) [5,25,36,37]. Literature reports have shown that the addition of Al ions into TiN layer can significantly change the TiN EWF [5,38-40]. The amount of Al ions at the interface between high-k dielectric and TiN layer will determine the shift of the metal gate work function and a decrease of 0.60 eV on TiN EWF can be achieved using Al diffusion approach [32]. In this work, the TiN EWF value is decreased by the incorporation of Al into TiN metal electrode using an AlN layer between HfO_2 and TiN films as an alternative material for Al diffusion source. The usage of AlN to control the metal gate EWF has been reported as a promising approach for work function engineering for CMOS technology [46-48]. In addition, the HfO_2/AlN stack is thermally stable at high temperatures [46]. Aluminum nitride films are usually obtained by PVD, ALD and sputtering depositions [47-49]. In this PhD work, the HfO_2, AlN and TiN layers were deposited *in situ* by an ALD system in order to study the influence of Al diffusion at the interface between HfO_2 and TiN to lower the metal gate EWF. Thermally stability control of Al diffusion into TiN and conformality are advantages of using HfO_2/AlN/TiN stack deposited by ALD. In contrast, TiAl is today only reported to be deposited using PVD, which lacks conformal deposition in trenches and fin structures. Therefore, the usage of AlN/TiN stack is more suitable for 3D technology, such as finFET's. The blanket ALD films were characterized using XRR (to evaluate the film thickness), XPS and SIMS (to investigate the Al diffusion into TiN film). TiN EWF was extracted C-V measurements from MOS capacitors.

4.4.2 Thickness, composition and Al diffusion studies

Figure 40a shows the growth of AlN layer on top of HfO_2 and TiN. The growth per cycle (GPC) was obtained using the XRR thickness. After 50 cycles, the growth behavior of AlN layer

is independent of the surface either when growing onto HfO_2 or TiN. Indeed, the growth is almost linear with GPC's of 0.042 nm/cycle.

XPS was performed using Al K_α X-ray source (1486.6 eV) with a spot size of 400µm and the film sputtering was performed using Ar^+ ions with energy of 500 eV. SIMS measurements were done using 500 eV O_2^+ ion beam with angle of 44º. From XPS analysis, the AlN compound formation is confirmed by the presence of Al 2p and N 1s peaks (see Figure 40b). The Al:N ratio was approximately 1.4 for 1.2 nm thick AlN, which indicates that the AlN layer contains more Al than N. In addition, a native oxidation of AlN was observed, which results in a distorted stoichiometry ratio. This can be explained because part of the Al is oxidized to Al_xO_y. Figure 40c presents the SIMS measurement on a TiN/AlN/HfO_2/SiO_2/Si sample after 20 minutes of forming gas anneal. For this TiN/AlN/HfO_2 structure, two layers of TiN were used:

i) The first TiN layer was deposited *in situ* after HfO_2 and AlN (2 nm thick) by ALD;

ii) Second TiN film was deposited on the top of the ALD TiN *ex-situ* by PVD.

The Al diffusion profile (related to the right axis on Figure 40c) was quantified by SIMS of Al implantation experiments ($2x10^{13}$ atoms/cm^2 at 5 keV). These measurements had confirmed the presence of ^{27}Al inside the TiN layer, which indicates the Al diffusion into TiN layer. Additionally, the presence of ^{48}Ti evidences that the mixing does not entirely consume the TiN films. Also, with the ^{27}Al presence into TiN layer it is possible that a reaction between Al and TiN can occur resulting in a TiAlN compound formation [69].

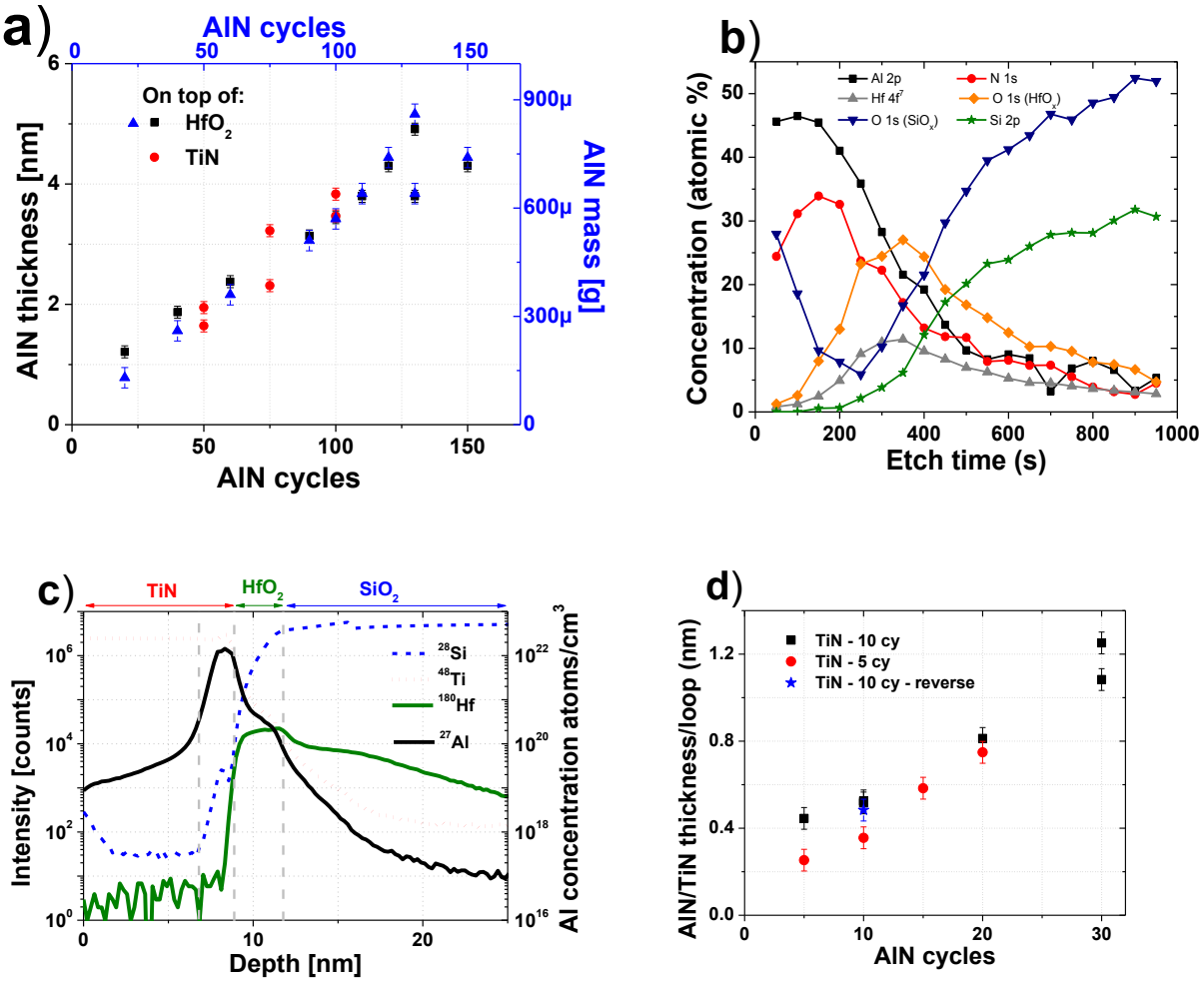


Figure 40 – a) AlN thickness and AlN mass versus AlN cycles of AlN/HfO_2/SiO_2/Si and AlN/TiN/SiO_2/Si structures; b) XPS measurement on 1.2 nm of AlN (on top of HfO_2); c) SIMS measurement on a structure TiN/AlN/HfO_2/SiO_2/Si after forming gas anneal; d) AlN/TiN thickness versus AlN cycles for TiN/AlN/HfO_2/SiO_2 laminate. TiN-10cy-reverse means that the first layer of the laminate is TiN instead of AlN.[§§§]

Regarding to the AlN/TiN laminate stacks (see section 3.4), each loop sequence of the AlN/TiN laminate stacks were done with "x" cycles of AlN (with "x" between 5 and 30) and with "y" cycles of TiN deposition (with y=5 and y=10). Figure 40d shows the AlN/TiN laminate growth per loop for fixed TiN cycles (5 and 10 cycles) and varying the AlN cycles. The growth of AlN/TiN laminate per loop presents a linear growth. Thus, the growth of TiN and AlN is almost the same on both structures, as suggested by a nearly similar growth rate per loop for samples with 5 and 10

cycles of TiN, however, for thicker TiN (obtained with 10 cycles) the growth rate is slightly higher. Nevertheless, as previously concluded from Figure 40a, the AlN/TiN growth seems to be independent of the first layer, since there is no significant difference on these laminate growth if the first layer of this stack is a TiN or AlN.

4.4.3 Electrical measurements

1 MHz Capacitance-voltage (C-V) measurements were performed on MOS capacitors using a Keithley model 590 C-V, 4200 SCS and Agilent 4284A LCR analyzers. The electrical parameters were extracted using the method described in appendix 7.5. Table 13 presents MOS capacitor structure, name and the extracted TiN EWF values. As described in section 3.4, the capacitors were fabricated on p-type Si (100) with SiO_2 and a 2-nm-thick HfO_2 as an interfacial layer and dielectric, respectively. Various SiO_2 thicknesses, between 1.4 and 5.7 nm, were achieved using the slant etch procedure [49]. Therefore, different equivalent oxide thickness (EOT) values can be expected due to several dielectric stack (SiO_2/HfO_2) thicknesses. The EOT values were directly extracted from C-V measurements. All the samples presented the same EOT values, between 1.1 nm and 6.2 nm (see section 7.5).

Table 13 – Sample name, structure and extracted metal EWF. [§§§]

Sample name	**Structure**	**Metal EWF (eV)**
Pt ref	$Pt/HfO_2/SiO_2/Si$	5.60 ± 0.01
TiN ref	$Pt/TiN/HfO_2/SiO_2/Si$	5.05 ± 0.01
Al dif.	$Pt/TaN/TiN/HfO_2/SiO_2/Si$	4.68 ± 0.02
TiN/TiAl	$Pt/TiN/TiAl/TiN/HfO_2/SiO_2/Si$	4.13 ± 0.01 – 3.96 ± 0.03
TiN/AlN	$TiN/AlN/HfO_2/SiO_2/Si$	5.01 ± 0.01 – 4.78 ± 0.01
Laminate	$TiN/AlN/HfO_2/SiO_2/Si$ - laminate	4.85 ± 0.01 – 4.59 ± 0.01

As mentioned in section 3.4 and shown in Table 11, MOS capacitors with Pt/HfO_2/SiO_2/Si and Pt/TiN/HfO_2/SiO_2/Si structures were used for EWF extraction routine calibration. The Pt EWF value of 5.60 eV was extracted from Pt ref. sample, and 5.05 eV is the extracted TiN EWF value from TiN ref. sample. Both metal EWF values are in good correspondence with values reported in the literature [37,76]. Furthermore, literature reports that for an N-rich TiN/HfO_2 interface, with N atoms replacing half of the O atoms at the HfO_2 side, the EWF value should be around 5.03 eV [25]. So, the EWF value extracted from the TiN ref. sample might be an indication that the TiN/HfO_2 interface is an N-rich interface, probably with N atoms replacing some O atoms at the dielectric side [25]. Table 13 presents the extracted metal EWF values for MOS capacitors with structures described in section 3.4.

The TiN EWF value of 4.68 eV was extracted from Al dif. (with Pt/TaN/TiN/HfO_2/SiO_2/Si structure) device (see Table 13). As previously mentioned the presence of Al at the TiN/HfO_2 interface decreases the dipole at that interface and therefore, lowers the EWF value. For this sample, as shown in Figure 41, the Al needs to diffuse through TaN and TiN layers to reach the TiN/HfO_2 interface [25]. Despite of the fact that TiN film presents a diffusion barrier of 2.42 eV for Al diffusion [25], a TaN layer was used to control the amount of Al diffused into TiN film. With this, some Al might be able to reach the TiN/HfO_2 interface and consequently, decrease the EWF value. This hypothesis is confirmed by the extracted EWF value of 4.68 eV, which is lower than the EWF value of 5.05 eV extracted from the TiN ref. sample. So, due to the extracted TiN EWF value it is possible to conclude that the Al can be at the TiN/HfO_2 interface, however, experimental measurements to confirm and quantify the exact Al concentration at this interface is lacking. Furthermore, using TiAl as an Al diffusion source, a reduction of 0.60 eV on TiN EWF can be achieved, and so, low TiN work function values around 4.1-4.2 eV can be obtained [5].

However, in this case the TiN work function shift is mainly related to the amount of Ti and Al at the TiN/HfO_2 interface (Figure 41). Literature reports that an Ti-rich TiN/HfO_2 interface presents nMOS work function values [25,30]. So, the usage of TiAl can introduce Al atoms (by Al diffusion) and increase the Ti concentration at the TiN/HfO_2 and therefore, decrease the TiN EWF value. This is evidenced by the extracted EWF values from TiN/TiAl devices; with 2 nm and 5 nm of TiAl the TiN EWF values were 4.13 eV and 3.96 eV, respectively. The amount of Ti and Al is dependent on TiAl layer thickness, meaning that thicker films might present more available Ti and Al atoms to diffuse until the TiN/HfO_2 interface. Thus, thicker TiAl layer results in a higher TiN EWF decrease, as evidenced by the EWF extracted from TiN/TiAl samples. Moreover, from the TiN work function values extracted from Al dif. and TiN/TiAl devices show that the TiN work function decreases with aluminum incorporation in metal layer. The different reduction on TiN EWF, 0.37 eV for Pt/TaN/TiN/HfO_2/SiO_2/Si films and 1.09 eV for Pt/TiN/TiAl/TiN/HfO_2/SiO_2/Si structures are related to different Al diffusion mechanisms. On Pt/TaN/TiN/HfO_2/SiO_2/Si structure, the Al needs to diffuse through the TaN and TiN layers to reach the TiN/HfO_2 interface (Figure 41). On the other hand, the Pt/TiN/TiAl/TiN/HfO_2/SiO_2/Si the Al needs to diffuse through only the bottom TiN layer to reach the TiN/HfO_2 interface (Figure 41). Additionally, the TiAl can increase the Ti and Al concentration at the interface between the metal electrode and high-k dielectric, which enhances more the tuning effect, as previously discussed. Hence, lower TiN EWF values can be obtained with TiAl/TiN approach.

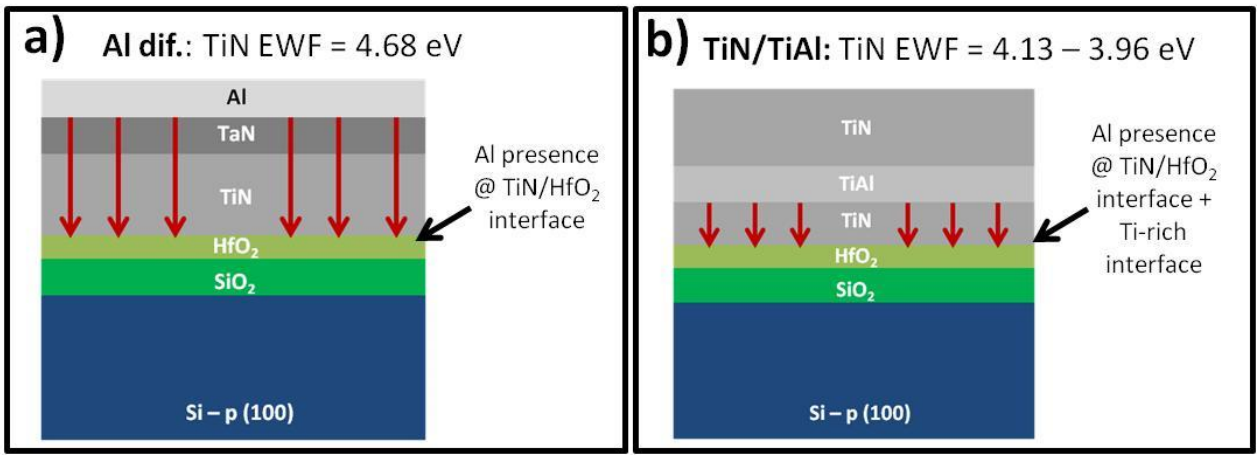


Figure 41 – Schematics for Al diffusion into TiN layer on a) Al dif and b) TiN/TiAl samples. The red arrows represent the Al diffusion path.

For TiN/AlN capacitors it can be expected that a reduction of TiN EWF value with an increase on AlN thickness occurs. Figure 41a shows the TiN EWF *versus* AlN thickness for TiN/AlN devices. It has been observed that the TiN effective work function can be decreased with an increase on AlN thickness. This effect is similar to what has been reported for the case of pure Al diffusion [69]. In fact, as previously discussed, the Al presence at the TiN/HfO_2 interface results in an additional dipole moment formation, resulting in lower values for TiN EWF [25,37]. Basically, this Al at the TiN/HfO_2 interface can: (i) go to TiN side, (ii) go to HfO_2 side or (iii) segregate at the interface. Literature reports that TiN layer presents a negligible diffusion barrier for Al diffusion [25]. Additionally, for diffusion into HfO_2 layer, a barrier of 2.16 eV is found by Al atoms, while a barrier of 0.22 eV is found for diffusion towards the interface (Figure 42b) [25]. Therefore, it can be expected that Al is mainly located at the TiN/HfO_2 interface. SIMS measurements (Figure 40c) show that the largest amount of Al remains at the TiN/HfO_2 interface or near this region inside TiN layer; confirming the hypothesis stated above. In addition, the EOT values was not increased, value between 1.1 nm and 6.2 nm, which indicates that the Al is mixing

with TiN layer [37]. Moreover, it has been observed that the thicker AlN layer results on the lowest TiN EWF value. However, the effect of Al at the TiN/HfO_2 interface is reduced for thicker AlN layers, since the extracted values of TiN EWF for thickness of AlN films of 3.2 nm (TiN EWF=4.79 eV) and 4.2 nm (TiN EWF=4.78 eV) did not change much. The Al and N concentrations are increased with thicker AlN layers. As discussed previously, N-rich TiN/HfO_2 interface presents pMOS work function value [25,30]. Thus, an increase on N concentration at the TiN/HfO_2 interface might reduced the effect of the Al presence at the same interface. Therefore, the TiN EWF value might not change even with thicker AlN layers, as observed for samples with AlN thickness of 3.2 nm and 4.2 nm (Figure 42a).

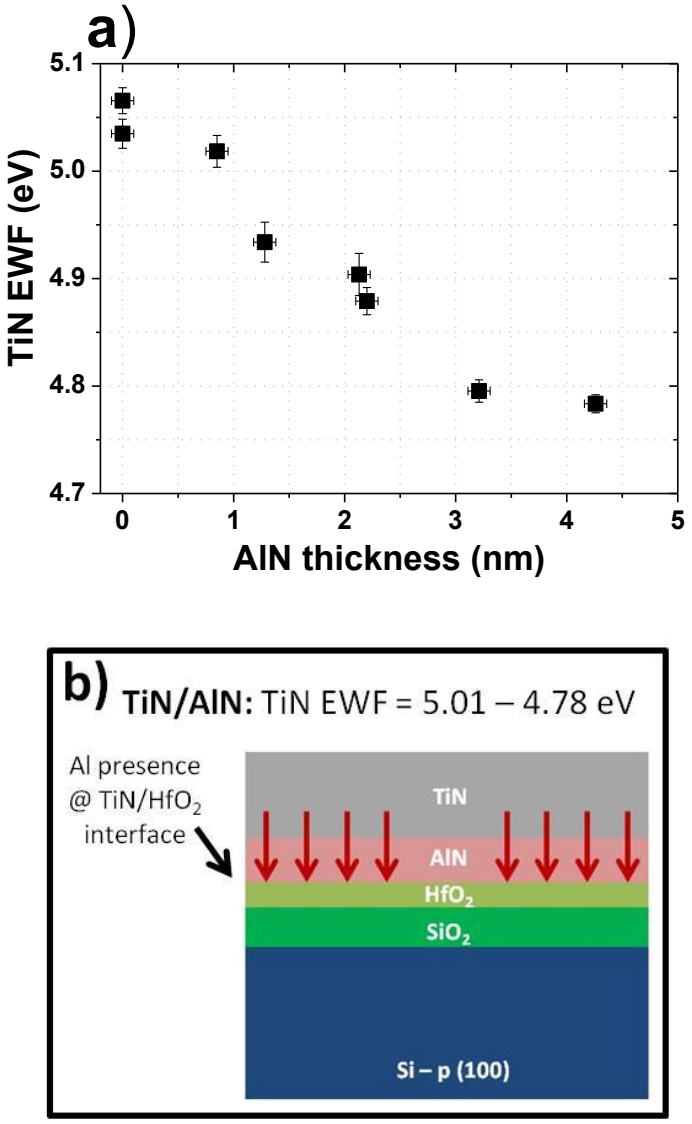


Figure 42 – a) TiN EWF versus the AlN thickness for TiN/AlN/HfO_2/SiO_2/Si structures[§§§]; b) Al diffusion schematics for TiN/AlN samples. The red arrows represent the Al diffusion path.

Figure 43a presents TiN EWF *versus* AlN/TiN ration for the capacitors with the TiN/AlN laminate structures. The AlN/TiN laminate ratio consists on the ratio of AlN and TiN cycles on laminate structure, for example the AlN/TiN ratio of 1 presents the same number of cycles for AlN and TiN depositions, while the AlN/TiN ratio of 3 presents the three times more cycles for AlN than TiN cycles. In addition, increasing the AlN/TiN ratio, the amount of Al is also increased due

the higher thickness of AlN layer, and care was taken that the same laminate thickness was obtained for different TiN and AlN cycles. So, as it can be seen in Figure 43a, the extracted values of TiN EWF decrease with higher AlN/TiN ratio values, resulting in an increase of AlN thickness per loop (since the number of TiN cycles is fixed for all AlN/TiN laminate depositions). This effect is analogous to the EWF reduction with TiN/AlN samples presented in Figure 42a, where the Al presence at the TiN/HfO_2 interface results in lower values for TiN EWF [25,37]. Thus, the lowest TiN EWF value of 4.59 eV was extracted from the laminate device with thicker AlN/TiN stack, which represents a reduction of 0.19 eV on TiN EWF in comparison with the lowest work function values extracted from AlN/TiN stack (Figure 42a). This indicates that the laminate deposition is more effective for TiN EWF tuning. In fact, in the laminate samples Al needs to diffuse through a thin layer of TiN to reach the TiN/HfO_2 interface and consequently, decreasing the TiN EWF value (Figure 43a). Also, N atoms can diffuse through the TiN layer and reach the metal-dielectric interface, which will increase the TiN work function value. However, the additional N (introduced by the AlN layer) might be accommodated by the TiN bulk layer rather than diffuse to the TiN/HfO_2 interface. With this, less N will reach the metal/dielectric interface. Then, the effect of Al presence at the TiN/HfO_2 interface is not suppressed by a N-rich interface, as observed for AlN/TiN samples (Figure 42a). Thus, lower values of TiN EWF can be expected for AlN/TiN laminate structures. The lowest TiN EWF value of 4.59 eV was extracted from the laminate device with thicker AlN/TiN stack, which confirms that the laminate deposition is more efficient for Al mixing with TiN layer, as expected. Additionally, for the laminate devices with AlN as first deposited layer, the extracted TiN work function presented slightly lower values than for laminate devices with TiN as first layer. On TiN/AlN/HfO_2 structures the Al is actually already at the TiN/HfO_2 interface, while on AlN/TiN/HfO_2 structures the Al needs to diffuse through the TiN

layer to reach that metal-dielectric interface (Figure 43b). As a result, lower values for TiN/AlN/HfO_2 structures can be expected.

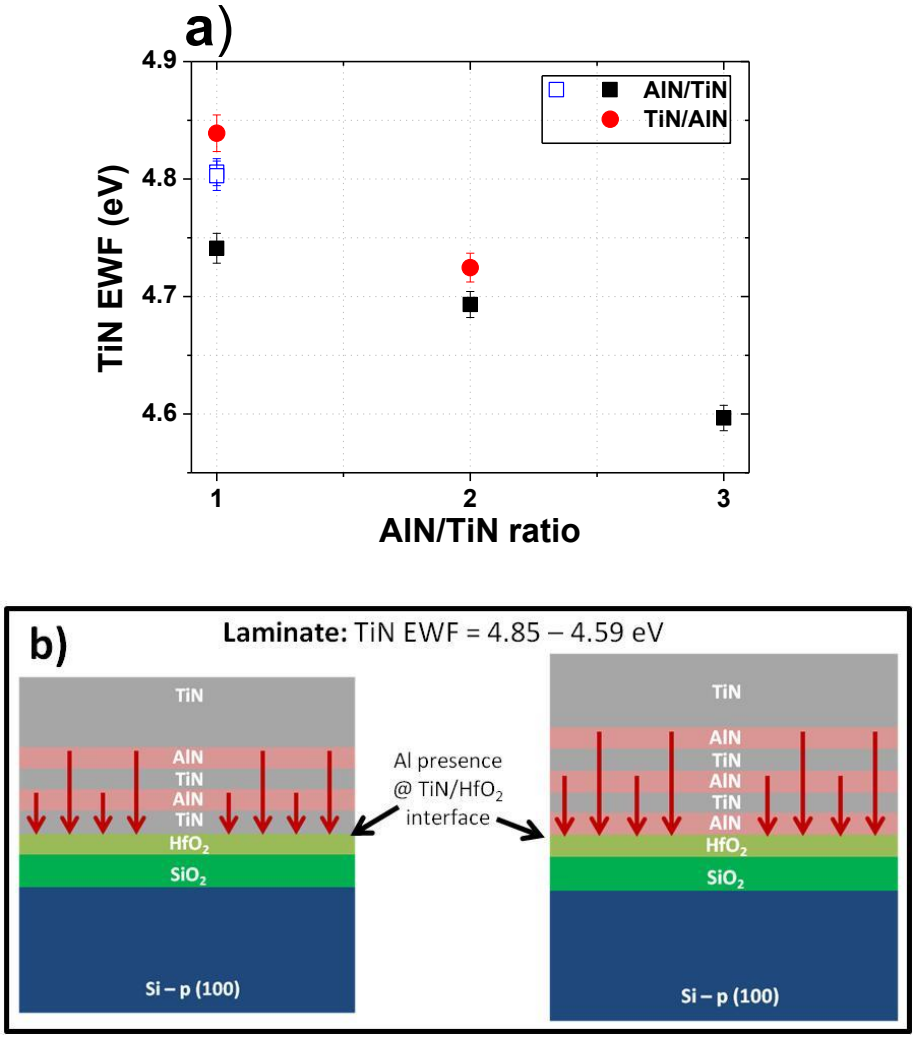


Figure 43 – a) TiN EWF versus the AlN/TiN ratio for laminate devices. The open symbols are for laminate structures deposited with 5 loops. §§§ b) Al diffusion schematics for Laminate samples. The red arrows represent the Al diffusion path.

In summary, it can be concluded that the Al diffuses through TiN layer, resulting in a decrease on metal electrode work function value. Therefore, low values for TiN EWF can be achieved using AlN as an Al diffusion source. A decrease of 0.26 eV and 0.45 eV on TiN work function value were extracted from AlN/TiN stack and AlN/TiN laminate stack, respectively. So, the AlN/TiN

laminate structures have been shown to be more effective for Al mixing into TiN layer and consequently, reducing the TiN work function than just increasing the AlN thickness. In addition, the mixing of Al into TiN suggest that Al can react with TiN and form TiAlN compounds, however, a physical analysis is required to confirm this hypothesis [69]. Moreover, all the TiN EWF values are applicable for CMOS technology [8,68].

4.5 PVD and ALD TiN - Summary

Table 14 presents a summary with all the TiN EWF values extracted from PVD and ALD samples. The different values of TiN effective work function can be related to chemical reactions inside the metal layer and/or at the interface between TiN and gate dielectric.

Physical vapor deposition was used to obtain a 20 nm thick TiN layer with electrical resistivity of 324 μΩ.cm, which indicates that the film is mettalic. These PVD TiN layer was used as upper electrode on MOS capacitors and Schottky diodes. Raman spectroscopy measurements had shown the presence of Ti and N vacancies into the TiN film. On Schottky diodes fabricated with PVD TiN, the Ti and N vacancies dissolution during the forming gas anneal process inside the TiN layer are mainly responsible for TiN EWF shift. As discussed in section 4.3.4, the Ti and N vacancies rearrangement in the TiN layer can occur during the sintering process, leading in changes on contact resistance, ideality factor and TiN EWF values. A change of 0.10 eV on TiN EWF value can be expected due to Ti and N vacancies dissolution during the FGA process. Furthermore, for MOS capacitors the dipoles variations at the interface between the metal and dielectric layers must be also considered. MOS capacitors fabricated with PVD TiN had presented 0.30 eV shift on TiN EWF values, due mostly to dipoles variations (mainly related with O vacancy at the TiN/SiO_2 interface) and Ti and N vacancies dissolution effects.

Table 14 – Summary of all TiN EWF values.

PVD TiN Samples[****]			
Sample	**Structure**	**Metal EWF (eV)**	**ΔEWF (eV)**
SiON	TiN/SiON/Si	4.65	-
SiO_2[7]	TiN/SiO_2/Si and Al/TiN/SiO_2/Si	4.35 – 4.05	0.30
Schottky diodes[7]	TiN/Si and Al/TiN/Si	4.55 – 4.45	0.10
ALD TiN Samples[††††]			
Sample	**Structure**	**Metal EWF (eV)**	**ΔEWF (eV)**
Pt/TiN Ref.	Pt/TiN/HfO_2/SiO_2/Si	5.05	-
TiN/AlN ref.	TiN/AlN(0nm)/HfO_2/SiO_2/Si	5.01	-
TiN - Al dif.	Pt/TaN/TiN/HfO_2/SiO_2/Si	4.68	0.37
TiN/TiAl	Pt/TiN/TiAl/TiN/HfO_2/SiO_2/Si	4.13 – 3.96	1.09
TiN/AlN	TiN/AlN/HfO_2/SiO_2/Si	5.01 – 4.78	0.23
Laminate	TiN/AlN/HfO_2/SiO_2/Si - laminate	4.85 – 4.59	0.42

In addition, lower TiN EWF values can be obtained with Al diffusion through this metal layer. The diffusion of Al into TiN layer can generate additional dipole at the interface between the metal gate electrode and high-k gate dielectric and therefore, lower values for TiN EWF can be expected. The impact of Al on TiN EWF was evaluated through MOS capacitors with an Al source embedded in the structure TiN/*Alsource*/HfO_2/Si. ALD was used to integrate an *Al source* on or in TiN layers. TiAl, AlN and Al layers were used as a Al source. A reduction of 1.09 eV on TiN EWF was obtained using TiAl on top of TiN (Table 14). This was likely to be induced by Al diffusion into TiN (near HfO_2). Indeed, 10 nm TiN yields only to a 0.37 eV TiN EWF decreasing. Furthermore,

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the study of TiN/AlN devices demonstrated that AlN layer can be used as *Al source* for TiN EWF adjustment. Al diffusion into TiN film was confirmed by SIMS and XPS measurements (see section 3.4). Also, with an increase on AlN thickness a decrease on TiN EWF was observed. Nevertheless, the Al diffusion into TiN film could be limited and reduced by the high Al concentration on the interface between the AlN and TiN. In addition, a decrease of 0.23 eV and 0.42 eV on TiN work function value were extracted from AlN/TiN stack and AlN/TiN laminate stack, respectively. So, the AlN/TiN laminate structures have been shown to be more effective to reduce the TiN work function than just increasing the AlN thickness

CHAPTER 5

CONCLUSIONS

This work presents the study of titanium nitride (TiN) films obtained by physical vapor deposition (PVD) and atomic layer deposition (ALD). The TiN layers were tested for their suitability as gate electrodes in MOS devices. For that MOS capacitors and Schottky diodes were fabricated using TiN as metal electrode. Additionally, FinFET devices were fabricated with PVD TiN as metal gate electrode to demonstrate that the developed TiN/Al metal stack is suitable for both, three dimensional (3D) and nMOS technology.

In a first approach, the physical and electrical properties of PVD TiN films were evaluated. The PVD TiN film, with thickness of 20 nm, presented low electrical resistivity value (324 μΩ.cm); which is an indication that this layer can be used as a metal electrode on MOS devices. The presence of Ti and N vacancies inside the TiN layer were confirmed by Raman spectroscopy analysis. Furthermore, oxygen incorporation on TiN surface layer was confirmed by XPS analysis and it is attributed to exposure of the TiN film to ambient air. Moreover, that surface oxidation does not alter the electrical resistivity of the TiN layer, for the thickness and thermal budget studied. Flat-band voltage and TiN EWF values were extracted from MOS capacitors fabricated with Al/TiN/SiO_2/Si, TiN/SiO_2/Si and TiN/SiN_xO_y/Si structures. Chemical reactions, such as Ti

and N vacancies inside the metal layer and/or at the interface between TiN and gate dielectric, can occur during thermal process, such as forming gas anneal (FGA) process, and therefore, different TiN effective work function and flat-band voltage (V_{FB}) values can be expected. Variations on TiN EWF and V_{FB} values are mainly related to dipole variations at the interface between metal electrode and dielectric. To experimentally substantiate the results, TiN effective work function was also investigated using Schottky diodes. Different TiN EWF and ideality factor values are attributed to vacancies reactions, such as Ti and N, during the FGA process on TiN/Si structures. In addition, oxygen incorporation can also influence the ideality factor values. The difference in TiN EWF extracted values from MOS capacitors and Schottky diodes is related to dipole variations and it was estimated to vary on average at maximum 0.45 eV on TiN EWF value. Moreover, the analysis of MOS capacitors and Schottky diodes fabricated with PVD TiN as metal electrode had shown that those films are suitable for nMOS applications (between 4.15 eV and 4.45 eV).

Secondly, TiN layers were obtained by ALD process. It is known that films obtained by ALD present stoichometric composition. Usually, ALD TiN layers show effective work function values suitable for pMOS applications. The Al diffusion into TiN layer can decrease the TiN EWF value due to an additional dipole formation at the interface between the metal gate electrode and high-k gate dielectric. In order to evaluate this effect, MOS capacitors were fabricated with several TiN and *Al source* structures as metal electrode (see section 4.4). Decreases in TiN EWF values were observed using TiAl, AlN and Al layers as *Al diffusion sources*. The Al diffusion profile into TiN was investigated by SIMS and XPS measurements. In addition, the study of AlN/TiN laminate structures has demonstrated to be more effective to reduce the TiN EWF value than just increase the AlN thickness. So, the Al diffusion technique can be used for TiN EWF adjustment for nMOS suitable values.

Finally, FinFET devices were fabricated using TiN as metal gate electrode. However, to study the Si nanowire properties, junctionless transistors (JL) were fabricated before FinFET devices. The electrical characterization of JL devices demonstrated that they are working like a gated resistor and the Si milling by Ga^+ FIB process can be used to obtain Si nanowires. So, FinFET devices were fabricated using Si milling (by Ga^+ FIB) and Al/TiN/SiO_2/Si gate structure. $I_{DS}xV_{DS}$ and $I_{DS}xV_{GS}$ measurements indicate that the fabricated FinFET device works like a conventional nMOSFET device. The extracted V_T value of 0.73 V corresponds to Al/TiN work function of 4.45 eV, which is appropriate for nMOS applications. This work function value is in agreement with the EWF values extracted from MOS capacitors and Schottky diodes (section 4.3). So, the Al/TiN stack obtained by PVD is suitable for three-dimensional devices, such as FinFET. In summary, this work conclusively shows that:

i) Al diffusion into TiN can be used for metal gate work function tuning;

ii) TiN films are suitable for planar and three-dimensional CMOS technology;

Although all the objectives of this PhD work were accomplished, there are some suggestions for future work.

Metal gate work function engineering is one of the keys to improve the performance of sub-22nm CMOS devices. The Al diffusion is a good approach to tune the TiN EWF however; further studies with AlN/TiN stacks should be performed. Additionally, scaling AlN/TiN stack thickness is necessary for employment on sub-22nm devices, due to device´s gate limited area. Furthermore, a study on TiN phase influence on its effective work function should be also performed, since the metal work function is dependent on film phase and composition.

As previously mentioned and highlighted, this thesis shows the fabrication of the first FinFET device in Brazil; however, further developments should be performed in order to increase the

device performance. Scaling the silicon nanowire (SiNW) dimensions can increase the FinFET and junctionless devices performance. Lower *fin* width dimensions, up to 20 – 10 nm, could be achieved using electron beam lithography systems. In addition, the implementation of a high-K/metal gate stack on FinFET devices could enhance the device performance (by decreasing the leakage current, for example). Furthermore, the usage of appropriate metal gate electrode, Al or TiN, with EWF values beween 4.1 and 4.5 eV, for pMOS and TiN or Pt, with EWF values beween 4.9 and 5.1 eV, for nMOS, and a reduction on Si height is also needed to improve the JL performance, since the complete depletion of gate channel would be easier on smaller SiNW.

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APPENDIX 1

LIST OF PUBLICATIONS

➢ Articles:

- L.P.B. Lima, M.V.P. dos Santos, M.A. Keiler, H.F.W. Dekkers, S. De Gendt, J.A. Diniz, "*N-Junctionless Transistor Prototype: Manufacturing Using a Focused Ion Beam System*", ECS Trans., **66**, 61 (2015).
- L.P.B. Lima, H.F.W. Dekkers, J.G. Lisoni, J.A. Diniz, S. Van Elshocht, S. De Gendt, "*Metal gate work function tuning by Al incorporation in TiN*", J. App. Phys., **115**, 074504 (2014).
- [8]L.P.B. Lima, J.A. Diniz, C. Radtke, M.V.P. dos Santos, I. Doi, J. Godoy Fo, "*Influence of Al/TiN/SiO2 structure on MOS capacitor, Schottky diode, and fin field effect transistors devices*", J. Vac. Sci. Technol. B, **31**, 052202 (2013).
- H.F.W. Dekkers, L.P.B. Lima, S. Van Elshocht, "*Conductivity Improvements of Atomic Layer Deposited Ta_3N_5*", ECS Trans., **58**, 195 (2013).
- [90]M.V.P. dos Santos, L.P.B. Lima, J.A. Diniz, J. Godoy Fo, "*Fabrication of p-type silicon nanowires for 3D FETs using focused ion beam*", J. Vac. Sci. Technol. B, **31**, 06FA01 (2013).
- L.P.B. Lima, J.A. Diniz, C. Radtke, I. Doi, J. Miyoshi, A.R. Silva, J. Godoy Fo, "*Oxygen incorporation and dipole variation in tantalum nitride film used as metal-gate electrode*", J. Vac. Sci. Technol. B, **30**, 042202 (2012).
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- [100]L.P.B. Lima, M.V.P. dos Santos, F.H. Cioldin, J.A. Diniz, I. Doi, J. Godoy Fo, "*Junctionless Fabrication on SOI Wafers Using Focused Ion Beam Milling and Al Diffusion*", ECS Trans., **49**, 367 (2012).
- F.H. Cioldin, L.P.B. Lima, I. Doi, J.A. Diniz, J. Godoy Fo, E.A. Zambotti, "*Investigation of thermal stability of titanium nitride using a RTA process*", ECS Trans., **49**, 1 (2012).
- L.P.B. Lima, J.A. Diniz, I. Doi, J. Miyoshi, A.R. Silva, J. Godoy Fo, "*Tantalum Nitride as Electrode for MOS Technology and Schottky Diode*", ECS Trans., **39**, 69 (2011).

➢ Brazillian national-state newspaper:

- J.A. Diniz, L.P.B. Lima; M.V.P dos Santos; "*Nanofios de Silício ampliam capacidade de processadores"*, Jornal da Unicamp, Campinas, Brazil, 599, p. 5, 02-June- 2014.
- J.A. Diniz; L.P.B. Lima; M.V.P dos Santos; "*Nasce o Transistor 3D - Grupo desenvolve o 1º transistor 3D do país*". Jornal da Unicamp, Campinas, Brazil, 3, p. 3, 25-March-2013.
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- J.A. Diniz; L.P.B. Lima; M.V.P dos Santos; "*Pesquisa feita na Unicamp cria chip com dispositivo 3D*". Correio Popular - Campinas, Campinas, Brazil, p. B8 - B8, 26-February-2013.
- J.A. Martino; J.A. Diniz; L.P.B. Lima; M.V.P. dos Santos; "*Transistor 3D é fabricado no Brasil pela primeira vez*". Revista FAPESP, São Paulo, Brazil, 13-December-2012.

➢ Conference Contributions (with proceedings):

- L.P.B. Lima; M.V.P. dos Santos; J. Godoy Filho; H.F.W Dekkers; S. De Gendt; J. A. Diniz, "*Focused Ion Beam milling for Si nanowire and Junctionless transistor prototype.*", 58th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN), Washington, USA, 2014.

- H.F.W. Dekkers, L.P.B. Lima, S. Van Elshocht, "*Conductivity Improvements of Atomic Layer Deposited Ta_3N_5*", Materials for Advanced Metallization (MAM), Leuven, Belgium, 2013.
- M.V.P. dos Santos, L.P.B. Lima, J.A. Diniz, J. Godoy Fo, "*Fabrication of p-type silicon nanowires for 3D FETs using focused ion beam*", 57th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN), Nashville, USA, 2013.
- L.P.B. Lima; J. A. Diniz; I. Doi; J. Godoy Filho; "*Protoype of Junctionless Transistor on SOI wafers using Focused Ion Beam milling*", American Vacuum Society 59th International Symposium and Exhibition (AVS), Tampa, USA, 2012.
- L.P.B. Lima; M.V.P. dos Santos; F.H. Cioldin; J.A. Diniz; I. Doi; J. Godoy Filho; "*Junctionless fabrication on SOI wafers using Focused Ion Beam milling and Al diffusion*", 27th Symposium on Microelectronics technology and devices (SBMicro), Brasília, Brazil, 2012.
- F.H. Cioldin, L.P.B. Lima, I. Doi, J.A. Diniz, J. Godoy Fo, E.A. Zambotti, "*Investigation of thermal stability of titanium nitride using a RTA process*", Brazilian Materials Reseach Society (MRS) Meeting (SBPMat), Florianópolis, Brazil, 2012.
- L.P.B. Lima; J. A. Diniz; Radtke C; I. Doi; J. Miyoshi; A.R. Silva; J. Godoy Filho; "*Structural and Electrical Characteristics of TaN Film Deposited by DC Sputtering for MOS Capacitor and Schottky Diode Upper Electrodes.*", American Vacuum Society 58th International Symposium and Exhibition (AVS), Nashville, USA, 2011.
- L.P.B. Lima; J. A. Diniz; Radtke C; I. Doi; J. Miyoshi; A.R. Silva; J. Godoy Filho; "*XPS Analyses and Work Function Extraction of Titanium Nitride Electrodes for MOS Technology and Schoktty Diode.*", Advanced Metallization Conference (AMC), San Diego, USA, 2011.
- L.P.B. Lima; M.A. Moreira; J.A. Diniz; I. Doi; "*Titanium Nitride Deposited by DC Sputtering for MOS Gate Electrode Application*". 13th International Conference on the Formation of Semiconductor Interfaces (ICFSI), Prague, Czech Republic, 2011.
- L.P.B. Lima; J.A. Diniz; I. Doi, J. Miyoshi; A.R. Silva; J. Godoy Filho; "*Tantalum Nitride as Electrode for MOS Technology and Schottky Diode*", 26th Symposium on Microelectronics technology and devices (SBMicro), João Pessoa, Brazil, 2011.

APPENDIX 2

CHARACTERIZATION TECHNIQUES

7.1 X-ray photoelectron spectroscopy (XPS)

Basically the x-ray photoelectron spectroscopy (XPS) measurement consists on the study and analysis of energy from photo-electrons emitted from the material surface. For this purpose, the material surface is placed in a vacuum chamber and photons, with x-ray energy, are irradiated towards the material surface and, therefore, some energy is transferred to the surface atoms. Depending on material composition and irradiated photons energy, some photon-electrons (PE), originated from the atom's electron outer shell, can be ejected from the surface material. The energy of the emitted photon-electrons (EPE) is associated to surface composition and the number of EPE is highly related to the surface atom concentration. Fundamentally, photons can interact with matter by two possibilities:

i) The particle can be scattered through an electron orbiting the atom, and consequently, the photon loses some energy. This process of energy loss is called Compton scattering;

ii) The particle can interact with an electron orbiting the atom and all the photon energy is transferred to the electron, and therefore, this electron can be emitted from the atom.

The XPS measurement is based on the process of the photon total energy is transferred to an atom's electron (second case described above) and Figure 44 shows a schematic of this process. First, no electrons are ejected from the atom if the incident photon energy is lower than the threshold energy (E_{th}) which is characteristic of each material and therefore, the photon-emission process will not occur. The photon-emission process will start only if the energy of the incident photon is higher than the material's threshold energy, and it is important to notice that this process is independent of the light source intensity.

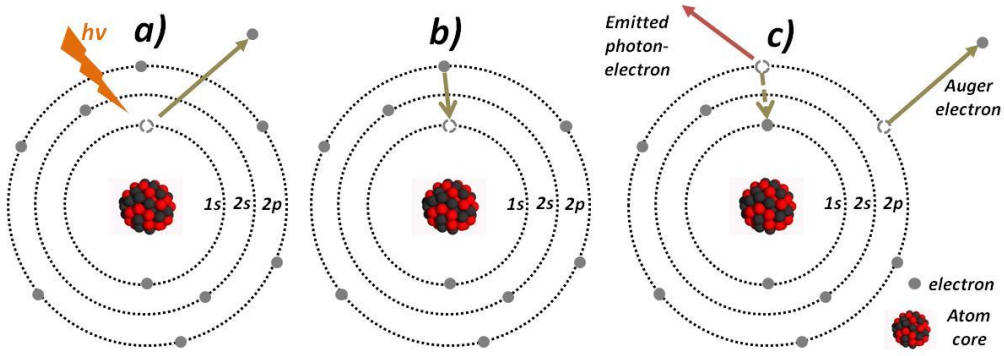

Figure 44 – Schematics of a) photoemission process; b) electron's rearrangements; c) emission.

If the incident photon energy is sufficient to start the photon-emission process, the number of EPE is proportional to the incident radiation intensity. Thus, increasing the amount of incident photons with energy higher than E_{th} reaching the material's surface, more EPE will be ejected from this surface. The kinetic energy of that EPE (K_{EPE}) is linearly proportional to the frequency (energy) of incident photons; however, only energies higher than E_{th} will be transferred to the EPE as kinetic energy (see equation 15). It is important to notice that the photo-emission process is extremely fast, around 10^{-16} seconds.

$$E_{th} = hv - K_{EPE} \quad (15)$$

The energy of x-ray source is represented by the term *hv* at equation 15. In principle the XPS spectrometer analyses the kinetic energy from the emitted photo-electrons (K_{EPE}). So, it is possible, using XPS analysis, to determine the photon-electron binding energy by *hv* and K_{EPE}.

The electron binding energy is proportional to the distance to the atom core; so, high E_{th} can be expected for electrons closer to the atom core and therefore, higher *hv* is needed to start the photo-emission process. On the other hand, electrons located far from the atom core present lower binding energy values and so, less *hv* is needed to start the photo-emission process. Furthermore, the E_{th} depends on the atom and material characteristics. Thus, since the binding energy is specific for each element, the chemical composition can be determined by XPS analysis due to different E_{th}. For gases, the binding energy of an orbiting electron is the same value as the ionization energy or electron ionization potential. For solid materials, the energy to remove an electron from the material surface (called work function) needs to be considered on biding energy study. In addition, Auger electrons can be ejected from the surface material, and then a good calibration of the apparatus is required to determine the E_{th}. In this work, XPS measurements were done on metallic films, so a brief description of the apparatus to do that on metal layers will be given.

The metallic sample is electrically placed with the spectrometer and, usually the sample is connected to the same ground connection as the spectrometer. With this, the Fermi levels and the energy of the higher occupied level of metallic sample and spectrometer are aligned. So, it is possible to measure and estimate K_{EPE} value. However, it is needed to consider the metal work function (ϕ_F) and consequently, equation 15 is not valid anymore. The ϕ_F is defined as the minimum energy needed to eject an electron from the highest occupied energy to the vacuum level (E_{vac}), shown on equation (16).

$$\phi_F = E_F - E_{vac} \tag{16}$$

Where E_F is the material's Fermi level. So, equation 15 can be expressed in terms of element's binding energy (E^F_B), K_{EPE} and the spectrometer work function (ϕ_{Fsp}):

$$E_B^F = h\nu - K_{EPE} - \phi_{Fsp} \quad (17)$$

Therefore, with a good initial calibration of spectrometer and equation (17) it is possible to determine the value of E^F_B. The system (spectrometer) calibration can be done by placing a standard gold (Au) sample and adjusting the Au binding energy ($E^F_{4f7/2}$=83.96eV). The binding energy scale is calibrated considering two different lines with well known values, for example, cooper (Cu) presents 3s and $2p_{3/2}$ transition lines. If the spectrometer chamber is maintained in ultra high vacuum (UHV) environment, the initial calibration is valid; however, if reactive gases are injected inside the chamber, new calibration process is needed.

Moreover, as previously discussed, XPS is a *surface* technique, with a resolution around 1 nm. However, it is possible to do the sample material sputtering and XPS measurement combined *in-situ*; as in:

i) The XPS measurement of the top surface is done;

ii) Some part of sample material is removed by sputtering (usually with Ar^+ ions);

iii) Immediately after the sputtering and *in-situ*, another XPS measurement is performed;

So, this process can be done several times and a XPS of a depth profile can be achieved. Also, using the sputtering method, the measurement of an oxidized surface is avoided. Nevertheless, some mixing (surface and bulk layers) might occur during the sputtering process.

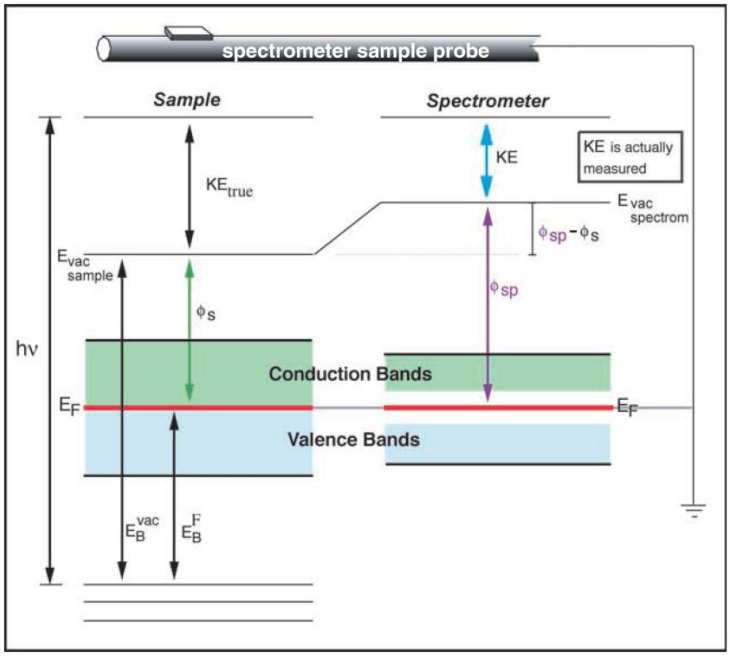

Figure 45 – Schematic of energy band diagrams for a metal sample (grounded to the spectrometer). Extracted from J.C. Vickerman[‡‡‡‡].

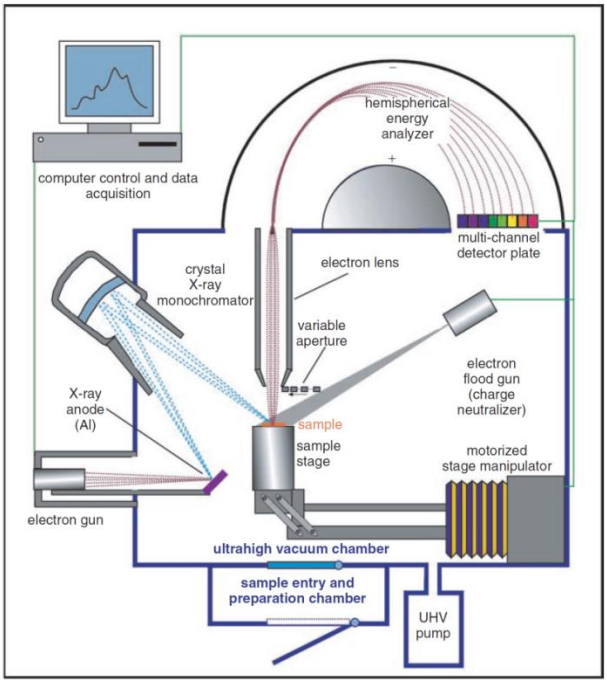

Figure 46 – Schematic of a XPS system used in this work. Extracted from J.C. Vickerman.

‡‡‡‡ J.C. Vickerman, "Surface Analyses – The Principal Techiniques", 2nd edition, 2009.

7.2 Raman spectroscopy

Raman spectroscopy is based on the vibrational modes spectroscopic technique, and for this reason, this method is frequently said to be complementary to infrared spectroscopy. Basically, as described on J.C. *Vickerman*, the Raman effect (first observed by C.V. Raman in 1928) "*relies upon the polarization of the electron cloud describing a chemical bond by the electric field of incident electromagnetic radiation, which induces a dipole moment, which in turn is time dependent due to the vibration of the atom forming the bond*".

So, in summary, the Raman effect is the consequence of the interaction between an incident radiation (with frequency of ν_i) and the surface material, which leads into molecules *virtual electronic state* (composite function of rotational, vibrational and electronic states) and therefore, an emission of a photon from the first excited vibrational (frequency of ν_{vib}) state (shown in Figure 47). These emitted photons are called Stokes photons, with frequency of $\nu_i + \nu_{vib}$. Also, the emission of anti-Stokes photons (high energy photons re-emitted from a vibrating molecule; with frequency of ν_i-ν_{vib}) can occur. If the energy of the incident radiation coincides with a molecular state, the Raman scattering is highly increased, and this condition is known as the resonance Raman effect.

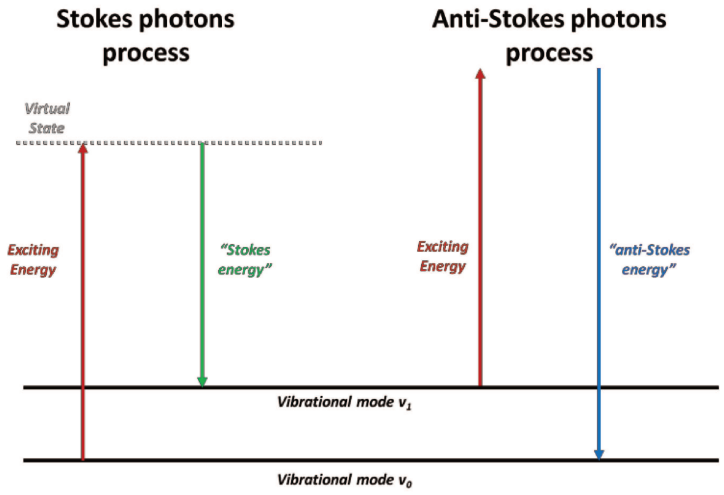

Figure 47 – Energy level schematics of the vibrational Raman effect.

Since the anti-Stokes photons present smaller intensity counts than the Stokes photons, usually the Stokes mode is monitored. A simple schematic of Raman spectroscopy measurement is shown in Figure 48. The incident radiation (preferably monochromatic) is scattered by the sample and Raman-shifted waves are identified by detector.

Using Raman spectroscopy it is possible to determine several properties of the sample, such as composition, crystal structure and strain. For example, Raman analysis has been widely used for SiGe characterization, in order to extract the surface composition and strain.

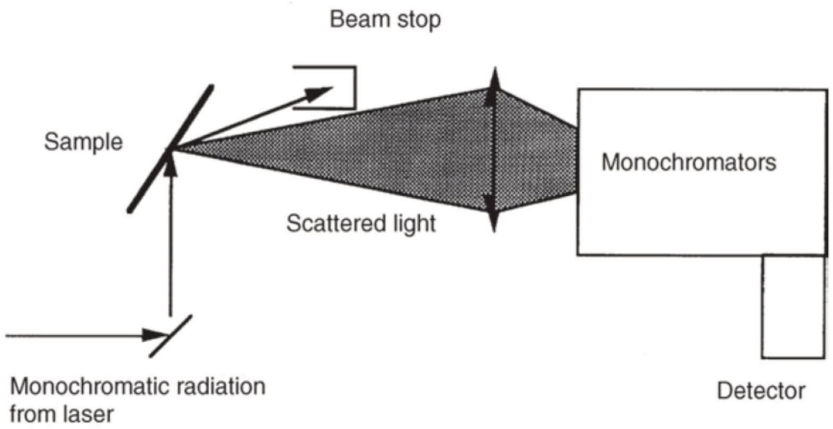

Figure 48 – Schematic of a Raman experiment. Extracted from J.C. Vickerman.

7.3 Energy dispersive x-ray spectroscopy (EDS)

Energy Dispersive X-Ray Spectroscopy (EDS) is a chemical microanalysis technique used in conjunction with scanning electron microscopy (SEM) which detects X-rays emitted from the sample during bombardment by an electron beam to characterize the elemental composition of the sample [93,94]. The technique exploits the fact that a X-ray photon is generated when an orbiting electron is displaced by an electron of the SEM. When the sample is bombarded by the SEM electron beam, inner shell electrons are ejected from the atoms comprising the sample surface (Figure 49a) and empty spaces are filled by electrons from a higher state (Figure 49b). As a result of this process X-ray is emitted to balance the energy difference between the two electrons' states (Figure 49c). X-ray energy is characteristic of the element from which it was emitted and the X-ray detector measures the relative abundance of emitted X-rays versus their energy [96]. When an incident X-ray strikes the detector (usually a solid state semiconductor) it creates an electron-hole pair which is converted into a charge pulse (that is proportional to the energy of the X-ray) which is converted to a voltage pulse by a charge-sensitive preamplifier (Figure 50). The signal is then sent to a multichannel analyzer where the pulses are sorted by voltage amplitude. Preamplifier output is a voltage *ramp* where each X-ray appears as a voltage step on the ramp. The energy, as determined from the voltage measurement, for each incident X-ray is sent to a computer for display and further data evaluation. The spectrum of counts *versus* X-ray energy is evaluated to determine the elemental composition of the sampled volume. EDS detectors are designed to convert the X-ray energy into the voltage signal as accurately as possible. At the same time, the electronic noise must be minimized to allow the detection of the lowest X-ray energies. Figure 51 presents the energy levels of atomic shells and electronic transitions. Table 15 shows the X-ray emission energy for Al, Ga, Pt, Si and O [97].

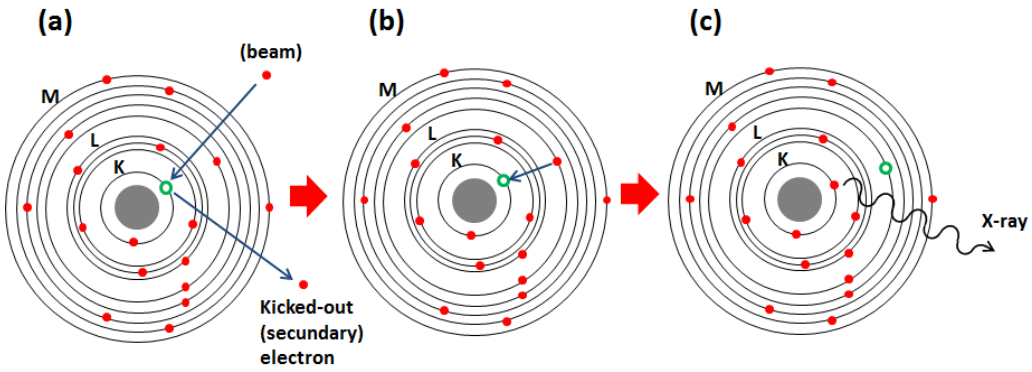

Figure 49 - Schematics of (a) atomic bombardment by the SEM electron beam causing electrons from inner shell to kick-out; (b) empty orbital is filled by electron from a higher state and (c) X-ray is emitted to balance the energy difference between the two electron's states.

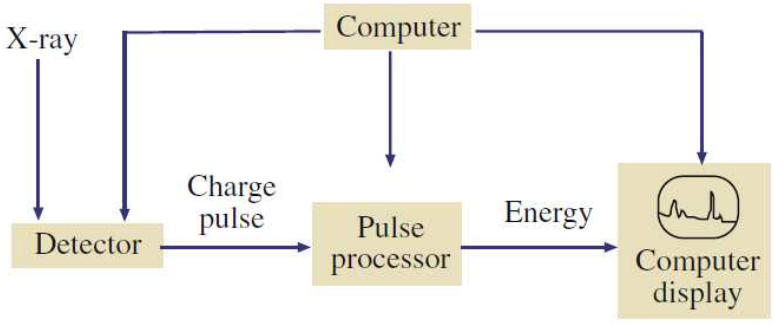

Figure 50 - Schematic diagram of the principle of XEDS. A computer controls the detector, the processing electronics and the display.

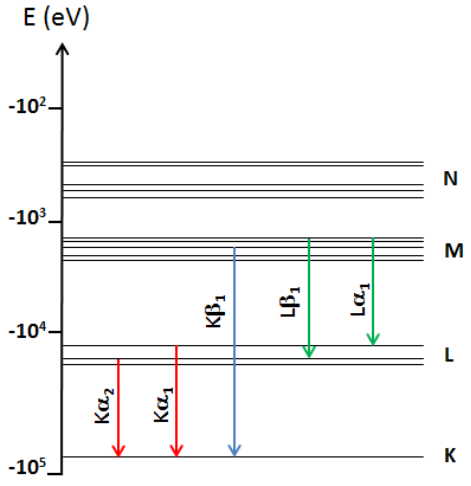

Figure 51 – Energy levels of atomic shells and electronic transitions.

Table 15 – X-ray emission energy of Al, Ga, Pt, Si and O.[86]

Element	***Energy (keV)***					
	Ka_1	***ka_2***	***L1***	***La_1***	***La_2***	***Ma_1***
Al	1.486	1.486	-	-	-	-
Ga	-	-	1.036	1.097	1.097	-
Pt	-				-	2.050
Si	-	1.739	-	-	-	-
O	0.524	0.524	-	-	-	-

The X-ray detector (Figure 52a) is fabricated from high purity silicon crystal with a large area contact facing the incoming beam. There is an anode contact on the opposite side to which a bias voltage is applied (Figure 52b). When the detector is exposed to X-rays, it converts each detected photon into an electron cloud with a charge that is proportional to the characteristic energy of that X-ray. These electrons are raised into the conduction band of the silicon semiconductor and leave behind holes that behave like free positive charges within the sensor. The electrons are then collected at the anode.

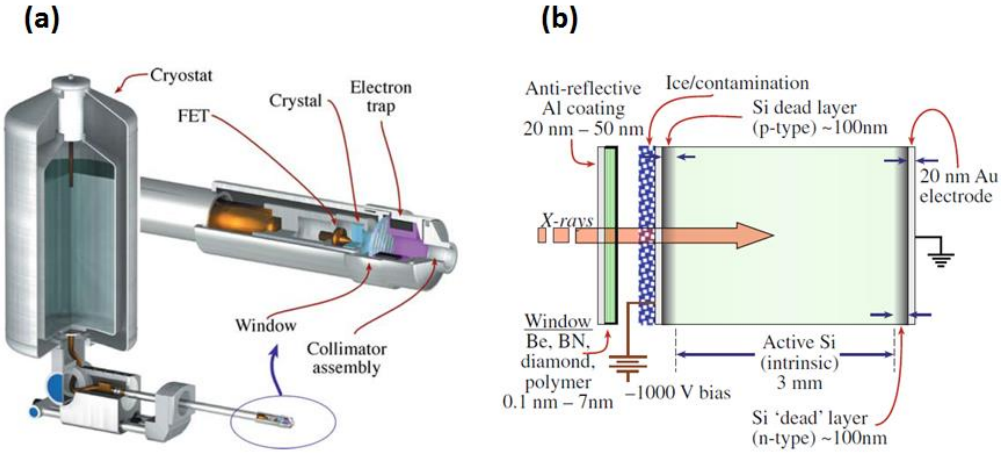

Figure 52 - a) Cross section of an Si(Li) EDS detector. In the intrinsic Si region the incoming X-rays generate electron-hole pairs which are separated by an applied bias. A positive bias attracts the electrons to the rear ohmic contact and this charge pulse is amplified by an FET. b) Diagram of the individual elements.

7.4 Ideality factor and metal work function extraction from Schottky diodes

The metal-semiconductor contact presents low voltage and charges concentration drop during the conduction mode and high switching speed, and therefore, solar cell devices are fabricated using this metal-semiconductor contact. Figure 53 shows the band diagrams of the ideal case for metal-semiconductor contact. The metal work function (Φ_m) is higher than the semiconductor work function (Φ_s), so semiconductor Fermi energy level is higher than metal Fermi energy level.

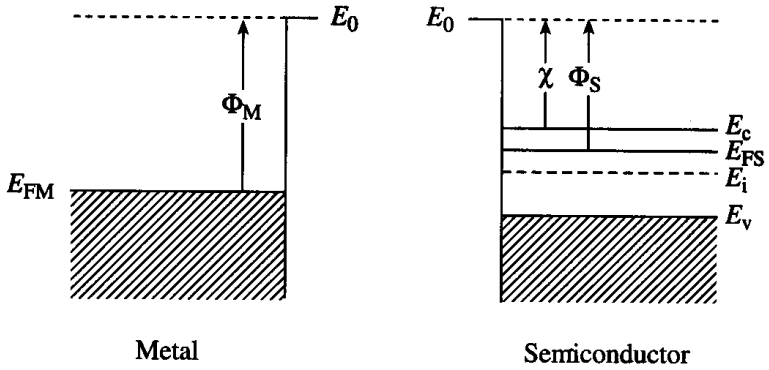

Figure 53 – Ideal metal-semiconductor energy band diagrams before the contact. E_0 is the vacuum level.

Before the physical contact, the electrons presented in the semiconductor are in a higher energy level than the electrons in the metal material. After the physical contact, the system composed by the metal and semiconductor will be in equilibrium, where semiconductor and metal electrons will be at the same energy level and the both material's Fermi levels will be aligned at the same energy level. Thus, a depletion region will be generated by the movement of electrons from both materials to achieve the equilibrium. In this depletion region, the electrons density is lower than in the semiconductor, resulting in a conduction and valence energy band *tilt*, as shown in Figure 54. For n-type semiconductor, the conducting band will *move away* from the Fermi level, indicating that

the electron density is smaller in this region. With this, a barrier Φ_B will be formed and block the electrons flow from metal to semiconductor. The height of this barrier Φ_B can expressed as:

$$\Phi_{Bn} = \Phi_M - \chi_{Si} \; ; \; \Phi_{Bp} = \frac{E_G}{q} - \Phi_M + \chi_{Si} \tag{18}$$

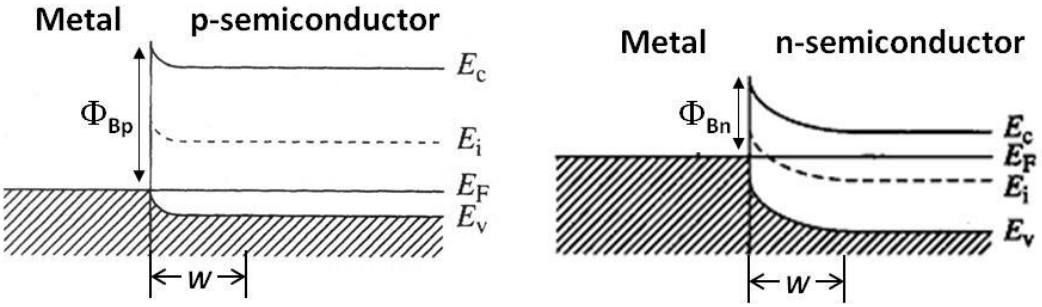

Figure 54 – Schottky contact (ΦM>ΦS) under equilibrium conditions for p-type and n-type semiconductor. χSi is Si electron affinity

For a real diode, the total current flow at the *pn* junction (I) is be expressed as:

$$I = I_S \left[exp \frac{V k_B T}{\eta q} - 1 \right] \tag{19}$$

Where, I_S is the saturation current, k_B is the Boltzmann constant, q is the electron charge ($1.6x10^{-19}$C), V is the applied bias and η is the diode's ideality factor. So, the ideality factor can be estimated using equation (20) and log(I) *verus* V plot.

$$\eta = \frac{\frac{d(logI)}{dV} k_B T}{q \ln(10)} \tag{20}$$

Thus, the ideality factor can be easily determined by taking the log(I)xV linear slope and dive by term $k_BT/q\ln(10)$, which at 300K is approximately 60mV. In addition, I_S value can be extract from the log(I)xV curve, it is the intersection between the linear slope tangent line and the x-axis, and therefore, the Schottky barrier height (Φ_b) is given by:

$$\Phi_b = -\frac{q}{kT} ln \left(\frac{I_S}{A^{**} T^2 A} \right) \tag{21}$$

Where A^{**} is the Richardson constant and A is the device area. Then, the metal work function (W_F) can be determined considering Si electron affinity (χ_{Si}) and equation (21), as follow:

$$W_F = \Phi_b + \chi_{Si} \quad (22)$$

7.5 C-V measurements: parameters extraction from MOS capacitors

Capacitance-voltage (C-V) measurement allows the extraction of several parameters from semiconductor device and materials; for example, oxide charges, oxide thickness, interface trap density, flat-band voltage and metal electrode effective work function. Figure 55 shows a schematic of a basic MOS capacitor and the C-V curves for low and high frequencies. For C-V measurements, DC bias voltages are applied on MOS capacitor while the capacitance measurements are done with an AC signal. In this work, AC frequency of 1MHz was used for C-V measurements. So, the bias is applied as a DC voltage sweep, which drives the MOS capacitor structure from its accumulation region into the depletion region, and then into inversion region (as shown in Figure 56).

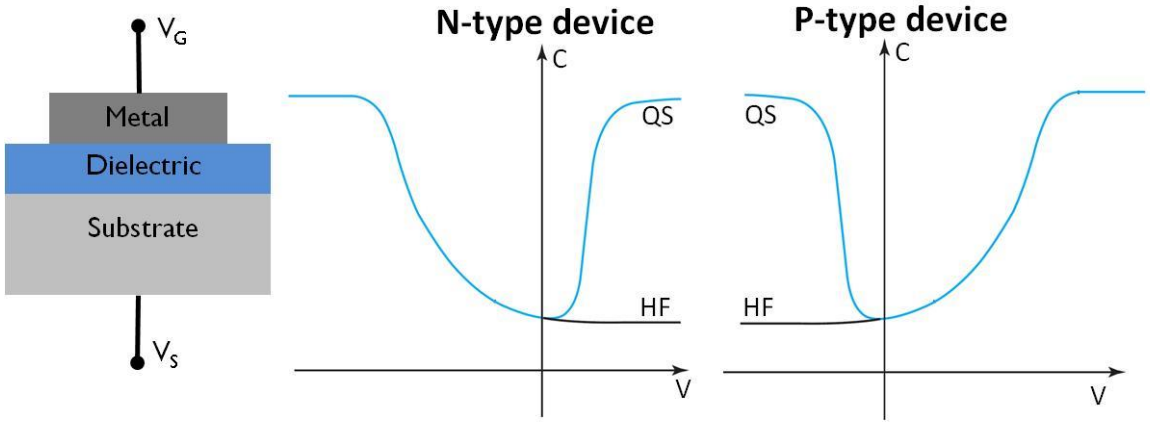

Figure 55 – MOS capacitor schematic and C-V characteristics for low and high frequencies.

At the accumulation region, the majority carriers in the substrate accumulate near the dielectric interface (see Figure 56), due to the strong DC bias. Those charges cannot get through the dielectric

layer increasing the carrier density at this region, and therefore, the capacitance achieves its maximum value. Furthermore, decreasing the DC bias, the majority carriers are "pushed away" from the dielectric interface, and there is a formation of a depletion region. Moreover, when the DC bias voltage is reversed, the majority carriers will be distant from the dielectric layer, and the capacitance achieves its minimum value (see Figure 56).

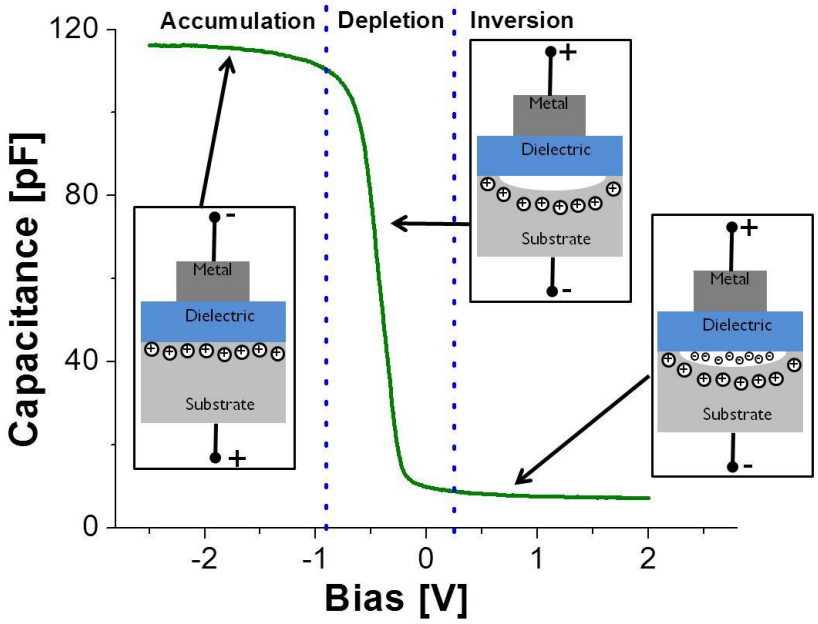

Figure 56 – C-V characteristic showing the three regions: accumulation, depletion and inversion.

Figure 57a shows the equivalent circuit for a C-V measurements model, considering the capacitance (C), serie resistance (r_S) and conductance (G). Typically, C-V measurements were performed using two different models: i) parallel model (Figure 57b) and ii) series model (Figure 57c). The appropriate measurement model can be determined by the comparison of the dissipation factor obtained at two different frequencies, for example at 100 kHz and 1 MHz.

Small capacitance yields large reactance, and so, the effect of the parallel resistance (G_P) is relatively more significant than the series resistance (R_S). Then, when compared with the

capacitive reactance, the R_S value can be neglected. On the other hand, when the capacitance presents large value (low impedance), R_S is more significant than G_P and then, G_P can be neglected. So, in summary, a series measurement is performed on devices with low impedance, while parallel measurement is employed on high impedance samples.

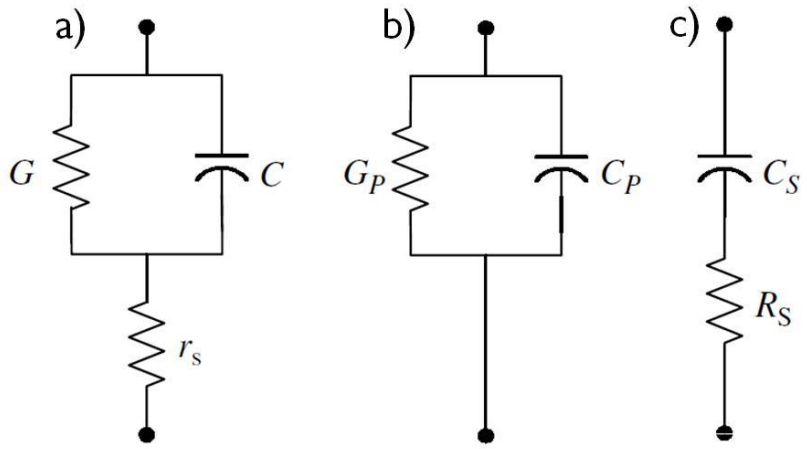

Figure 57 – a) Basic circuit model for C-V characteristic; b) parallel mode circuit; and c) series mode circuit.

Several device and semiconductor parameters (such as substrate doping, dielectric thickness, interface charge density) can be extracted from the C-V measurements. In this work, mainly the flat-band voltage (V_{FB}) and metal work function (W_F) were extracted from the C-V characteristics. Typically, the flat-band voltage is determined by comparison the measured high frequency C-V characteristic with the ideal theoretical C-V curve (obtained without the effects of dielectric charges and work function difference). However, V_{FB} can be extracted from the intercept of experimental $1/C^2$ *versus* V characteristic, as shown in Figure 58 [65]. The metal work function can be calculated by equation (23).

$$W_F = V_{FB} + \frac{Q_{SS}}{C_{ox}} + \chi_{Si} + \frac{E_{gsi}}{2} \mp \phi_b \qquad (23)$$

Where Q_{SS} is the effective charge density and E_{GSi} is the silicon gap energy.

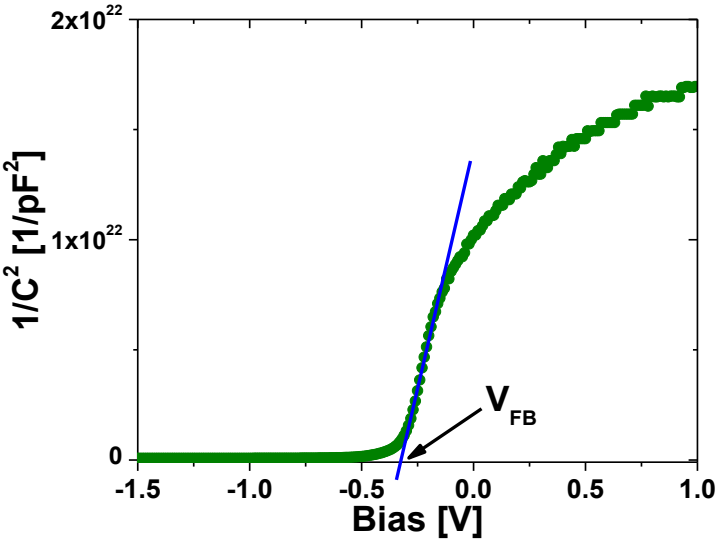

Figure 58 – Example for VFB extraction using $1/C^2$ method.

In addition, some parameters can affect the C-V characteristic resulting, in some cases, on distortions on those curves. Figure 59 shows dielectric thickness, substrate doping, effective charge densities and interface trap densities influence on C-V curves.

The maximum capacitance (C_{max}), at the accumulation region, is defined as:

$$C_{max} = \frac{\varepsilon_0 \varepsilon_{die} A}{t_{die}} \quad (24)$$

Where t_{die} is the dielectric thickness, A is the device area, ε_0 is vacuum dielectric constant and ε_{die} is dielectric's constant. So, decreasing the dielectric thickness, the C_{max} will be increased as shown on Figure 59a. This effect is predominant at the accumulation region. In addition, the equivalent oxide thickness (EOT) can be extracted as:

$$EOT = \frac{\varepsilon_0 k_{die} A}{C_{max}} \quad (25)$$

The depletion region at the interface between the dielectric and substrate is related to the substrate net doping. With an increase on the substrate doping, the depletion region will be reduced and, consequently, the silicon capacitance will be increased. Also, the threshold voltage is

increased, and therefore, as presented on Figure 59b, the inversion region is shifted (distorted) for more positive bias voltages. The effective charge density (Q_{SS}) mainly affects the flat-band voltage value. Higher Q_{SS} values result into lower V_{FB} values. As a result, the C-V curve is shifted to the left with an increase on Q_{SS}, as shown on Figure 59c. Distortions on C-V curves can also be attributed to interface trap density (N_{it}), as shown in Figure 59d, due to the simultaneous reduction on V_{FB} and increase on threshold voltage.

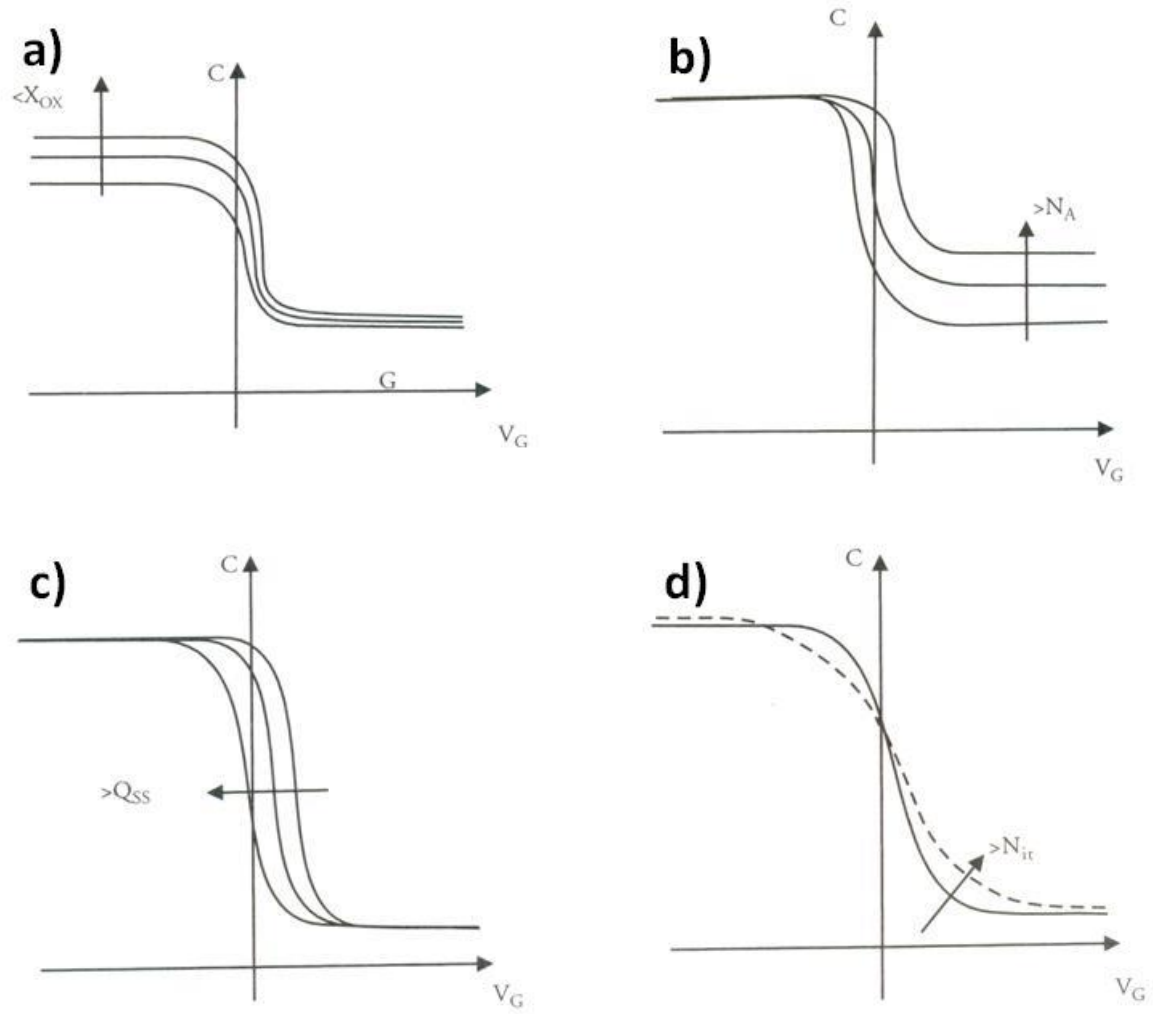

Figure 59 – Influence of a) dielectric oxide thickness; b) Si doping concentration; c) interface charge density and d) interface trap density on C-V characteristics.

APPENDIX 3

JUNCTIONLESS TRANSISTOR OPERATION

In order to reduce the complexity in the manufacturing process of nano-scale devices, junctionless (JL) transistors were developed. Unlike the traditional planar MOSFET and FinFETs, JL transistors are devices without source/channel and drain/channel junctions, and therefore, those devices present a constant doping profile between source, gate and drain. Silicon nanowire (SiNW) structures are used for gate formation in JL devices. Unlike planar MOSFET and FinFET, junctionless transistors operate in the accumulation regime, due to the unique doping profile (no junctions). Basically, the JL transistor is a resistor in which the mobile carrier density can be modulated by the gate [78,79].

For JL transistor, a high uniform doping concentration (between 10^{19} and 10^{21} cm^{-3}) is required in order to achieve appropriate current drive, and consequently, a large body current can be found when JL transistor is working in the "on state". In the "off state" the channel is depleted and therefore, no conduction through the channel is observed. However, the difference between the gate material work function and semiconductor influences the formation of the depletion region

into the channel during the "off state". Additionally, the transistor dimensions should be small enough to allow the channel depletion, which turns the device off.

The conduction mechanisms are different in FinFET and JL devices. As mentioned before, JL transistors operate in accumulation regime, while FinFETs operate in inversion mode. Figure 60 shows these mechanisms in inversion-mode, *traditional* accumulation-mode and JL devices. For in junctionless transistors, the depletion of the heavily doped gate nano structures generates a large electric field perpendicular to the current flow below the threshold voltage (V_{th}), and so, the device is turned off. However, since the channel is electrically neutral (no junctions), above the threshold voltage the electric field drops to zero. This is the opposite of what happens on inversion-mode or even *traditional* accumulation-mode devices, where the electric field achieves the highest values when the device is in the "on state". Table 16 shows a comparison between an inversion-mode FET and JL devices.

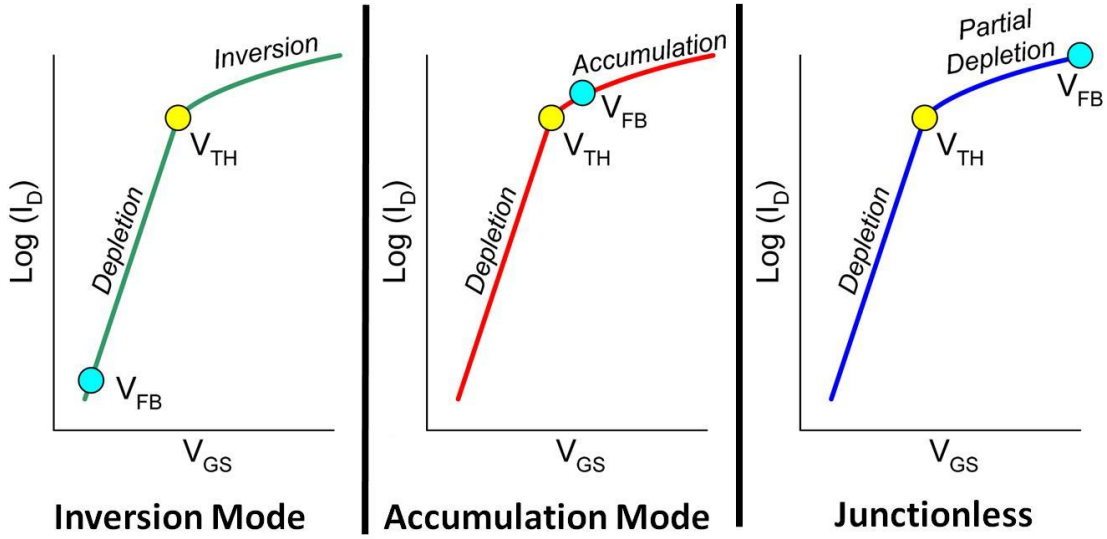

Figure 60 – Conduction mechanisms. Extracted from references 70 and 93.

Table 16 – Comparison between inversion-mode FET and junctionless devices.

Inversion-mode FET[70]	**Junctionless**[68,69,70]
SS ~ 60 – 75 mV/dec	SS ~ 60 – 300 mV/dec
$I_D \approx \mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})^2$	$I_D \approx q\mu N_D \frac{T_{Si} W_{Si}}{L} V_{DD}$

Usually silicon p-type substrates are used for n-channel inversion-mode devices, which presents flat-band voltage (V_{FB}) values lower than the V_{th}. The Si substrate is depleted in sub-threshold regime (between V_{FB} and V_{th}). For gate-source voltage (V_{GS}) values higher than V_{th}, the device operates in inversion regime, with Si surface in *inversion mode* (see Figure 60).

On the other hand, n-channel accumulation-mode devices are fabricated in lightly doped n-type Si substrates. The Si substrate is depleted in sub-threshold regime and V_{th} is determined when the substrate leaves the depletion regime. With this, a small bulk current started to flow through the channel. The V_{FB} is determined when the entirely Si substrate is neutral and, in contrary to the inversion-mode devices, the V_{FB} is slightly higher than V_{th} (see Figure 60). The device is not fully depleted in the region between V_{th} and V_{FB}. For V_{GS} values higher than V_{FB} the device operates in accumulation regime, with Si surface in *accumulation mode* (see Figure 60).

As previously mentioned, heavily doped substrates are required for JL devices. Si substrates with high n-type doping concentration are used for n-channel JL devices. The substrate is depleted in sub-threshold operation, and consequently, the device is turned off (see Figure 60 and Figure 61a). As well as occurs in accumulation-mode devices, a bulk current starts to flow when the channel is neutralized (see Figure 61b). However, due to the high doping concentration, this current is larger in JL transistors than in accumulation-mode devices. The depletion layer into Si channel decreases with an increase on the V_{GS}. As a result, the neutral channel is reduced and the device is not entirely depleted. For low drain-source voltage (V_{DS}), when the V_{GS} assume values near the V_{FB}, the channel region starts to become neutral. Increasing the V_{DS} value, the JL operates

into saturation mode (see Figure 61c) and presents output characteristics similar to traditional MOSFET devices.

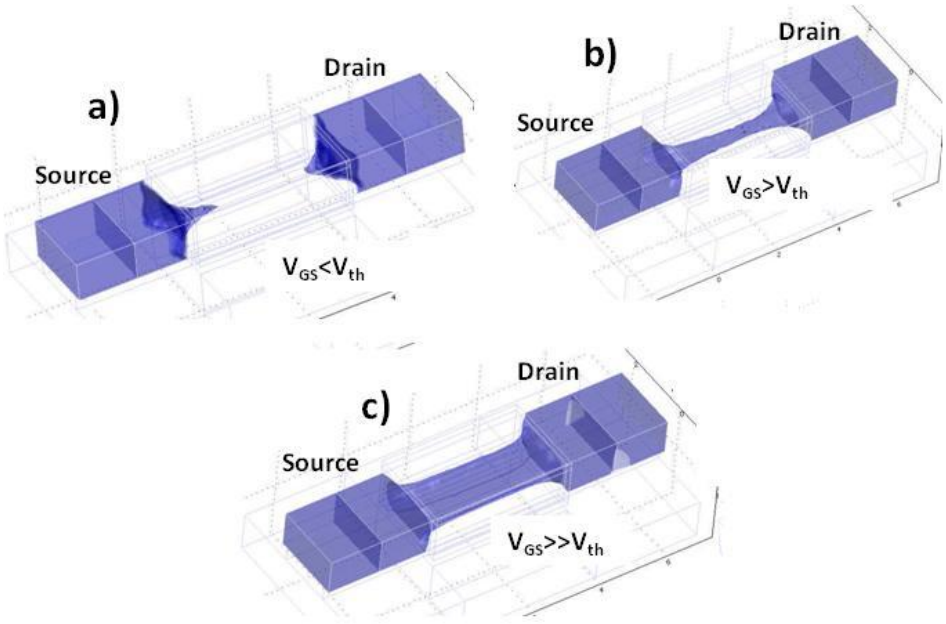

Figure 61 – Electron concentration plots in an n-type JL transistor. Extracted from reference 101.

Literature reports that JL devices presents *better* drain induced barrier lowering (DIBL) and SS values than the conventional 3D MOSFET with the same dimensions. Furthermore, once the zero temperature coefficient (ZTC) is reached no changes on I_{DS}-V_{GS} characteristics are observed on JL devices [78,79,101] However, due to the high substrate dopant concentration, the carrier mobility on low electric field is severe reduced on JL transistor when it is compared to 3D MOSFET devices. With this, lower drain current (I_D) and trans-conductance values can be expected for JL devices [78].

APPENDIX 4

ENVIRONMENT, SAFETY AND HEALTH (ESH) PROTOCOLS

The experimental work of this thesis was performed at the Center for Semiconductor Components (CCS), located at the University of Campinas (UNICAMP), and at Interuniversity Microelectronics Centre (IMEC) in Belgium. In both Centers, all personnel is obliged to follow various environment, safety and health (ESH) trainings. The trainings and safety procedures are almost the same in both Centers. The ESH trainings cover the general safety in the lab, the correct use of chemicals and wet benches, and how to handle emergency situations. Prior to any type of experiment, the safety issues are discussed with the room responsible and the material safety data sheet (MSDS) of the chemicals are consulted and if required discussed with the ESH department. In addition, during each experiment, the required personal safety items (such as: clean room clothes, safety shoes, safety glasses, gloves) have been worn. Furthermore, all the available chemicals were already preinstalled on the processing tools and the replacement of those chemicals is done by the trained tool responsible at both, CCS and IMEC clean rooms. Moreover, before being able to operate any tool inside the clean room, every personnel is trained by the tool responsible. At CCS, a training record will be maintained listing a person's competency for an

item of equipment. This competence will be graded as either *User* or *Expert*. An *User* may use the equipment, within the guidelines given in the clean room Operating Instructions for the equipment. An *Expert* will additionally be able to reconfigure the equipment, and train people to be *Users*. Additionally, all exposures and plasma etch experiments were executed on the processing reactors following either CCS's and IMEC's policy and regulations regarding the exposure to electromagnetic radiation, and the use of toxic gasses. Also, chemical etches were part of this work and they were done by responsible staff and processing tools. No deviation from the standard way of working, approved by CCS's and IMEC's EHS department, was required.