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Faculdade de Engenharia Elétrica e de Computação

Leonardo Sulato de Moraes

Design of a RF Frequency Divider for an IEEE802.15.4g Transceiver

Projeto de um Divisor de Frequência RF para um Transceptor IEEE802.15.4g

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Supervisor: Prof. Dr. Fabiano Fruett

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Abstract

This work presents the complete process, from design to testing, of an CMOS frequency divider. The divider is based on DSTC (Dynamic Single-Transistor Clock) topology and aimed to work with input frequencies of at least 2 GHz and presenting low output phase-noise. The circuit is integrated in a full transceiver and fabricated in TSMC 65 nm CMOS RF-MS technology. The complete divider block is comprised of two divider cores and buffers occupying an area of 132.72μm x 58.79μm in total, with the divider core itself being 30.92μm x 46.94μm.

Design cycle issues, for example, tool licensing problems, rendered it impossible to obtain the circuit parasitic extraction. These resulted in a fabricated circuit that requires an over-voltage to operate accordingly to its original specification. The circuit characterization is made through indirect measures since the divider outputs are not available for probing. For the circuit input, an external signal generator with well-known characteristics is utilized to generate the signals.

Considering the over-voltage condition the circuit shows an input frequency range greater than 2 GHz and a phase-noise of -135 dBc/HZ at 1 MHz offset frequency. In this condition, the results proved to be within the expected behavior and thus, the proposed circuit is considered functional.

Keywords: Frequency divider; DSTC; Integrated circuits.

Resumo

Este trabalho apresenta o processo completo de desenvolvimento de um divisor de frequência CMOS, do projeto aos testes de caracterização. O divisor é baseado na topologia DSTC e tem como objetivo trabalhar com frequências de entrada de pelo menos 2 GHz e apresentar um baixo ruído de fase de saída. O circuito é integrado em um transceptor completo e fabricado na tecnologia TSMC 65 nm CMOS RF-MS. O bloco completo é composto por dois divisores e *buffers* de saída ocupando uma área total de 132.72μm x 58.79μm, sendo que cada divisor individualmente ocupa 30.92μm x 46.94μm.

Dificuldades durante o fluxo de projeto, como por exemplo problemas com licenças para ferramentas, tornou impossível realizar a extração de parasitas. Isso resultou em um circuito fabricado que requer sobretensão para operar de acordo com suas especificações originais. A caracterização do circuito é feita através de medidas indiretas, uma vez que as saídas do divisor não estão disponíveis para acesso com *probes*. Um gerador de sinal externo, com características conhecidas, é utilizado para gerar os sinais de referência para as entradas do circuito.

Considerando a condição de sobretensão, o circuito mostra uma faixa de frequência de entrada maior que 2 GHz e um ruído de fase de -135 dBc/HZ em um *offset* de frequência de 1 MHz. Nessa condição, os resultados se mostram dentro da performance esperada, validando portanto que o circuito é funcional.

Palavras-chave: Divisor de frequência, DSTC, Circuitos integrados.

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List of abbreviations and acronyms

AWG	Arbitrary Waveform Generator
CEITEC	Centro Nacional de Tecnologia Eletrônica Avançada
CCSNano	Cetro de Componentes Semicondutores e Nanotecnologia
CML	Current Mode Logic
DANL	Displayed Average Noise Level
DSTC	Dynamic Single-Transistor Clock
DRC	Device Rule Checking
DUT	Device Under Test
EVM	Error Vector Magnitude
FIB	Focused Ion Beam
FSK	Frequency Shift Keying
GSM	Global System for Mobile Communication
HTTP	Hypertext Transfer Protocol
ILFD	Inject-Locked Frequency Divider
LNA	Low-Noise Amplifier
LO	Local Oscillator
LVS	Layout Versus Schematic
MAC	Media Access Control
OSI	Open System Interconnection
PEX	Parasitic Extraction
PLL	Phase-Locked Loop
PSS	Periodic Steady State
PVT	Process, Voltage, and Temperature
QFN	Quad-Flat No-Lead

RF	Radio Frequency
RFDAC	Radio Frequency Digital-to-Analog Converter
RO	Ring Oscillator
SCPA	Switched Capacitor Power Amplifier
SEM	Scanning Electron Microscope
SMTP	Simple Mail Transfer Protocol
TSPC	True Single-Phase Clock
VCO	Voltage Controlled Oscillator

List of symbols

$\Delta\theta$	Phase Error
ϵ	Amplitude Error
η	Drain Junction and Miller multiplication effect
k	Boltzmann Constant
Ω	Resistance
ω	Angular Frequency
ϕ	Phase Difference

Contents

1 Introduction

This dissertation is dived in four chapters where the process of design and measurement of a Radio Frequency (RF) frequency divider is presented and discussed. Chapter 1, Introduction, presents an overview on communication systems as well on application and functionality of the proposed circuit and the bibliographic revision. In Chapter 2, Circuit Specification and Design, it is presented the proposed circuit design and simulation results to demonstrate circuit functionality and expected performance. In Chapter 3 the utilized test procedure and equipment as well as results from fabricated circuit measurements are presented. Finally, Conclusion summarizes the obtained results from this work and propose possible future work.

1.1 Communication system overview

Any system, from simple devices such as remote controllers to complex structures such as satellite communication systems relies on wireless data transmission.

Although vastly different one from another, from an end user point of view, communications systems can usually be described by a conceptual model known as Open System Interconnection (OSI) model. This model is used to describe a communication system independently of its actual implementation and hardware and relies on a layered structure with interconnection between subsequent layers. The reference structure as defined in [1] comprises of seven layers named from top to bottom as Application, Presentation, Session, Transport, Network, Data Link, and Physical and is shown in Figure 1.1.

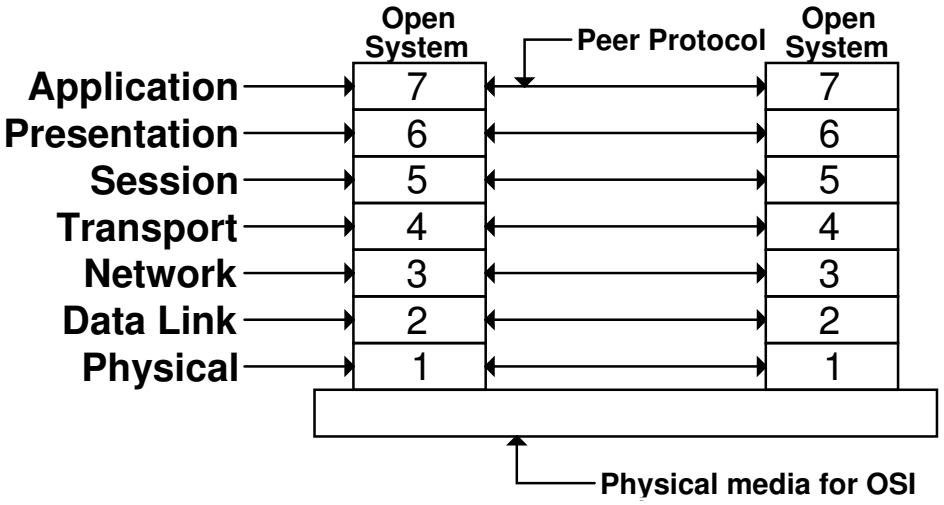


Figure 1.1 – Reference seven layer structure from OSI model (Adapted from [1]).

Each layer is responsible to perform a function as to when all combined create a system that is capable of interoperability with other systems. A brief description of each layer function is as follows.

- **7 - Application:** this layer, being the topmost one, is responsible to provide protocols and data to software applications that in turn, the end-user interacts with. The software itself is not part of the Application layer but relies on it to establish communication. Examples of protocols utilized in this layer are Hypertext Transfer Protocol (HTTP) and Simple Mail Transfer Protocol (SMTP) while software that interacts with this layer would be any web browser.

- **6 - Presentation:** this layer is responsible mainly to prepare the data to the Application Layer employing encryption, compression, and translation. The compression process is used to improve the communication speed by reducing the amount of data that is transferred between layers 7 and 5. Translation is responsible to make data intelligible between two devices that may be using different encoding methods and thus passing data that is coherent to the Application layer. Finally, if the connection between the devices is encrypted this layer also implements the process of decryption/encryption before passing the data to the next layer.

- **5 - Session:** this is the layer that establishes, manages, and closes the communication between devices. This process involves, for example, to determine how long a device should wait for a response when trying to communicate with another and how long a connection should last to ensure that all data is transmitted.

- **4 - Transport:** this layer is responsible to control the data flow between the devices, such as to define data rate appropriate for a given connection, where to send the data, and how much data is being transmitted. In this layer, on the transmitter side, data is broken into blocks designated as segments. On the receiver side, the transport layer reassembles the segments before passing to the next layer. Transport layer is also responsible to determine if the data was successfully transmitted and re-transmits it if any error is found.

- **3 - Network:** this layer simplify the data between different networks. In the transmitter, the segments data from layer four are further broken down into smaller chunks known as packets. In the receiver, an analogous process occurs where the packets are reassembled into segments. The network layer provides the address between devices to allow identification and routing for data transmitting.

- **2 - Data Link:** similarly to what the Network layer does for devices in different networks the Data Link layer acts when the devices are on the same network. This layer takes the packets from the previous layers and further breaks them down into

smaller sections called frames. This layer also handles flow and error control for communications in the same network.

- **1 - Physical:** finally this layer includes the actual physical equipment which handles the data transfer. The physical layer is also the one responsible to convert the data into a bitstream.

When implementing a system based on this model, in general, layers seven to four are implemented through software/programming while the other layers (three to one) are implemented on hardware. The IEEE802.15.4g specification [2], which is the scope where this work is inserted into, addresses two of seven layers of the OSI model. The media access control (MAC), which relates to the Data Link layer, and the Physical (PHY) which relates to the one with the same name in the OSI model and in which this work is included. Most of the IEEE802.15.4g documentation refers to the specification of structures needed for data processing to create a compliant signal with the standard which are implemented using digital blocks which when combined creates the modulator and the demodulator.

Figure 1.2 shows the proposed reference modulator that should be implemented for this standard. In this reference modulator it is possible to note that the output signal is noted as "RF". This signal is the one that should go trough analog circuitry to then be transmitted at an certain frequency. An analogous process happens when receiving data. The standard specification just defines certain performance parameter that the analog transmitter and receiver should comply such as output minimum output power, receiver sensitivity, frequency deviation, and spectral mask but does not defines a specific architecture to be used in the analog circuitry and thus leaving to the system designer to define what to use.

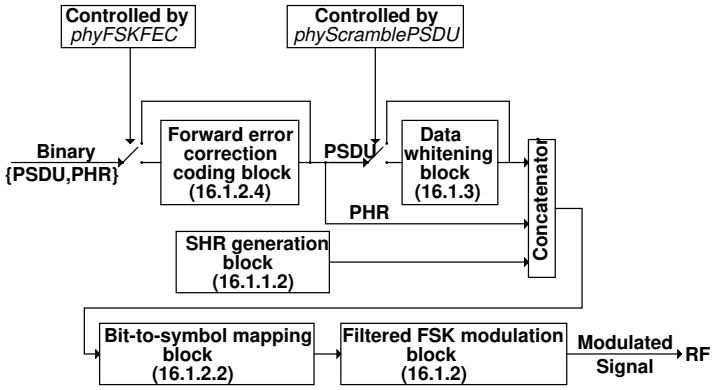


Figure 1.2 – Reference Frequency shift keying (FSK) modulator. (Adapted from [2].)

1.1.1 Transceiver Architectures

The Radio Frequency (RF) transceiver is composed by the junction of the transmission and the reception system which does the linking between the digital modem and the radio frequency signals. Although several options on how to implement the transceiver exists the target objective is always the same. In the transmission path, the signal coming from the baseband modem is converted from digital to an analog waveform that is then up-converted to the desired RF frequency and amplified by a power amplifier (PA). The opposite process happens for the reception path. The RF signal coming from the antenna goes through a low-noise amplifier (LNA) and frequency down-conversion before converting from analog to digital domain and be to the baseband modem. Figure 1.3 shows a generic transceiver architecture. It is possible to observe in the figure that the Local Oscillator (LO) is not in the direct path of the received/transmitted signal but provides signal for both and thus any degradation in this block impacts the system as a whole.

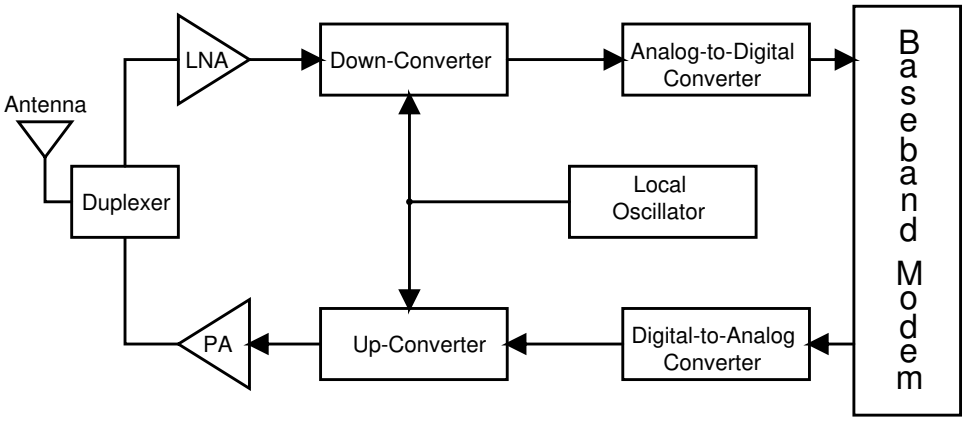
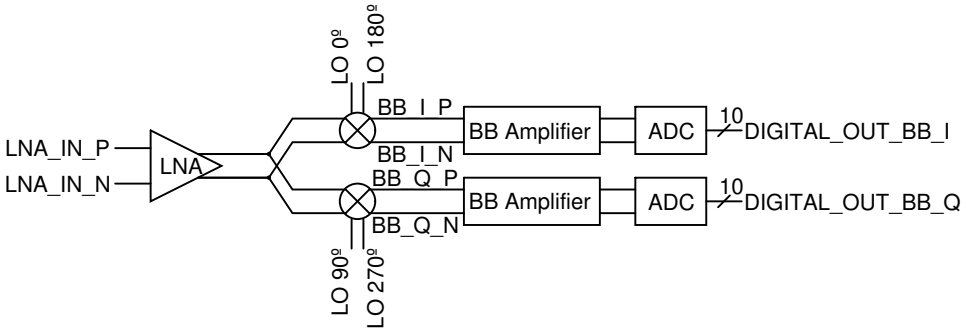


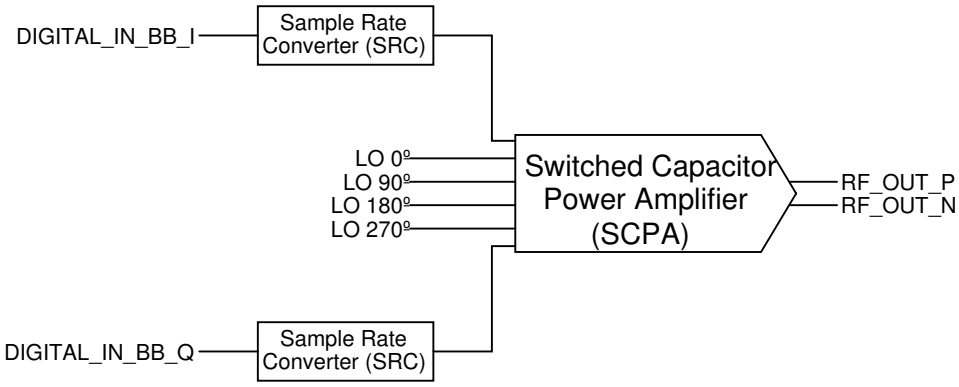
Figure 1.3 – Generic simplified transceiver architecture.

The project in which this work is inserted into utilizes for the receptor path a superheterodyne, also called Low-IF, receiver and the transmitter is based on a IQ-Sharing [3] transmitter. The diagram for both are presented in Figures 1.4a and 1.4b. In both signal paths it is observed that the LO should provide differential signals in-phase (LO 0° and LO 180°) as well quadrature (LO 90° and LO 270°) and thus adequate LO topology should be used to provide these signals.

It is possible to observe that, in both transmitter and receiver paths, differential signals are used. This choice is made since, although there is an increase in area, it is known that differential signaling is more resistant to electromagnetic interference, minimizes cross-talk, and inherently cancels even order harmonics.



(a) RF receiver Low-IF topology.



(b) RF transmitter IQ-Sharing topology.

Figure 1.4 – Topology used in the transceiver.

1.1.2 Local Oscillator

The common choice to implement the LO is to use an Phase-Locked Loop (PLL). This circuit consist in a closed-loop system which by using a stable low frequency reference signal, usually provided by crystal oscillators, controls an higher frequency oscillator. The fundamental blocks of this circuit, as shown in Figure 1.5, are the phase detector, low-pass filter, voltage controlled oscillator (VCO), and loop divider. The phase detector is responsible to detect the difference between the reference signal and the feedback signal and create a control signal that indicates if the oscillator frequency should go up or down. The low pass filter is used to reject spurious high-frequency tones as well noise from the control voltage and create a smooth control voltage to ensure stable operation and control of the oscillator. The loop divider takes the high frequency oscillator output and divides it back in a ratio that should make it equal to the reference frequency. Controlling the ratio of the divider is used to choose the system output frequency. At last, the oscillator is the one actually responsible to create the high frequency signal which can be implemented using several different topologies that can grouped into two general categories: ring oscillators (RO) and LC-oscillators.

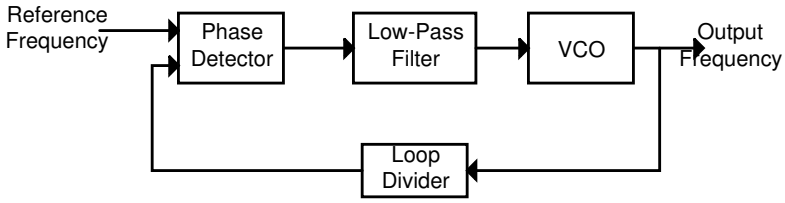


Figure 1.5 – Generic PLL Configuration.

Considering that quadrature outputs are required, some options are possible to obtain it. One is to use an direct frequency synthesis, in which the oscillator works at the system frequency and create the quadrature outputs by either coupling two identical oscillators operating at 90° phase difference or by using just one oscillator and passing its output through RC networks to create the desired phase difference. Another method is to use an oscillator working at double the system frequency and then passing its output signal trough a divide-by-two circuit. The use of a direct frequency synthesis approach rises a concern with an effect known as LO-pulling. As described in literature ([4]; [5]), this phenomena consists in the coupling of the high power modulated signal from the PA coupling back to the VCO and causing a corruption, adding noise, and even deviating the operating frequency, thus in a system which is has a power amplifier this option is not advised. The use of RC networks are also not feasible due to the required area, thus the decision is to use the synthesize the signal at double the frequency.

The frequency divider that is used in to create the quadrature outputs should then follow severe specifications to try keeping the signal from the VCO as intact as possible keeping a clean spectrum and low noise. Also, the same divider can be used on the PLL loop divider block since usually the digital implementation used in these circuits cannot operate at the frequency provided in the VCO output and thus analog dividers are used to handle the initial divisions.

1.2 Motivation and Objective

Given that a frequency divider is almost certain to be present on a transceiver, be it on a PLL loop divider or to generate the system working frequency and quadrature signals, this circuit is an important building block inside the system. Literature ([6], [7], [8]) addresses different concerns regarding this kind of circuit and how to implement it to optimize the divider performance be it related to operating operating frequency range, area, power consumption, noise or the circuit implementation complexity. Given the various possible manners in which to implement an frequency divider this work intends to find a topology that fulfils the requirements imposed by the system specification derived from the IEEE802.15.4g in which it is to be present. The proposed frequency divider circuit is then designed, fabricated and characterized to check its performance and compare to the expected requirements.

1.3 Bibliography Review

There are currently several different ways to implement frequency dividers available in the literature, ranging from simple and well-known topology such as digital implementation using logic gates, to more complex topology such as Injection-Locked Frequency Dividers (ILFD) which relies on harmonics generation and filtering. In this dissertation, the following topologies are selected for discussion.

- Injection-Locked Frequency Divider (ILFD)
- Digital Dividers
  - Current Mode Logic (CML)
  - True Single-Phase Clock (TSPC)

1.3.1 Injection-Locked Frequency Divider (ILFD)

This kind of topology is able to achieve high-frequency operation while keeping a considerably low consumption and thus becoming a popular topic for the development of dividers suitable for applications such as radars [9] and even emerging 5G [10]. This topology, in which the most simple implementation is presented in Figure 1.6 consists of an oscillator which, instead of working at its resonant or free-running frequency, will be working locked at a sub-harmonic of the injected signal (V_{INJ}) to be divided. The working principle of this circuit is the following. If the gate signal (V_{INJ}) of transistor M3 is just a DC signal, the circuit will be working in its free-running mode. Transistor M3 will act as a fixed current source for both transistors M1 and M2. In nodes V_{OUTP} and V_{OUTN} it will be present a signal at the resonant frequency $\omega_0 = 1/\sqrt{L \times C}$, in node V_m there will appear a signal at 2 times the output frequency due to contribution of both current branches. If we were now to superimpose an AC signal with frequency ω_1 to the V_{INJ} the node V_M will be forced to oscillate at the same ω_1 frequency which will in turn cause transistors M1 and M2 to act as mixers due to the switching of the drain current injected by M3. At the output, it will be observed all the even harmonics starting from the first sub-harmonic of ω_1. The LC tank circuit then filters the higher-order harmonics leaving only the desired $\omega_1/2$ component. A more in-depth approach to ILFD circuits modeling can be found in [11] and [12]. Since in this work the proposed circuit is required to provide quadrature outputs, in Figure 1.7 is presented one of the most common approach to couple two of such dividers in a way that quadrature outputs are generated.

It is possible to observe that this topology presents two concerns, one is the occupied silicon area since it is necessary to have an inductor in the circuit. The other problem is the so-called locking range, which is the range of input frequency that the divider is able to operate, This concern arises from the fact that since this divider is based

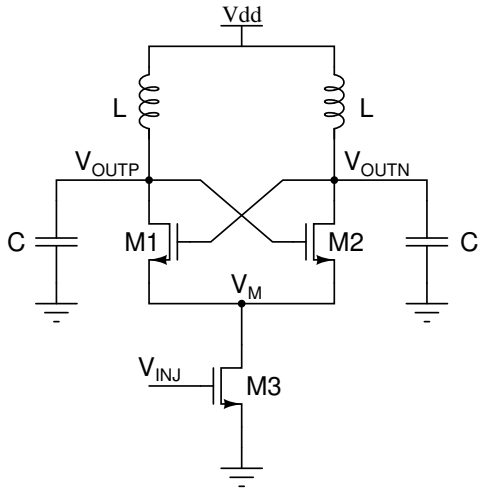


Figure 1.6 – ILFD circuit diagram.

on an oscillator the locking range will be usually restricted to a close range of resonant frequency ω_0. There are several works such as [10] and [8] which addresses methods of extending the locking range of the circuit at cost of complexity.

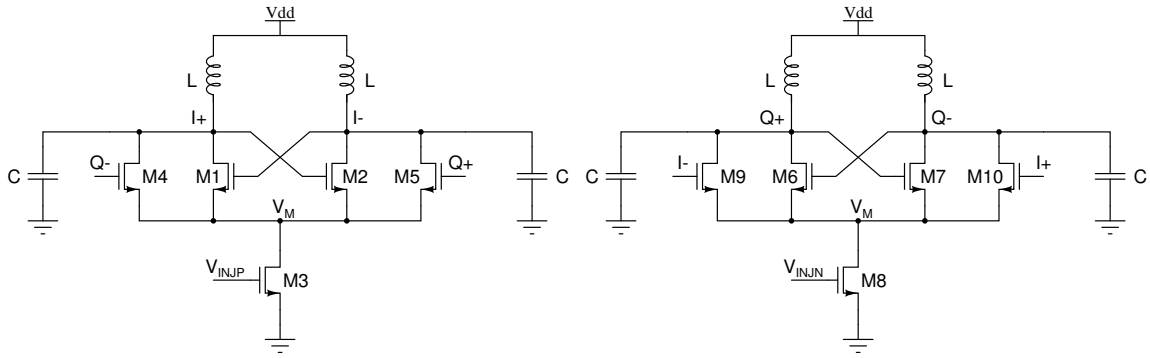


Figure 1.7 – Quadrature ILFD circuit diagram.

1.3.2 Digital Dividers

Another method of implementing a frequency divider is to explore more common digital implementations such as a divide-by-two block using flip-flops connected in negative feedback as presented in Figure 1.8. The main factor that will limit operation frequency in this kind of topology is the way in which the individual flip-flop is implemented. Among several topologies found in the literature, two options stand out due to their high operation frequency capability. Following are presented the ones that comply with the requirements in this work.

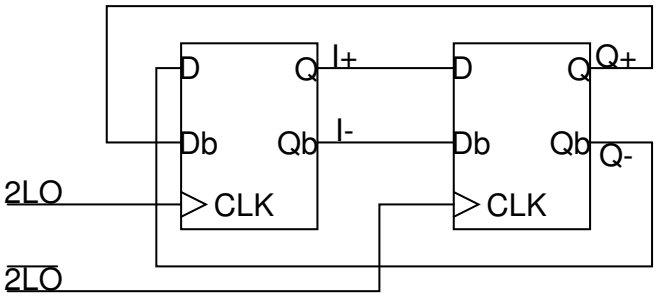


Figure 1.8 – Top level divide by two using two latches.

1.3.2.1 Current Mode Logic (CML)

CML logic consists in a differential logic family where in order to achieve high-speed operation instead of switching voltage, current signals are switched to create the desired output. The output voltage created by this current switching usually has a smaller amplitude to allow faster switching times. The most common CML latch topology is presented in Figure 1.9, where only one load is shared between both tracking and hold stages, and the load type is a passive resistor. Although there is the possibility to also use inductors instead of resistors this option is not considered due to the area penalty that it implies.

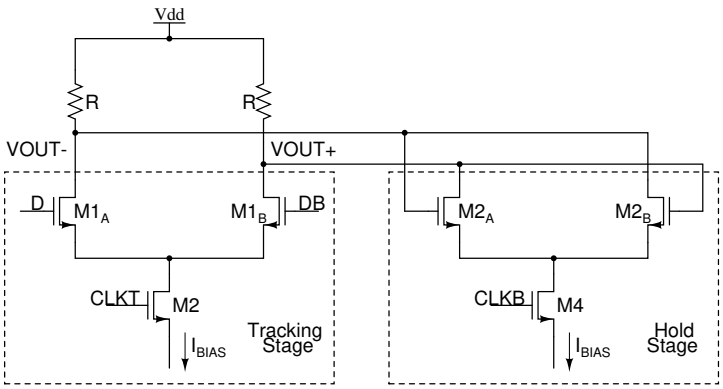


Figure 1.9 – CML logic flip-flop circuit.

The operation of this circuit is as follows: whenever signal CLKT is high and CLKB is low, the latch tracking stage is active meaning that depending on the value of the differential input signal $V_D - V_{DB}$, the bias current (I_{BIAS}) will flow through only transistor $M1_A$ or $M1_B$. In turn, whenever signal CLKT is low and CLKB is high, the hold stage will be active and is responsible for holding the previous state voltage by means of switching the differential pair composed by $M2_A$ and $M2_B$. As stated before this circuit allows high-speed operation through current switching and smaller voltage output

amplitude given by Equation 1.1.

$$V_{OUT} = V_{OUT_{max}} - V_{OUT_{min}} = VDD - \left[VDD - R \cdot \frac{I_{BIAS}}{2}\right] = R \cdot \frac{I_{BIAS}}{2} \tag{1.1}$$

The switching speed of this circuit is directly associated with the capacitance present in node V_{OUT-} and V_{OUT+}, thus it is possible to show that the minimum required current for a given speed and load requirement is as given in Equation 1.2. Where ΔV is the minimum amplitude for switching on a transistor in the technology, C_{GD} and C_{DB} are the MOS transistor capacitance, C_{PAR} is the parasitic capacitance, Δt is the required transition time from high to low logic level, usually expressed as a percent of the waveform period, and (C_L) is the capacitance of the circuit which is being driven by the CML divider.

$$I_{BIAS} = (C_L + C_{GD} + C_{DB} + C_{PAR}) \cdot \frac{\Delta V}{\Delta t} \tag{1.2}$$

In literature, examples of inductorless high-frequency CML dividers such as [13], [14], demonstrates that this topology is able to achieve high-frequency operation while still presenting a high locking range. In both works, the presented power consumption is low, being 6.6 mW the highest reported. This is due that only the divider core circuit is taken into consideration and the needed buffers to drive the desired load is not presented.

1.3.2.2 True Single-Phase Clock Dividers (TSPC)

The TSPC concept was first proposed in [15] as a method of creating dynamic logic which requires, as stated by its name, only a single phase of the clock signal to operate. This principle was further extended in [16], in which the TSPC basic stages shown in Figure 1.10 are utilized to create improved both single-ended and differential flip-flops.

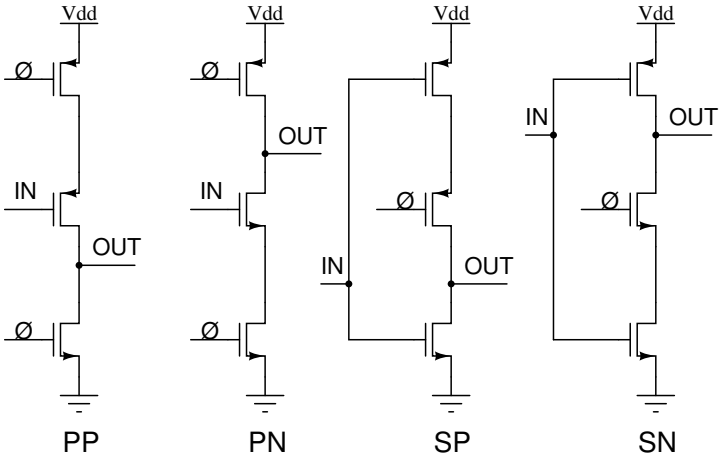


Figure 1.10 – TSPC basic building blocs. (Adapted from[16].)

This topology advantage resides in being a dynamic logic structure which reflects in low power consumption. Initially, this topology was limited to relatively low frequencies compared to the ones desired in this work but with CMOS technology scaling, and consequently transistor's maximum operation frequency f_t increase. It was later shown in [6] that the TSPC logic family could achieve operating frequencies above 15 GHz in a 65 nm CMOS technology. The main concern for this topology is that in this work it is required full differential outputs while operating in frequencies above 1 GHz, and since TSPC structures are mainly used in digital circuits where differential signal are not always required, examples of high-speed operation with differential configuration as shown in [16] such as the one in Figure 1.11 are quite scarce. The most recent publication found regarding this topology is [7]. In this paper, according to Table 1.1, when looking at the propagation delay parameter of DSTC flipflops using either 180 nm or 90 nm technology, the maximum operating frequency is far below the desired. This is respectively shown in Equations 1.3 and 1.4. In both equations setup time (Ts) is ignored.

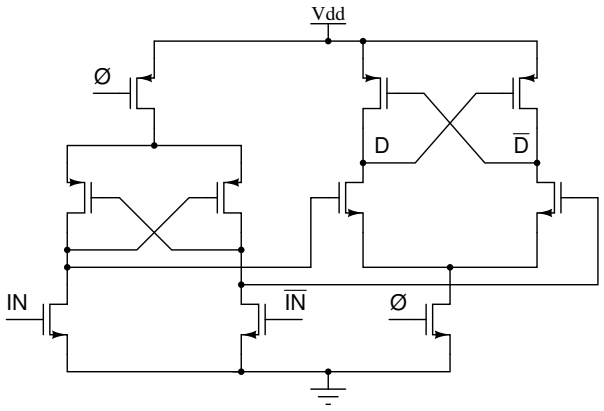


Figure 1.11 – Dynamic differential flip-flop. (Adapted from [16].)

$$Freq = \frac{1}{T_{prop} + T_s} = \frac{1}{2.32 \cdot 10^{-9}} = 431\ MHz \tag{1.3}$$

$$Freq = \frac{1}{T_{prop} + T_s} = \frac{1}{1.81 \cdot 10^{-9}} = 552\ MHz \tag{1.4}$$

A different approach for a TSPC divider is found in [17]. In this case, the proposed circuit presents true differential outputs created from a single input as shown in Figure 1.12. This topology uses two conventional single-ended TSPC dividers coupled by a resistor (Rc). The coupling of the output of one divider (node OUT^+) to the first stage of the second divider (node X^-) enforces an out of phase operation in this node which in turn propagates to the output creating the differential output. As stated in [17], the value of the coupling resistor should be carefully chosen to ensure that the pull-up and

Table 1.1 – Performance Parameters Table (Adapted from [7].)

Design Style	N° of Transistors	Width of NMOS (μm)	Length of PMOS (μm)	Avg. Power Comm (Watts)	Prop Delay (n/sec)	Prop. Delay Product (w/sec)
D Flip Flop using GDI using 180nm	18	.64	1.7	2.49×10^{-5}	2.65	6.59×10^{-14}
D Flip Flop using GDI using 900nm	18	.64	1.7	1.72×10^{-5}	1.79	3.07×10^{-14}
DSTC using 180nm	12	.64	1.7	1.91×10^{-6}	2.32	4.43×10^{-15}
DSTC using 90nm	12	.64	1.7	1.23×10^{-6}	1.81	2.22×10^{-15}

pull-down of node X^- will be done in time before either the input signal IN or the signal OUT^+ changes and is defined by Equations 1.5 and 1.6.

$$VDD \cdot \frac{R_{on}}{2R_{on} + Rc} \cdot \left[1 - e^{-\frac{T}{2[Ron//(Ron+Rc)]Cp}}\right] > (V_{th} + V_{sat}) \tag{1.5}$$

$$VDD \cdot \frac{R_c + 2R_{on}}{R_c + 4R_{on}} \cdot \left[1 - e^{-\frac{T}{2[2Ron//(2Ron+Rc)]Cp}}\right] < (V_{th} + V_{sat}) \tag{1.6}$$

In these equations R_{on} represents the channel resistance of transistor connected to node X^- and T is the period of the input signal.

This work ([17]) presents promising results since its operating input frequency range goes from 600 MHz to 5 GHz while keeping a small area in an 0.18μm. The only downside of this implementation is the use of a resistor and some of the other parameter performances such as phase error that limit the direct use of this topology as it will be later explained in Chapter 2.

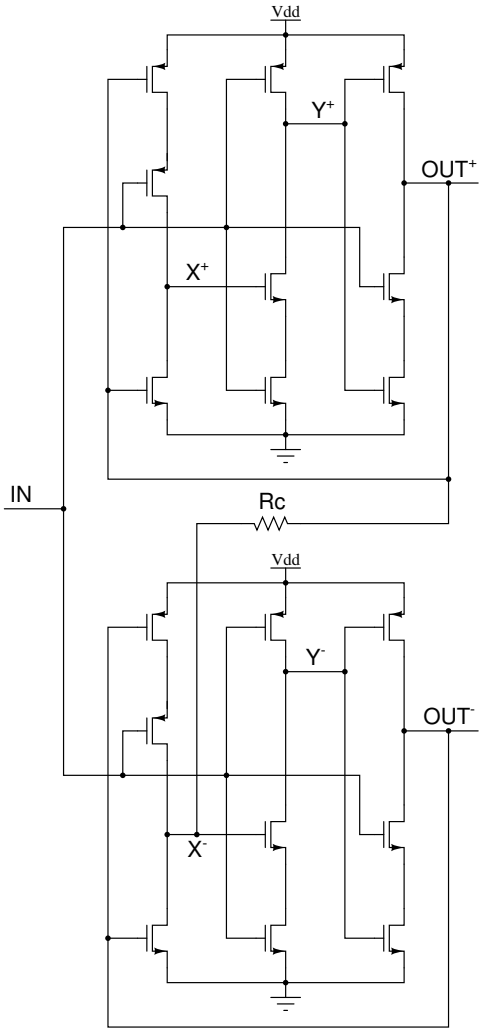


Figure 1.12 – Differential Single input TSPC divider. (Adapted from [17].)

1.4 Conclusion

After investigating the reviewed bibliography we are now required to set for one of the presented topologies to design the desired quadrature divider. In table 1.2 relevant design points and performance parameters of the discussed topology references are summarized.

Table 1.2 – Topology summary

Topology	Operating Frequency	Power	Area	Technology
ILFD [9]	23.03 ∼ 24.24	4.8	NA	65nm
ILFD [10]	19.3 ∼ 23.4	1.51	0.23	0.13μm
CML [14]	25 ∼ 102	2.81 ∼ 5.64	0.000635	28nm
CML [13]	12.5 ∼ 32	6.6	0.000255	22nm
TSPC [17]	0.6 ∼ 5	7 ∼ 12	0.0344	0.18μm

ILFD at first glance may seem to be the best choice since it can achieve high-speed operation while keeping low power dissipation but when considering the need for inductors in the circuit it poses a problem to use this topology since a limited area is available for this project.

When examining the CML implementation, as stated before, current consumption is the main concern. Utilizing Equation 1.2 and plugging in values compatible with the set design technology and required parameters latter explained in Chapter 2 for this project such as 400 mV for ΔV as the minimum voltage to turn on an NMOS transistor, a load capacitance of 300 fF and a transition time of 50 ps a current of 2.4 mA would be required for the tracking stage. Since usually the current for tracking and hold stages are the same this makes the total current consumption 4.8 mA that in turn, for a 1.2 V power supply, corresponds to 5.76 mW for a single CML DFF, thus a quadrature divider, which requires two DFFs would draw 11.52 mW from the power supply. Furthermore, an extra circuit would be needed to convert from CML to CMOS voltage levels to allow coupling between the frequency divider and the rest of the system and thus adding to the power consumption.

Although when comparing the consumption of TSPC circuits to CML presented in Table 1.2 the TSPC topology seems to be at a disadvantage. But it is to note the fact that the TSPC circuit was fabricated in an older technology and also that, as previously stated, the power reported for the CML circuits is only for the divider core and not take into account the driving circuits for the load. Thus to properly compare the power consumption results data for TSPC topology from [6] is shown in Table 1.3 as an excerpt from the original table present in the paper. When using the highest power consumption of 0.022 mW/GHz and considering an input frequency of 1.8 GHz the total power for a divider is 39.6 μW. Since this structure is a dynamic circuit and power will mainly depend on the existing nodes capacitance, it's expected that the power for a TSPC divider will increase since the desired load capacitance to be driven is 300 fF, but it is expected to be significantly lower than a CML counterpart and thus being the choice for designing a differential frequency divider.

Table 1.3 – Performance Parameters Table Excerpt. (Adapted from [6])

Design	Technology	Fixed Divide-By-2	
		$f_{in,max}$[GHz]	Power[mW/GHz]
RE-1	65 nm LP	15	0.020
RE-2	65 nm LP	19	0.017
RE-3	65 nm LP	18	0.020
RE-4	65 nm LP	21	0.022

2 Circuit Specification and Design

In this chapter, at first, is presented the system of which the circuit is part. Next is shown the desired performance metrics and the impact on the overall system. The proposed circuit design is then presented and discussed concerning the design points that are most relevant to the desired metrics. Lastly, the testbench overview and simulation results are presented and discussed.

2.1 Architecture Overview

The frequency divider in this project is to be designed as part of a larger project that contemplates an IEEE802.15.4g compliant transceiver. The block diagram is shown in Figure 2.1. As can be seen in this diagram, the frequency divider is the last block in the Local Oscillator (LO) signal generation chain. The divider is responsible for providing signals to three different structures, the baseband modem digital front-end, the receive mixer, and the transmitter structure. The transmitter is composed of the RF Digital-to-Analog Converter (RFDAC), which operates directly at the transmitter frequency, and the switched capacitor amplifier.

The frequency divider signals required for the RF transmitter are four, which work at the desired transmission frequency and should have a 90° phase lag between one another. These signals, usually called quadrature signals, will be generated by frequency division from the Phase-Locked Loop (PLL) differential output signal. These same signals are also required for the mixer on the receiver side to perform the RF signal down conversion. The signals for the baseband modem digital front-end are simply a further division from the RF frequency. These signals are needed by the digital circuits responsible for up-sample the baseband signals to the required sample rate of the RFDAC.

When looking at the requirements for the divider signal from these three different blocks, it is noted that the transmitter has the most stringent parameters, and thus, it is the block that determines the performance metrics to be achieved by the divider.

2.2 Performance Specification

The main specifications for a frequency divider are related to the frequency range in which it can operate, and how precise the frequency division is performed. Since this work is related to an integrated circuit, concerns related to circuit area and power consumption also exist. Below each design specification is presented and discussed.

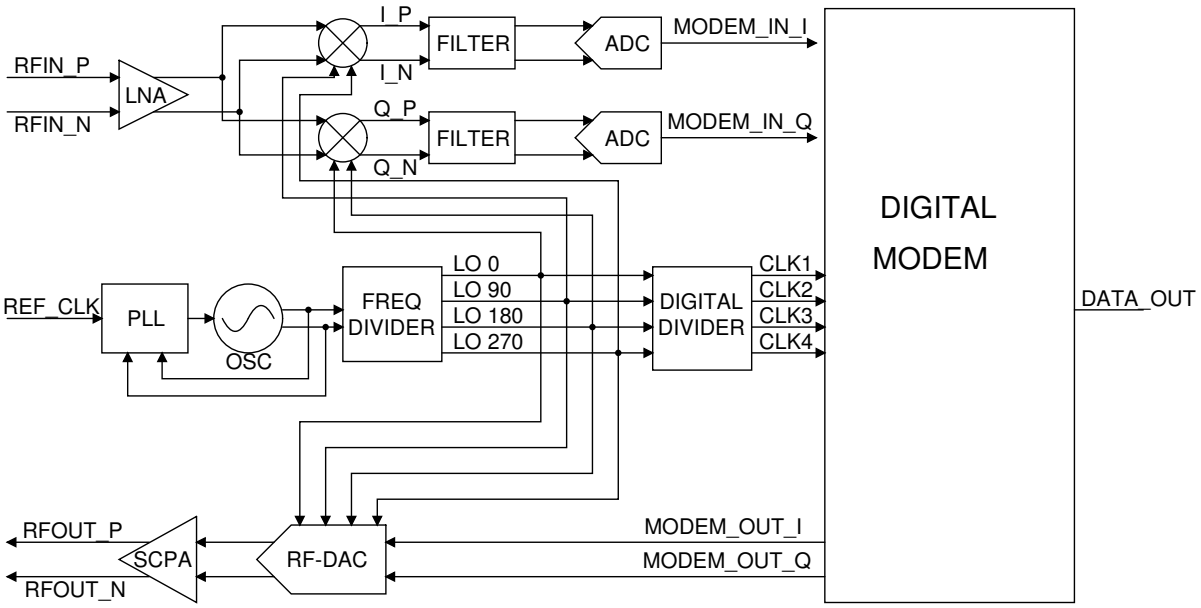


Figure 2.1 – Top level block diagram for the complete IEEE802.15.4g compliant system.

2.2.1 Input Frequency Range

This is the first and most basic specification of a frequency divider and comes from the system in which it is integrated. In this project, the circuit should be compliant with the following IEEE802.15.4g PHY's: 450 MHz, 863 MHz, 896 MHz, 901 MHz, 915 MHz, 928 MHz as defined in Table 66 presented in [2]. The highest frequency specified in the 928 MHz PHY is 960 MHz. Thus the highest input frequency that the divider should operate is at least 1.92 GHz. For simplicity, it is considered that the mandatory input frequency range specification is 2 GHz. Considering that IEEE802.15.4g also defines operating frequencies in the 1427 MHz and 2450 MHz range, it is desired but not mandatory to achieve an input frequency of 5 GHz as a secondary goal.

2.2.2 Phase Error

A second specification for the frequency divider is the capability of keeping the signals with ideal phase alignment. The baseband signal that will be fed into the transmitter has an IQ modulation Thus the LO should also provide quadrature signals with 90° phase difference between them in the up-conversion process. This requirement is important since perfect phase alignment in the LO signal suppresses signal image in the negative spectrum band in an effect known as sideband suppression. This effect happens due to the fact that IQ modulation has 90° phase difference. When combining the real and imaginary parts of both In-phase (I) and Quadrature-phase (Q) signals the resulting signal has just a real part in the spectrum, as shown in Figure 2.2.

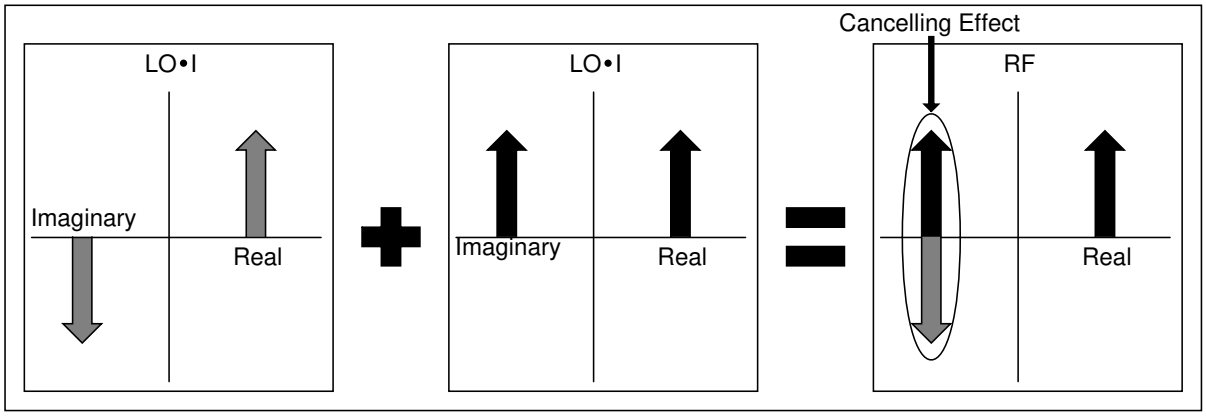


Figure 2.2 – Combination of I and Q signal when LO signal have 90° phase difference.

The phase error between the signals is simply calculated as shown in Equation 2.1. Effect of both phase error ($\Delta\theta$) and amplitude error (ϵ) in the resulting signal after up-conversion in both wanted sideband (P_+) and unwanted sideband (P_-) is shown in Equation 2.2 as deduced in [5]. To achieve a minimum sideband rejection of $-40\ dB$. When considering just phase mismatch in Equation 2.2, it is noted that the maximum acceptable phase error is approximately 1.1°, as its possible to see in Figure 2.3.

$$Quadrature\ Phase\ Error = |\phi(I/Q) - \phi(Q/I) - 90| \tag{2.1}$$

$$\frac{P_-}{P_+} = \frac{(1+\epsilon)^2 - 2(1+\epsilon)\cos(\Delta\theta) + 1}{(1+\epsilon)^2 + 2(1+\epsilon)\cos(\Delta\theta) + 1} \tag{2.2}$$

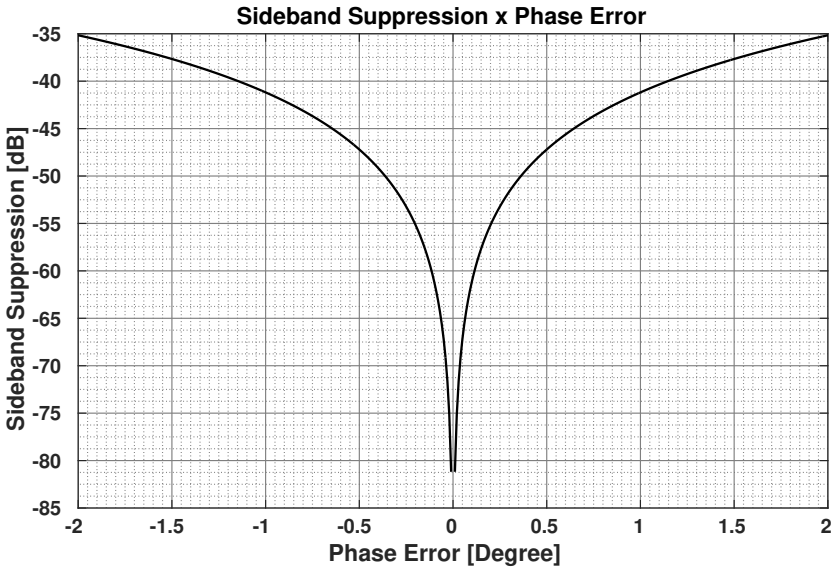


Figure 2.3 – Effect of phase Error in the sideband rejection.

2.2.3 Duty Cycle Stability

An important aspect of the frequency divider output signal is the duty-cycle value and the capability of keeping it stable along with its operation. As discussed in [3] the best Error Vector Magnitude (EVM) for an IQ-Sharing architecture transmitter is obtained when using a 50% duty-cycle when compared to a 25% one as shown in Figure 2.4. From this plot, it is inferred that considering that signal to be transmitted is ideal, to keep EVM below −60 dB the maximum due to duty-cycle variation is 1%. The equations used to plot these curves are presented in Appendix A.

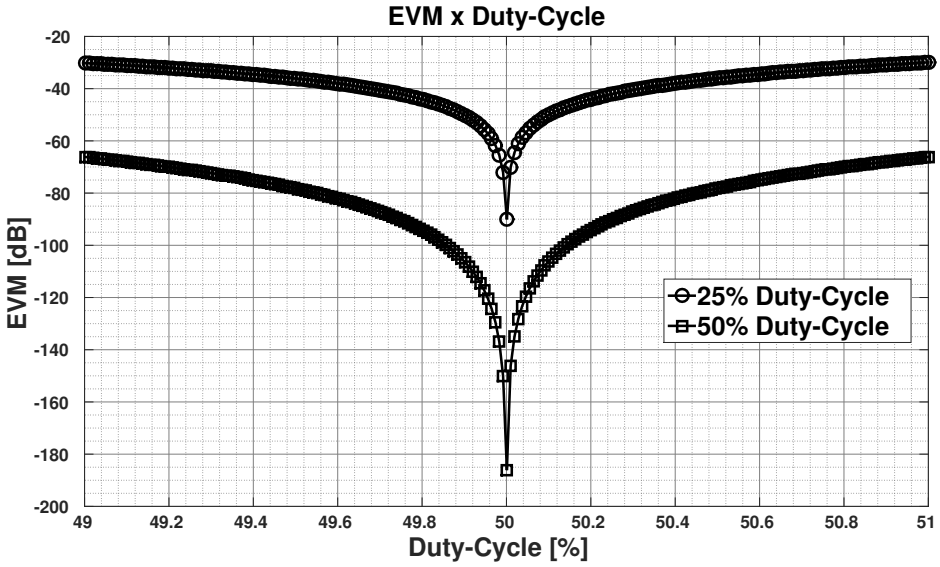


Figure 2.4 – EVM change due to changes in LO Duty-Cycle.

A second factor to be considered is that a 25% percent duty-cycle LO signal presents both odd and even harmonics while a 50% one have just the odd components and thus due to the SPCA switching operation the signal images that will be present at the output will be far of the transmitter carrier frequency and more easily filtered.

2.2.4 Phase Noise

The phase noise specification arises from the need of keeping the transmitter output spectrum in the signal band region the cleanest possible. Phase noise is the frequency domain representation of a periodic signal zero crossing point uncertainty, which is known in the time domain as jitter. A perfect oscillator can have it output represented as $V_{out}(t) = A\text{cos}\omega t$ which is a pure sinusoidal output, but when considering the noise in the circuit the output signal is now written as $V_{out}(t) = A\cos(\omega t + \phi_n(t))$ where $\phi_n(t)$ represents the signal phase variation induced by the circuit noise. The graphical representation of this effect is shown in Figure 2.5. In the frequency domain, the error in the zero-crossing point translates into the spreading of the signal spectrum besides the

ideal signal frequency as shown in Figure 2.6. When the noisy carrier is then mixed with the baseband signal to create the RF signal the wider band of the LO signal will also spread the output spectrum and raise the noise floor. A similar process happens in the reception side during the down-conversion phase. This process can be viewed as if each frequency different from the desired LO frequency is mixed with the signal, which will translate it to a sideband in the RF signal with a smaller amplitude. This is shown for the down-conversion in the reception in Figure 2.7.

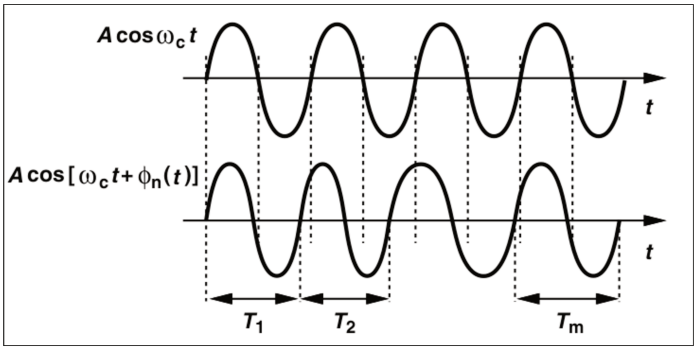


Figure 2.5 – Ideal and noisy waveform in time domain. (Adapted from [5].)

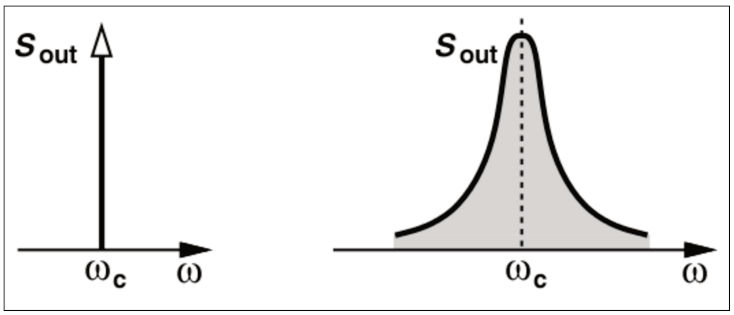


Figure 2.6 – Ideal and noisy waveform spectrum. (Adapted from [5].)

Phase noise is usually separated in the close-in, from carrier frequency till around 1 MHz offset, and far-out regions above 1 MHz where the phase noise settles into the floor level. In this work, it is required to be compliant with the GSM (Global System for Mobile Communications) standard, which is one of the most restrictive in the phase noise specification, and this should achieve a noise floor of -162 dBc/Hz at an 20 MHz offset.

2.2.5 Area, Power Consumption and Specification Summary

In this work, power consumption and circuit area are not restrictive specifications once there were no constraints on the design, but since the intended application for this circuit is an IEEE082.15.4g compliant modem, which is an IoT oriented specification

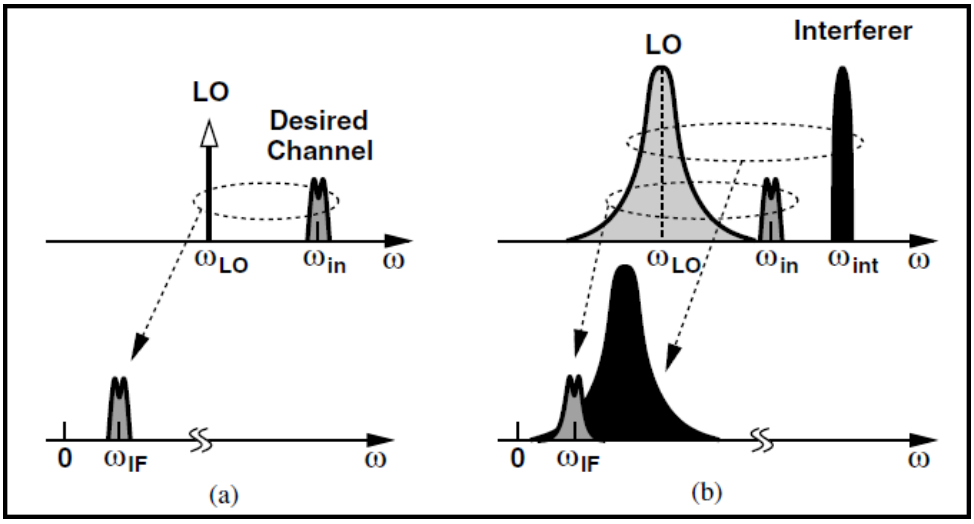


Figure 2.7 – Up-conversion process with (a) ideal LO signal and (b) noisy LO signal. (Adapted from [5].)

some efforts are made regarding these aspects. Power consumption ideally should be low to maximize a potential device battery life. One factor that is important to be taken into consideration regarding the current usage is the LO signal rise and fall times. This specification affects the current since to charge or discharge a certain capacitive load (C_L) in a fixed amount of rise time (t_r) or fall time (t_f) a current (I_{Charge}), as crudely approximated by Equation 2.3 when neglecting internal resistances, is necessary. In this work, the target rise and fall times are 50 ps as required by the transmitter block.

$$I_{Charge} = C_L \cdot \frac{\Delta V}{\Delta t_{r/f}} \tag{2.3}$$

The area is also tried to be kept at a minimum to save silicon area and should ideally be less than $100\mu m \times 100\mu m$. The summary for all proposed target specifications is presented in Table 2.1.

Table 2.1 – Specifications Summary.

Specification	Value	Unit
Input Frequency	≥ 2.0	GHz
Phase Noise	≤ -162 @20 MHz offset	dBc/Hz
Phase Error	≤ 1.1	^{o}
Duty-Cycle Stability	$\leq 1\%$	-
Rise/Fall Time	≤ 50	ps
Power Consumption	–	A
Area	100×100	μ^2

2.3 TSPC Divider

2.3.1 Functional Analysis

The proposed differential topology is presented in Figure 2.8. The circuit core is comprised of a cross-coupled differential pair that creates the differential signals *n1* and *n1b*. The following stages are implemented using the single-ended TSPC stages shown in Figure 1.10. Determining these stages is done by analyzing the signal coming from the previous stage and the function implemented by the TSPC stage. The signal propagation through the divider is presented in Figure 2.9. In nodes *n2* and *n2b* it is observed signals with 75 % that are in phase with the rising edge of the reference clock signal, these signal can also be utilized to derive 25% divided signal from the reference if passed through an inverter and further utilized in a topology that requires this kind of signals such as presented in [18] and [19].

Since TSPC circuits rely on dynamic logic there are certain phases of operation that the nodes *outp* and *outn* presents high impedance and are not able to properly drive the circuit load. Thus inverters are added as the last stage of the divider to isolate the previous node from the load and to adjust the circuit drive capability. Transistors *MRP* and *MRN* are added to the circuit to implement resetting capability to the flip flop by pulling nodes *n1b* to VDD and *n1* to GND when signal *RST* in high. Transistors *MRDN* and *MRN* are added as dummy devices to properly balance the capacitance in nodes *n1* and *n1b* and keep the circuit behavior as symmetric as possible.

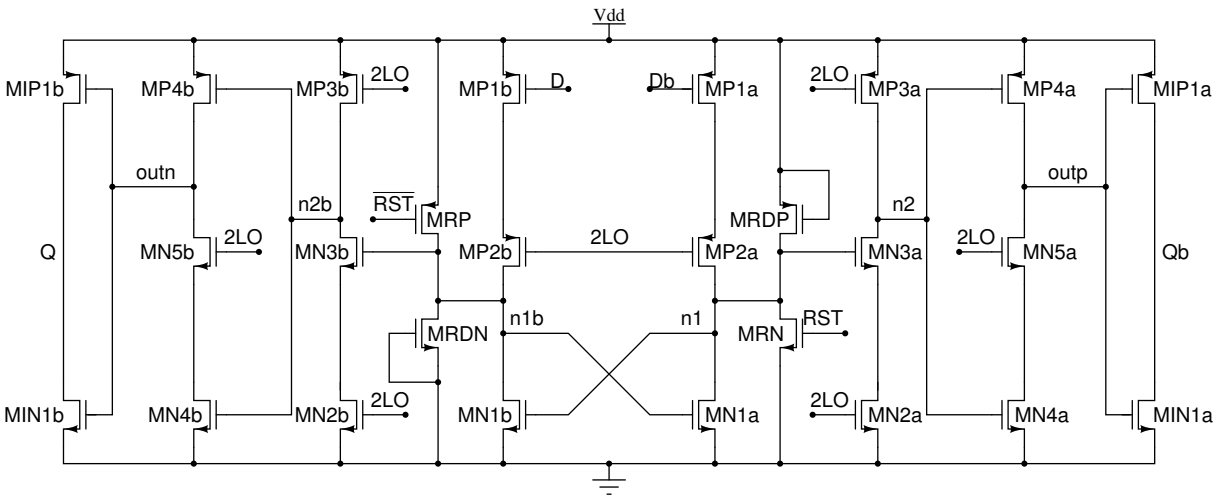


Figure 2.8 – Differential proposed TSPC topology.

The circuit behavior relies on the input clock denominated as *2LO* and can be separated in 4 (four) phases of operation, of just half the circuit for simplicity, as presented in Figure 2.10. This diagram aids in the circuit design by providing insight into which paths are critical for signal propagation. Since the desired duty-cycle is 50%, the

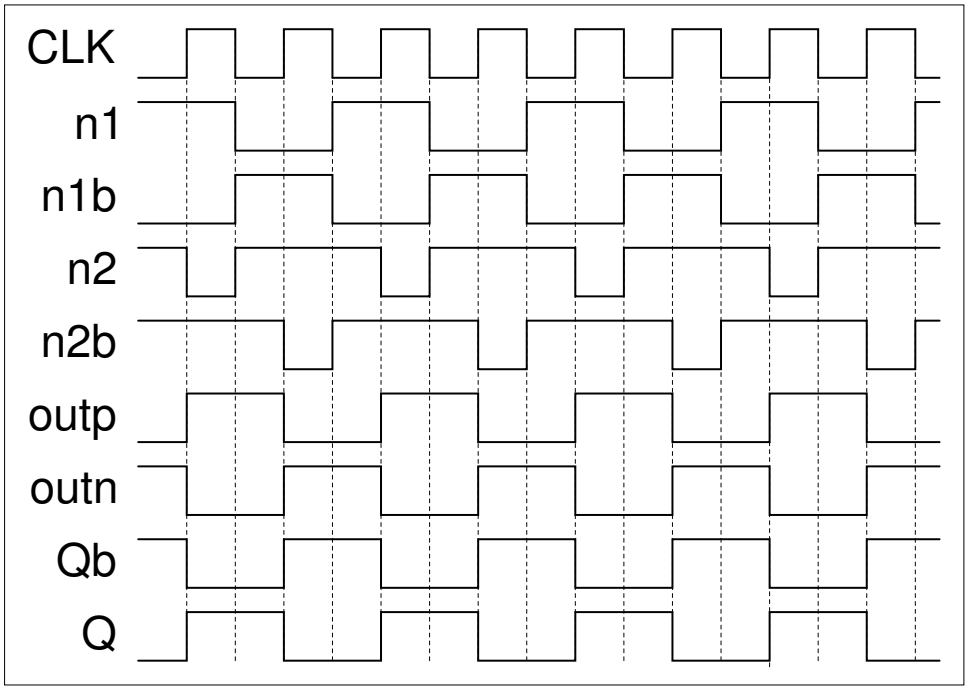


Figure 2.9 – Signal Propagation Through Divider.

propagation delay from input to output for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions should be identical. From the diagram it is noted that in Phase II nodes *n2* and *outp* have transitions as to switch the output *Qb* from $1 \rightarrow 0$. However for the output transition from $0 \rightarrow 1$, shown in Phase IV, only node *outp* switches, thus both these paths should be worked to keep the charge and discharge transitions in the output symmetrical.

From the fact that this is a dynamic logic circuit, the leakage effect will, over time, discharge the internal nodes. This will, in turn, disrupt the working flow of the circuit and thus imposes a minimum operating frequency. The maximum operating frequency of this circuit is defined by the slowest switching node of the circuit. When looking to the top-level schematic, in the closed-loop configuration presented in Figure 1.8, another limiting factor regarding the maximum operation frequency arises. Instead of the slowest node in each individual Flip-Flop, the limiting factor is now the propagation delay from input *CLK* to outputs *Q/Qb* since the setup time for the next Flip-Flop cannot be violated to ensure the correct function of the circuit.

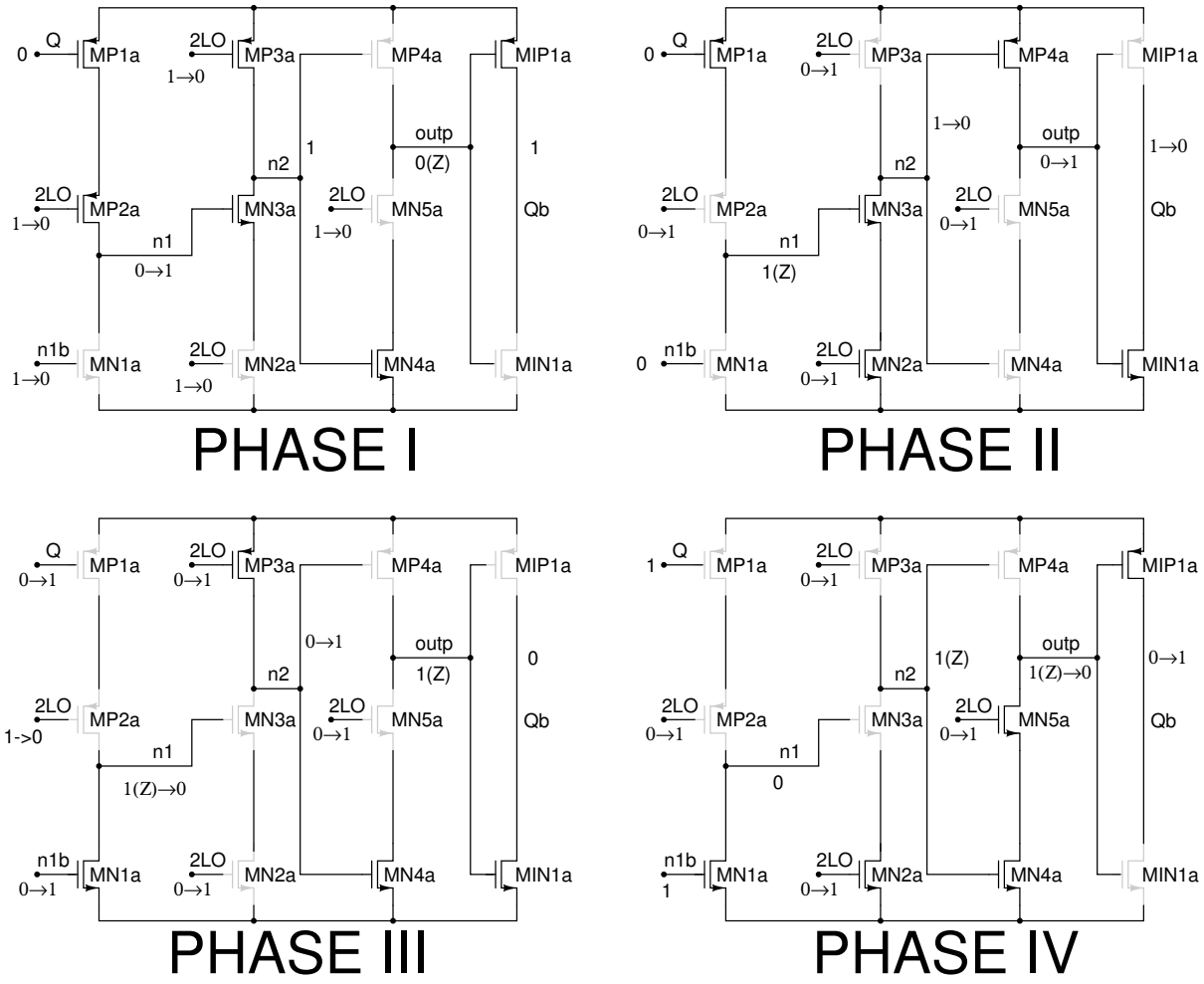


Figure 2.10 – Diagram for a divide-by-two operation.

2.3.2 Phase Noise Analysis

Regarding the phase noise of the divider circuit, a similar analysis as to the one done in [20] can be done. The proposed method reduces the operation of TSPC stages to the same of an simple CMOS inverter which presents the total phase noise, due to both flicker and thermal noise, during a switching operation as in Equation 2.4.

$$S_\Phi(f) = \left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} \left[\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f) \right] \right\}_{NMOS}$$

$$+ \left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} \left[\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f) \right] \right\}_{PMOS} \tag{2.4}$$

$$+ \frac{2\pi^2 f_{in} kT}{r_{edge}^2 C_L}$$

In this equation, $r_{edge} = I_D/C_L$, with I_D being the drain current of the transistor which is charging or discharging the load C_L at the moment when the output voltage crosses the halfway point of $VDD/2$. ΔT represents the switching duration used for the integration period of the noise. $S_I(f)$ and $S_{1/f}(f)$ respectively represents the Fourier transform of the thermal noise current and flicker noise of the transistors.

Looking now at the signal diagram presented in Figure 2.9 and the active transistors responsible for signal propagation in Figure 2.10 in each stage it is possible to determine which transistors are responsible to add jitter, and consequently phase noise in the frequency domain, to the divided signal, as shown in Figure 2.11. It is possible to note that the signal transitions in Phase I and Phase III as shown in Figure 2.10 do not contribute to the overall output jitter since the signals that present switching in these phases of operation have sufficient time to stabilize and don't propagates to the output.

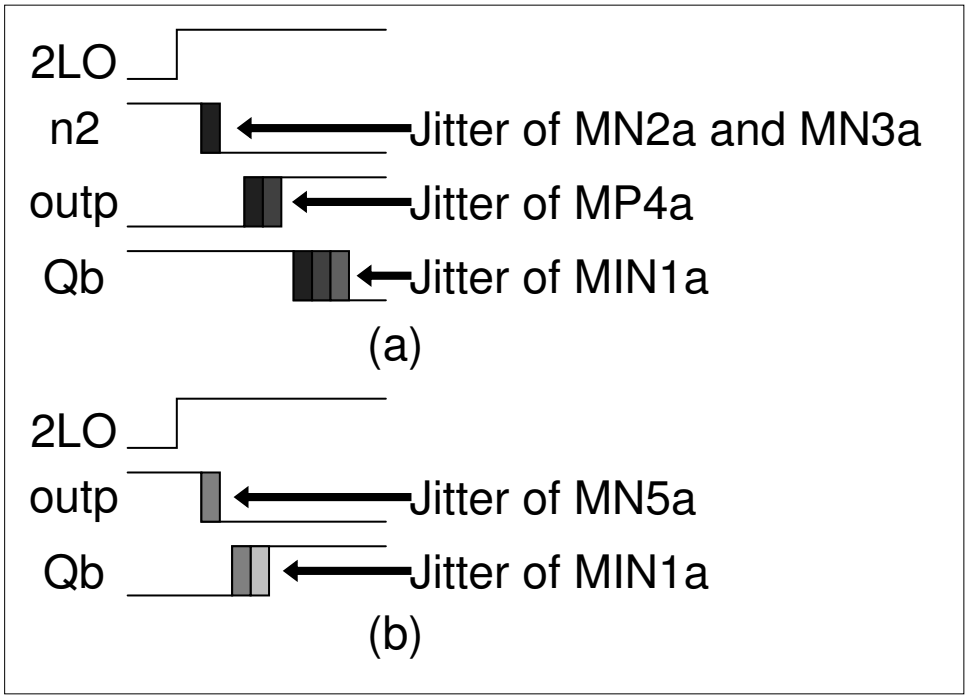


Figure 2.11 – Jitter contributions to output signal (a) Falling edge, (b) Rising edge.

Knowing which transistors are responsible to transfer noise to the output, it is possible to optimize the critical transistors for the required phase noise at the expense of power consumption. Since all the lengths are the same for devices in the design, the parameter to be optimized is the transistor width, as in Equation 2.5 [20]. W_a corresponds to the transistor which is driving a circuit node and W_b corresponds to the transistor which is being driven in this node. The factor η is approximately 2 and corresponds to the drain junction capacitance and the Miller multiplication of the gate-drain overlap capacitance.

$$S_\Phi(f) \propto \frac{(\eta W_a + W_b)^2}{{W_a}^3} \tag{2.5}$$

Taking into consideration both the working principle of this circuit and the noise injection mechanism the interactive process of sizing the transistors to match the simulation results to the desired specification can be started.

The design phase of this project takes place utilizing the EDA tool Cadence® Virtuoso® Platform for schematic, layout and simulation of the circuit and Mentor® Calibre® tool suite for physical layout verification. The utilized technology is TSMC 65 nm CMOS which is a low-power mixed-signal/RF process.

2.3.3 Testbench and Schematic Simulation Results

The utilized testbench setup in the simulation environment is presented in 2.12. The setup consists of the designed frequency divider as the device under test (DUT), voltage-independent sources to create the necessary power supply, and input RF signal and capacitors as loads to the circuit. The tests consist of a transient simulation of at least a hundred output cycles to assess phase error between outputs, duty-cycle, rise and fall times, and dynamic power consumption. A Periodic Steady-State (PSS) simulation in conjunction with a Periodic Noise Analysis (Pnoise) is also used to infer the phase noise of each output.

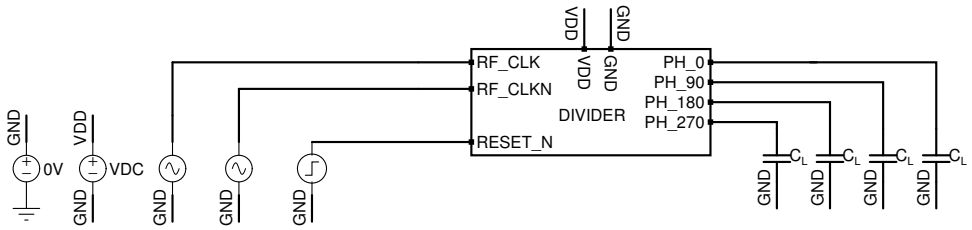


Figure 2.12 – Testbench setup utilized in circuit design.

The first design provided a minimum phase error, as expected from an ideal schematic simulation for a differential design, but the phase noise was above the desired specification. Utilizing the relation from Equation 2.5 the dimension for the critical transistors for the noise paths were adjusted. Looking into the power consumption it was noted that it could be reduced at the cost of the input frequency range by reducing the size of input stage transistors. The final dimensions for the transistors in the design are presented in Table 2.2.

The schematic design phase results in a divider capable of handling input frequencies in the range of 400 MHz to 4 GHz with a power consumption of 530.2 μW and 5.251 mW respectively for a 300 fF load. Figure 2.13 shows the power for all simulated frequencies. As expected the presented curve is a line since in a dynamic circuit the power consumption is proportional to the switching frequency. The circuit's largest phase error

Table 2.2 – Circuit Transistor Sizing.

Device	Channel Length (L) [nm]	Channel Width (W) [nm]	Number of fingers
MP1a,MP1b	60	920	6
MP2a,MP2b	60	920	6
MP3a,MP3b	60	920	8
MP4a,MP4b	60	920	9
MIP1a,MIP1b	60	920	34
MN1a,MN1b	60	400	3
MN2a,MN2b	60	400	15
MN3a,MN3b	60	400	15
MN4a,MN4b	60	400	9
MN5a,MN5b	60	400	9
MIN1a,MIN1b	60	400	34
MRP,MRDP	60	920	20
MRN,MRDN	60	400	20

seen in the simulations is 0.12° for the upper input frequency limit since the circuit is operating close to its failing point and the outputs start to desynchronize.

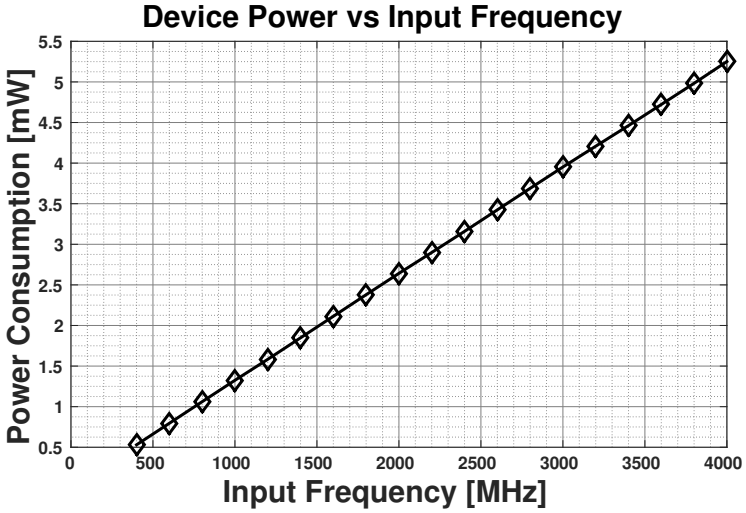


Figure 2.13 – Power versus Input Frequency.

Regarding the circuit phase noise, the obtained results for output frequencies of 900 MHz and 2 GHz are presented in Figure 2.14 for each single-ended output. As expected, they all present the same phase noise since the transistors that contribute to add noise to each output have the same sizing, and for increased frequency, the phase noise is worse due to higher switching activity. When sizing the transistors, current densities supported in the technology as well as capacitive effects are taken into consideration when deciding the use of fingers or multipliers for the transistors.

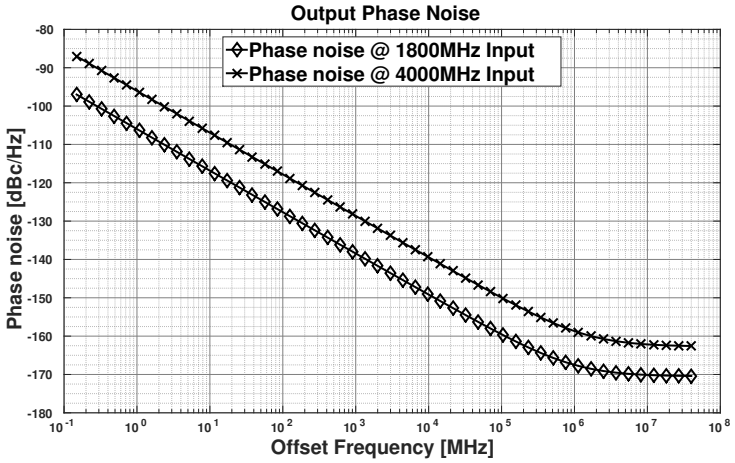


Figure 2.14 – Phase Noise Characteristic.

To finalize schematic phase simulations robustness to process, voltage, and temperature (PVT) variation is carried out. Temperature affects the circuit behavior by reducing the transistor saturation current as temperature raises and consequently decreasing maximum operation frequency and rise and fall times. Regarding power supply, a similar effect is noted as expected since the increase or decrease in voltage directly influences transistors gate-source voltage (V_{GS}) and thus drain current. These effects are summarized in Figure 2.15.

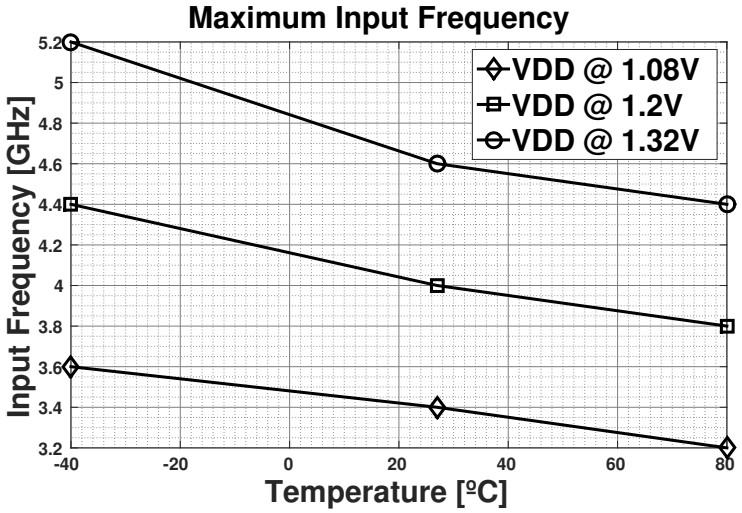


Figure 2.15 – Maximum input frequency given variation in temperature and power supply.

To assess the process variation, Monte Carlo simulations utilizing 1000 sample points are made. In Figures 2.17, and 2.16 are presented the worst-case variation across all four outputs for duty cycle and quadrature-phase error. It is observed that the duty-cycle falls outside the specification for the input frequency 4 GHz, but since this frequency is considerably above the required specification, it is not considered to be a problem. Regarding the phase error, it is seen that it never crosses, even when considering the

deviation, a phase error above 0.15°. The data point for an input frequency of 4 GHz is not present in 2.16, since it presents an error in the order of 1° and makes it difficult to visualize the rest of the data and also falls close to the specification limit.

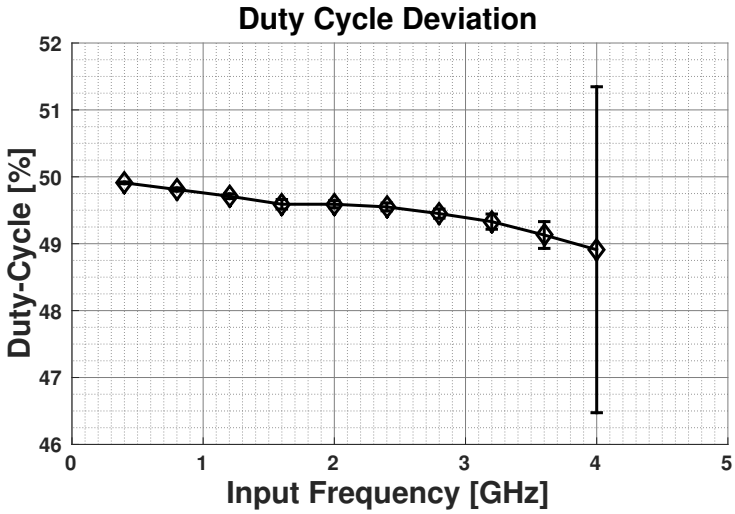


Figure 2.16 – Duty-Cycle Variation due to Process for Monte Carlo Simulation.

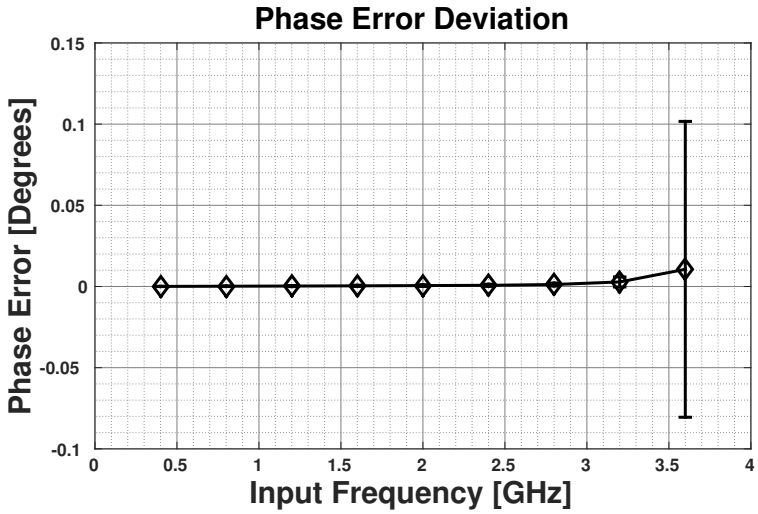


Figure 2.17 – Phase Error Variation due to Process for Monte Carlo Simulation.

Considering all the obtained results, it is deemed possible to proceed to the circuit layout phase since the results present a good margin from the desired specification.

2.3.4 Layout and Extracted Simulation Results

The layout process starts with an initial device placement of two flip-flop cells to form the divider, as presented in Figure 1.8. The placement follows traditional design recommendations such as device placement symmetry and proximity [21]. The placement presented in 2.18 is utilized to minimize issues regarding unbalanced signal routing that

may insert different delays in signal paths that should be symmetrical and also minimize process gradient variations.

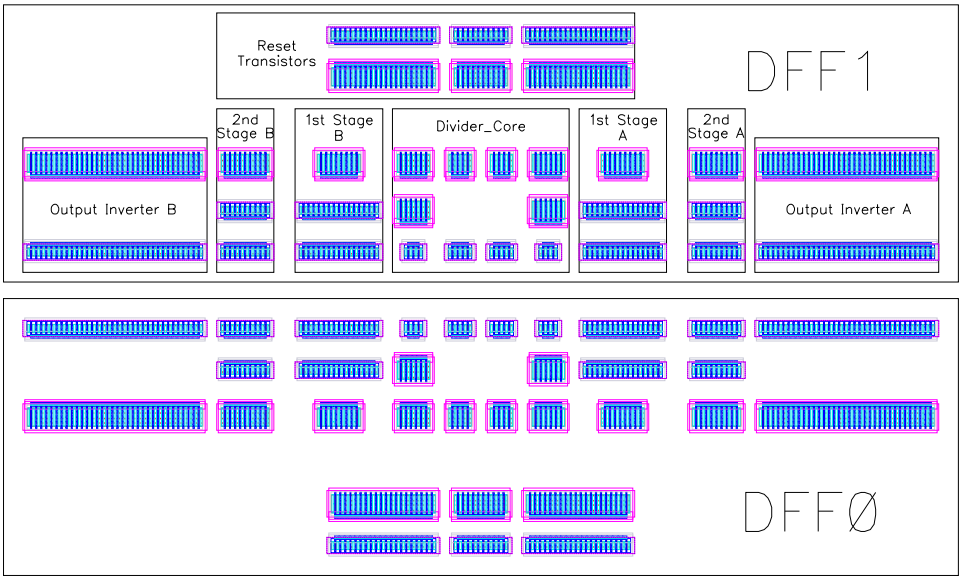


Figure 2.18 – Circuit Device Placement.

The next step after device placement is signal routing. This phase tends to be an interactive process since parasitic elements should be taken into consideration to achieve a well-matched layout in the end. These parasitic elements appear from the physical characteristics of the materials utilized in the interconnection between devices. Parasitic capacitance can appear from two different phenomena: the interaction between a signal path and the silicon substrate (ground) and from the interaction between two signal paths. In both cases, it is observed that the structures formed are capacitors as shown in Figure 2.19.

Parasitic resistance arises from the intrinsic resistance the material used for interconnection, usually a metallic material, presents. This characteristic is more predictable than the parasitic capacitance since the documentation for the technology process usually provides information about the interconnection resistance so the circuit designer can make preliminary estimates of parasitic resistance. Both resistors and capacitors will influence the RC delay experienced by the signal and thus influence the phase error that the layout inserts into each output.

The next phase is the verification of the layout. The first step is to check physical constraints such as geometries spacing and overlapping which are verified by Calibre ® Device Rule Checking (DRC) tool. After DRC, the layout topology check is done utilizing Calibre ® Layout versus Schematic (LVS) to be sure the circuit created in the layout corresponds to the circuit created in the schematic. Finally, a circuit extraction contemplating the layout parasitics is obtained through Calibre ® Parasitic Extraction (PEX) tool.

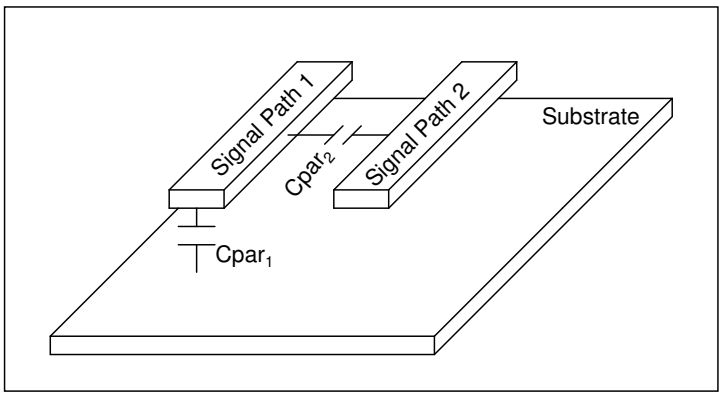


Figure 2.19 – Parasitic Capacitor Structures.

The circuit contemplating the parasitic devices is now utilized in the testbench presented in Figure 2.12 to re-run the simulations and check the circuit performance. If the simulation results are not according the desired specification, analysis of the results is necessary to identify the possible layout effects that create the discrepancy between schematic and extracted simulation. Modifications on the layout are made and then the verification process starts anew. In this project three layout iterations were necessary before achieving the desired results, the final layout for a single divider is presented in Figure 2.20 and the summary of the simulated extracted results in Table 2.3 for a 1.8 GHz input frequency. It is noted that the rise and fall time specifications are not properly met, but due to new loading specifications as better described in the next section, it is opted to keep the circuit design as it is.

Table 2.3 – Extracted Simulation Results @ 1.8 GHz Input.

Specification	Result
Duty-cycle - Q0	50.06 %
Duty-cycle - Q90	50.05 %
Duty-cycle - Q180	50.04 %
Duty-cycle - Q270	50.05 %
Rise Time - Q	55.6 *ps*
Rise Time - Q90	55.9 *ps*
Rise Time - Q180	55.8 *ps*
Rise Time - Q270	55.9 *ps*
Phase Error (Q - Q90)	0.098°
Phase Error (Q90 - Q180)	0.052°
Phase Error (Q180 - Q270)	0.053°
Phase Error (Q270 - Q0)	0.099°
Phase Noise (40 MHz offset)	−167.81 dBc/Hz
Power	2.93 mW
Size (W x L)	30.92μm x 46.94μm

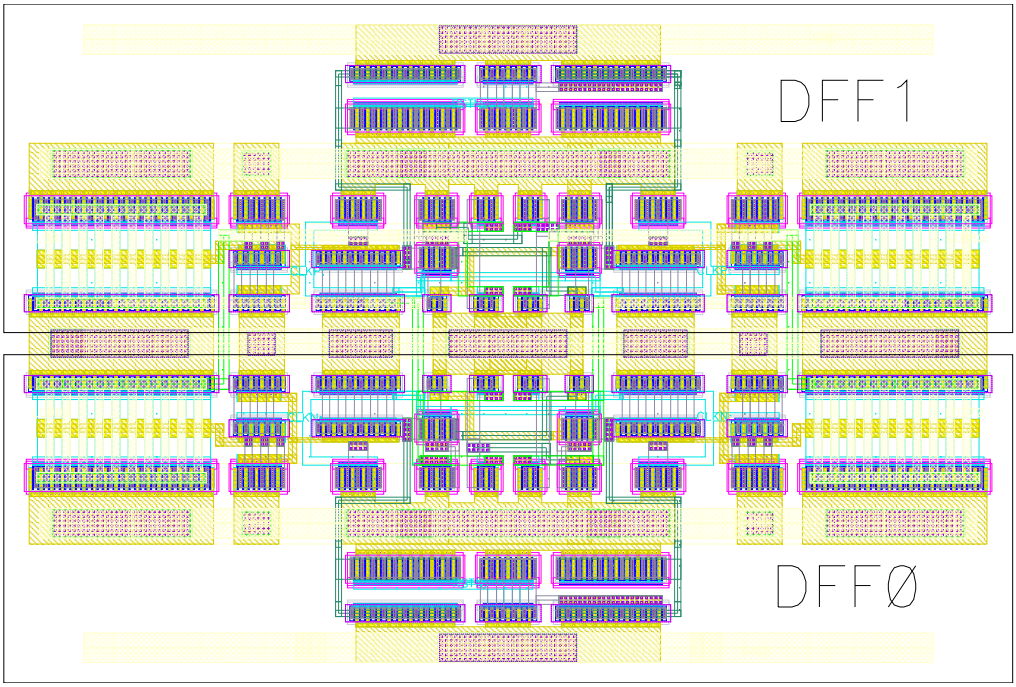


Figure 2.20 – Final layout version for the quadrature frequency divider.

2.4 Design Integration to Top-Level System

2.4.1 Schematic Top Level Integration

As previously stated in Section 2.1, the frequency divider block in this project is responsible to provide signal for the transmission path, the receiver path, and the baseband modem. To accomplish this task it was noted the need of employing a second frequency divider to further reduce the frequency before entering the baseband modem as well as buffers to ensure the proper driving capability to all three different circuits and thus some additional work is needed. The circuit schematic for the complete circuit is presented in Figure 2.21.

The second frequency divider utilized is the same as the one presented previously. To connect the output of the first divider to the second one its utilized buffers on all four output phases even though only two phases are needed. This is done to ensure symmetrical loading in all four outputs. The buffer for the transmitter path is adjusted to drive a 300 fF load and the buffers in the receiver path should drive a 200 fF load. Schematic simulation results for the complete circuit is provided in Table 2.4.

The results provided in this table are for the typical application frequency (1.8 GHz input frequency) and maximum supported input frequency (3.4 GHz). Note that the maximum input frequency is slightly reduced from 4 GHz to 3.4 GHz, this happens due to the buffer design which is decided to have a limited current and thus limiting the maximum frequency in which it can operate. The total power consumption has greatly increased mainly due

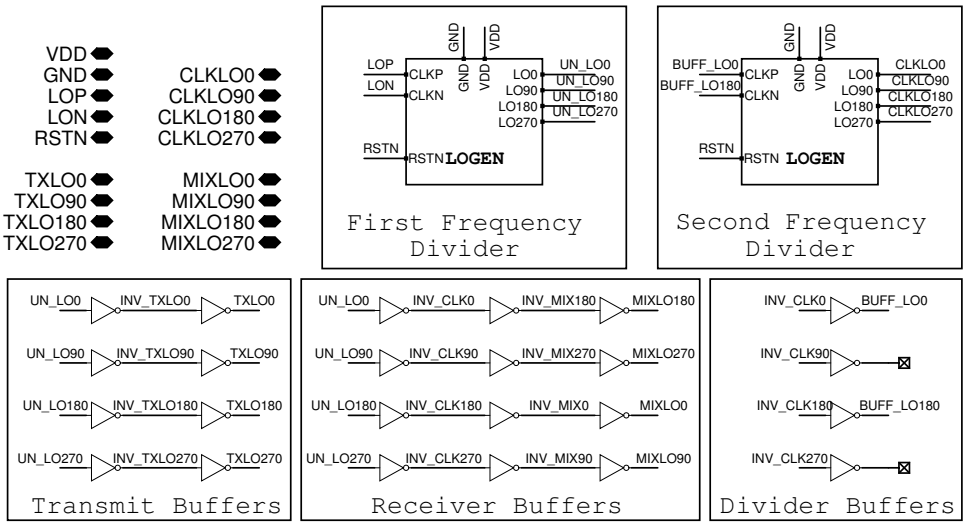


Figure 2.21 – Top level schematic for the complete frequency divider block.

to the buffers which need to drive a total of 2 pF load when combining all outputs. The testbench for the top-level integration is presented in Figure 2.22. The only difference from this testbench to the individual divider presented before in Figure 2.12 is the addition of outputs for each signal with the corresponding capacitive loads of 300 fF for transmitter path (**TXLO**) and 200 fF for both receiver and baseband path (**MIXLO** and **CLKLO**).

Table 2.4 – Top Level Divider Schematic results.

Specification	Results @ 1.8 GHz Input	Results @ 3.4 GHz Input
Duty-cycle-Q0	50.04 %	50.15 %
Duty-cycle-Q90	50.04 %	50.12 %
Duty-cycle-Q180	50.03 %	50.38 %
Duty-cycle-Q270	50.04 %	50.41 %
Rise Time - Q	29.85 ps	29.83 ps
Rise Time - Q90	29.75 ps	29.81 ps
Rise Time - Q180	29.78 ps	29.83 ps
Rise Time - Q270	29.83 ps	29.72 ps
Phase Error (Q - Q90)	0.099°	0.439°
Phase Error (Q90 - Q180)	0.021°	0.458°
Phase Error (Q180 - Q270)	0.077°	0.339°
Phase Error (Q270 - Q0)	0.024°	0.358°
Phase Noise (40 MHz offset)	−170.02 dBc/Hz	−164.22 dBc/Hz
1^{st} Divider Power	1.346 mW	2.506 mW
2^{nd} Divider Power	1.079 mW	2.047 mW
TX Buffer Power	2.313 mW	4.369 mW
RX Buffer Power	1.56 mW	2.951 mW
Interconnect Buffer Power	109.1 μW	206.3 μW
Total Power	6.407 mW	12.08 mW

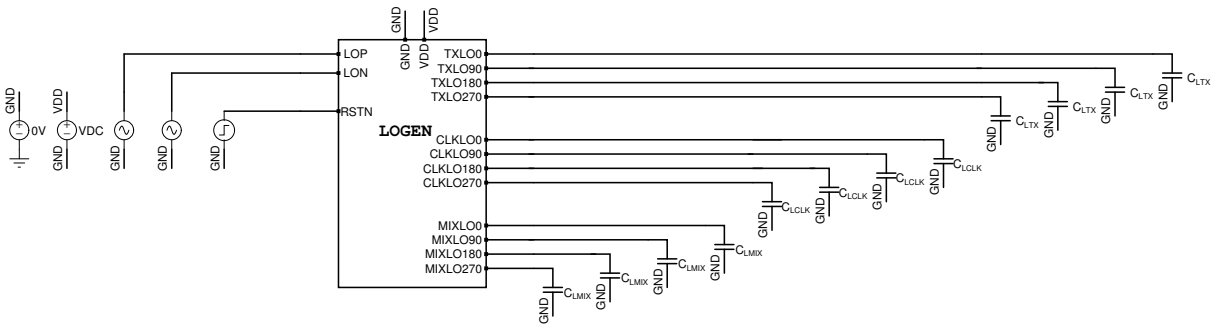


Figure 2.22 – Top level Testbench for the complete frequency divider block.

2.4.2 Layout Top Level Integration

The top-level layout is presented in Figure 2.23. In it it is possible to identify two copies of the individual divider cells, shown in Figure 2.20, and the buffer structures. The connection on the left-hand side of the layout, which provides the signal to the receiver path, is purposefully longer to account for the introduced parasitics which would arise in the chip level interconnection. As in the circuit level layout, the concerns with symmetry and signal path lengths exist in the block level layout to keep signal degradation due to layout parasitics to a minimum.

The final step would be to simulate the extracted layout with parasitics to ensure that the top-level layout still is in conformance with the specification and if there is any problem iterate over the layout and schematic until every design requirement is met. At the time of the design, some tool licensing restrictions made circuit extraction unable to run, thus, imposing a heavy penalty in the design cycle. As to try to contour this impediment, it is used the parasitic model previously extracted for the individual divider. Then, based on path length and width of the most critical interconnections not contemplated in the previous extraction, such as the buffers and the connection between the two dividers, capacitors were manually inserted in those nets to try to simulate the parasitic capacitors.

Though this is definitely not the ideal procedure it was the only option at the moment. The same transient, PSS, and PNoise simulations are utilized to assess the circuit performance. Table 2.5 presents the results for both nominal and maximum frequencies, using this estimate capacitance method. It is noted a reduction in maximum input frequency from 3.4 GHz to 3 GHz and an expected increase in the rise time but still in conformance with the specifications.

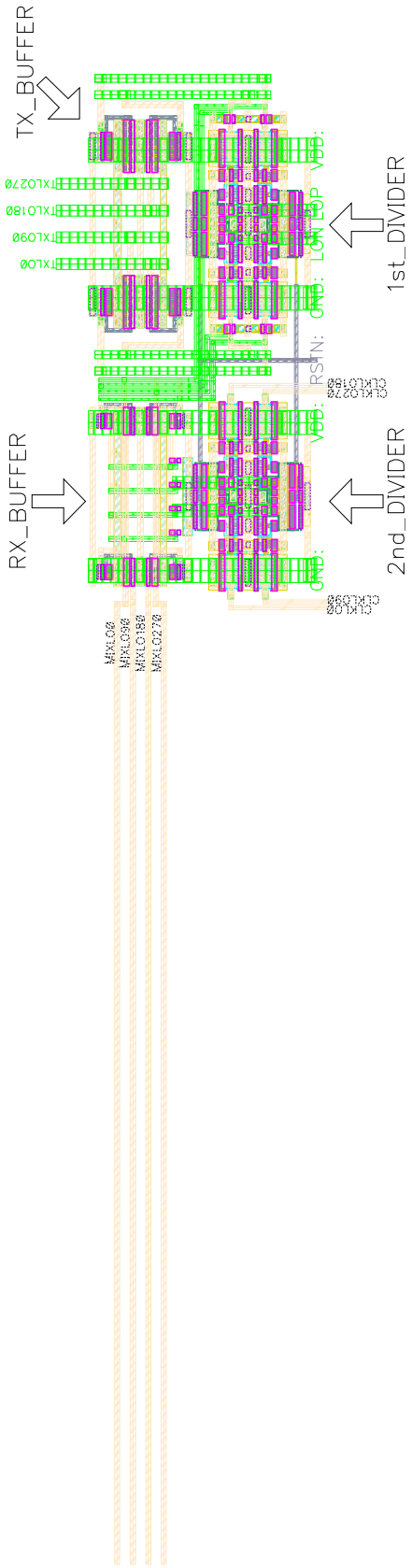


Figure 2.23 – Top level layout for the complete frequency divider block.

Table 2.5 – Top Level Divider Layout Estimated Capacitors Results.

Specification	Results @ 1.8 GHz Input	Results @ 3.0 GHz Input
Duty-cycle-Q0	50.02 %	49.79 %
Duty-cycle-Q90	49.91 %	49.76 %
Duty-cycle-Q180	50.12 %	50.03 %
Duty-cycle-Q270	50.21 %	50.07 %
Rise Time - Q	38.16 ps	38.27 ps
Rise Time - Q90	38.32 ps	38.3 ps
Rise Time - Q180	38.17 ps	38.13 ps
Rise Time - Q270	38.87 ps	38.35 ps
Phase Error (Q - Q90)	0.138°	0.373°
Phase Error (Q90 - Q180)	0.118°	0.479°
Phase Error (Q180 - Q270)	0.137°	0.310°
Phase Error (Q270 - Q0)	0.110°	0.434°
Phase Noise (40 MHz offset)	−168.84 dBc/Hz	−163.21 dBc/Hz
Total Power	7.27 mW	12.1 mW

After the complete chip was submitted to fabrication it was possible to do the parasitic extraction using Calibre ® PEX tool. The simulations were then done and the results presented in Table 2.6. The first immediate concern was the drastic reduction in the maximum operating frequency from 3.0 GHz to 1.9 GHz this immediately shows that the capacitance was highly underestimated.

Table 2.6 – Top Level Divider Layout Extracted results.

Specification	Results @ 1.8 GHz Input	Results @ 1.9 GHz Input
Duty-cycle-Q0	50.15 %	50.35 %
Duty-cycle-Q90	50.11 %	50.19 %
Duty-cycle-Q180	50.13 %	50.33 %
Duty-cycle-Q270	50.29 %	50.49 %
Rise Time - Q	37.32 ps	37.4 ps
Rise Time - Q90	37.35 ps	37.35 ps
Rise Time - Q180	37.12 ps	37.17 ps
Rise Time - Q270	36.89 ps	36.91 ps
Phase Error (Q - Q90)	0.389°	0.544°
Phase Error (Q90 - Q180)	0.224°	0.217°
Phase Error (Q180 - Q270)	0.160°	0.074°
Phase Error (Q270 - Q0)	0.005°	0.252°
Phase Noise (40 MHz offset)	−170.02 dBc/Hz	−164.22 dBc/Hz
Total Power	8.78 mW	9.263 mW

Taking a closer look at the parasitics report provided by the extraction tool and comparing the capacitance in the critical nets to the values of the estimated capacitors it was possible to observe that the main underestimation was in the coupling capacitors

between paths. An example is shown in Figure 2.24a where the output nets of the first divider are highlighted, in these nets the estimated capacitance was 25 fF. It is possible to see that in column "C Total" that the intrinsic capacitance is around 10 fF but in column "CC Total" the coupled capacitance alone is around 50 fF, which is double the estimated capacitance. Looking closer to which net was responsible for the coupling capacitance on 2.24b, it is seen that the power supply nets VDD and GND, which were included in the top-level design, were the ones mainly responsible for the increased capacitance.

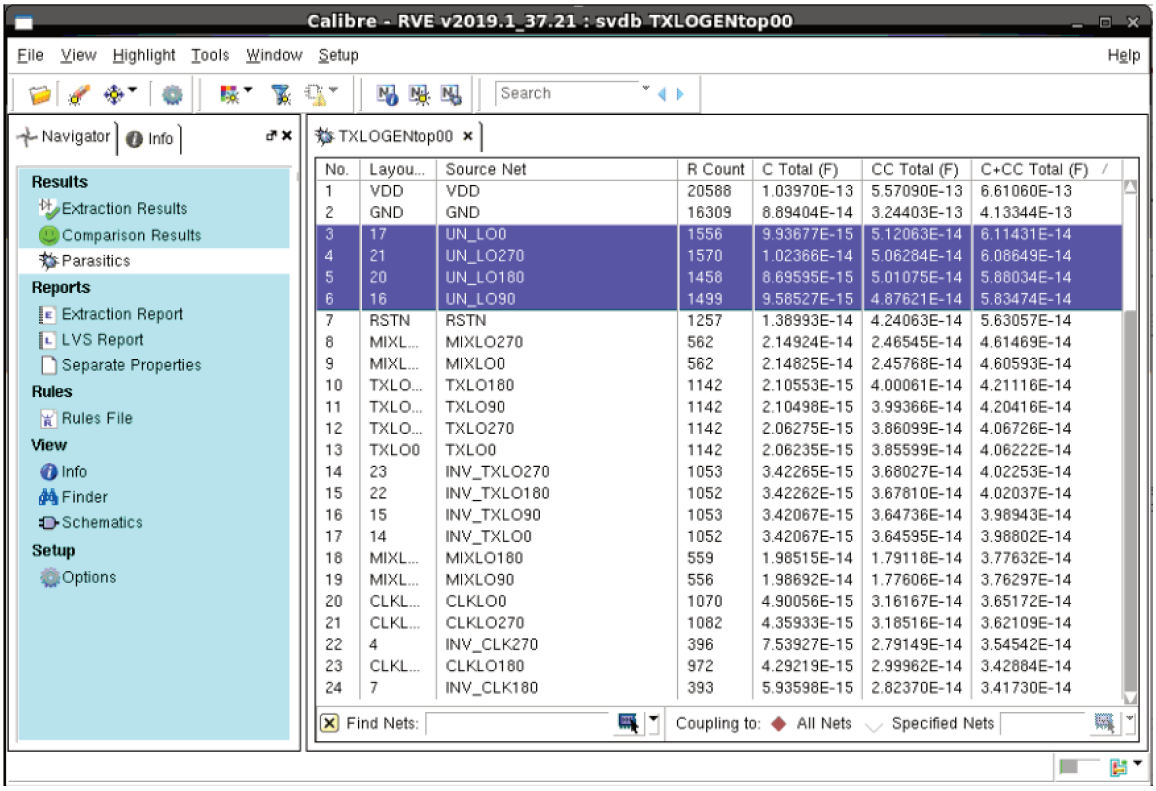
At this point, since the fabrication process was already undergoing, nothing could be done to change the circuit design. Since the design was borderline functional, simulations taking process corners into consideration were done to ensure that the mandatory input frequency of 1.8 GHz is possible to be achieved. When considering a 1.2V power supply and the circuit at 27 $^{\circ}C$, it was noted that in corners FS and SS the divider fails to operate, presenting an output of 300 MHz instead of 900 MHz. As a measure to overcome this problem, the power supply voltage is increased in the simulation since this will allow higher current values to flow through the transistors and thus to compensate for the added capacitance. The values were increased in steps of 0.05 V till the divider was able to properly work in all four process corners at an input frequency of 1.8 GHz. The results for these simulations are presented in Table 2.7 and shows that a power supply voltage of 1.4 V is needed to ensure proper circuit operation across all process corners. Due to increased voltage, the circuit consumption is also increased while rise and fall times and phase noise is reduced. The summarized results utilizing 1.4 V is presented in Table 2.8.

Table 2.7 – Extracted layout operation for process corners and power supply.

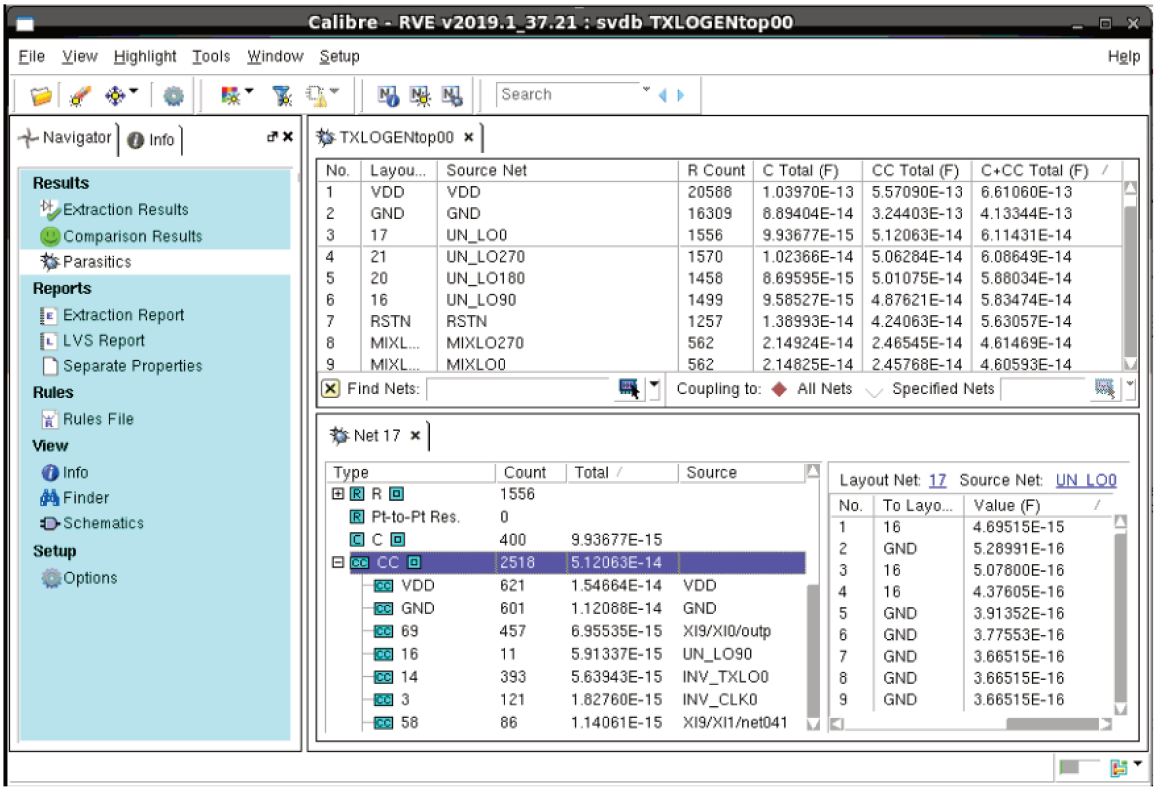
Power Supply	Process Corner				
	TT	FF	FS	SF	SS
1.2	Pass	Pass	Fail	Pass	Fail
1.25	Pass	Pass	Fail	Pass	Fail
1.30	Pass	Pass	Pass	Pass	Fail
1.35	Pass	Pass	Pass	Pass	Fail
1.4	Pass	Pass	Pass	Pass	Pass

2.5 Circuit Design Final Considerations

In this chapter, the complete design process of the frequency divider was presented from the initial block specifications to the final layout that is integrated in the chip design. Although software licensing problems lead to a final design that wasn't capable to provide correct operation the working principle of the divider topology is proven through simulation. The circuit was fabricated in TSMC 65 nm CMOS mixed-signal/RF process



(a) Output nets parasitic capacitance summary.



(b) Coupled parasitic capacitance detail.

Figure 2.24 – Parasitic report for top level layout.

and 100 samples were available for use being 50 samples just the fabricated die, 40 samples encapsulated in a Quad-Flat No-Lead with 100 pins (QFN100) package and 10 samples in

Table 2.8 – Top Level Divider Layout Extracted results Using 1.4 V power supply.

Specification	Results @ 1.8 GHz Input
Duty-cycle-Q0	49.62 %
Duty-cycle-Q90	49.61 %
Duty-cycle-Q180	49.67 %
Duty-cycle-Q270	49.67 %
Rise Time - Q	24.7 ps
Rise Time - Q90	24.62 ps
Rise Time - Q180	24.68 ps
Rise Time - Q270	24.37 ps
Phase Error (Q - Q90)	0.207°
Phase Error (Q90 - Q180)	0.022°
Phase Error (Q180 - Q270)	0.151°
Phase Error (Q270 - Q0)	0.033°
Phase Noise (40 MHz offset)	−169.74 dBc/Hz
Total Power	10.78 mW

a QFN100 package without the top-lid. In the next chapter the measurement process, from the requirements for the measurement setup to the circuit results are presented, discussed, and compared to the results obtained during the design phase.

3 Measurements Methodology and Results

In this chapter, the overall system configuration surrounding the frequency divider, which is necessary to realize the measurements, is explained. Following this, the methodology and measurement setup for the fabricated circuit is shown. Finally, measurement results are presented and discussed.

3.1 Fabricated System Overview

A micrograph of the chip is shown in Figure 3.1. The transmitter circuit is visible in the top-left corner and occupies an area of $1149\mu m \times 950\mu m$. The highlighted area is the region where the frequency divider is.

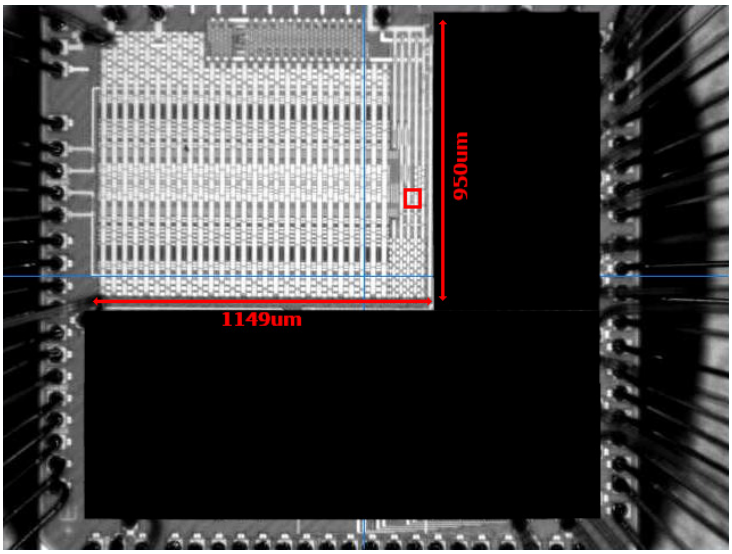


Figure 3.1 – Encapsulated chip micrography showing the transmitter block.

As shown in Figure 2.1, the chip has an integrated PLL and oscillator that feeds a signal to the frequency divider. Although this signal could be used as a source to the circuit, another signal path, shown in Figure 3.2, is implemented to feed the chip with an external signal. The configuration control for both the signal selector and bias voltage generator blocks comes from the register bank (RB) that is present in the digital modem block and is read/written by I2C protocol communication.

To effectively measure the divided signal from the circuit, three approaches are possible: (a) measure the signal at the transmitter output when the transmitter has no power supply provided; (b) measure at the transmitter output, but with the transmitter powered on and a fixed signal as the transmitter input; (c) measure the further sub-divided signal that goes to the digital modem. The third measurement method (c) requires an extra

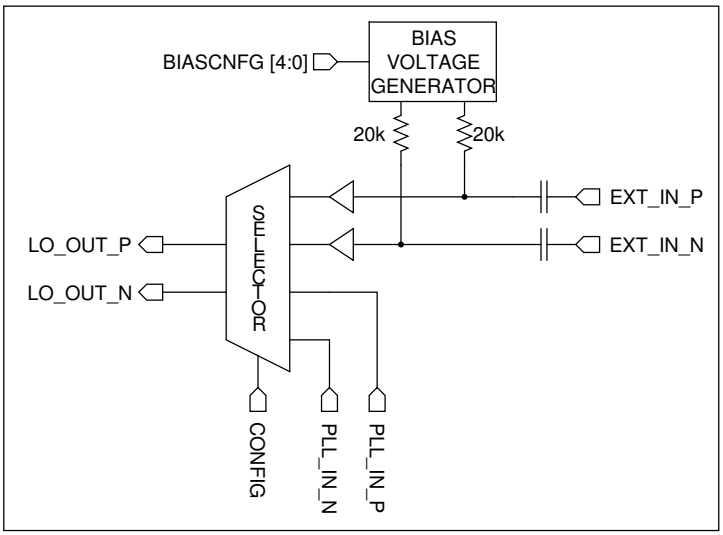


Figure 3.2 – Circuit diagram for external signal input.

I2C configuration to make the signal available as a modem output. Measurements using the sub-divided digital output allow just frequency measurements since the signal goes through several other divisions and components. Thus, the phase noise for the original divider output can not be inferred. In the case of measurement of the signal at the transmitter output, when no power supply is applied to the transmitter, only a fraction of the divider output will be measured due to capacitive coupling. When measuring with the transmitter powered on, the measured frequency is equal to the divider's output, and phase noise is expected to be slightly higher since there is also the contribution of the transmitter circuitry to the LO signal phase noise, but it is a good indicator of the divider performance.

Regarding power consumption of the frequency divider, a direct measurement cannot be readily obtained since the power supply is shared with other circuitry inside the transmitter. In Figure 3.3, a simplified diagram of the transmitter is presented. All the blocks outlined in red shares the same power supply as the frequency divider while only the transmitter itself uses a separated analog power supply. It is possible by means of control via register bank to reduce the current usage of the external data input processing block as also set the blocks that are not being used to a reset state and thus minimizing dynamic current consumption due to other blocks.

As a first step to do the measurements, a simple printed circuit board (PCB) is manufactured, shown in Figure 3.4, containing just the essential connections to control the register bank and some measurement points to assert biasing and simple functionalities.

It was noted that although seemingly properly biased, no response was obtained from the digital circuitry through the I2C interface, and thus testing of the analog circuits could not proceed. Testing other available samples resulted in the same observed behavior thus leading to the belief that the issue was somewhere in the connection between the

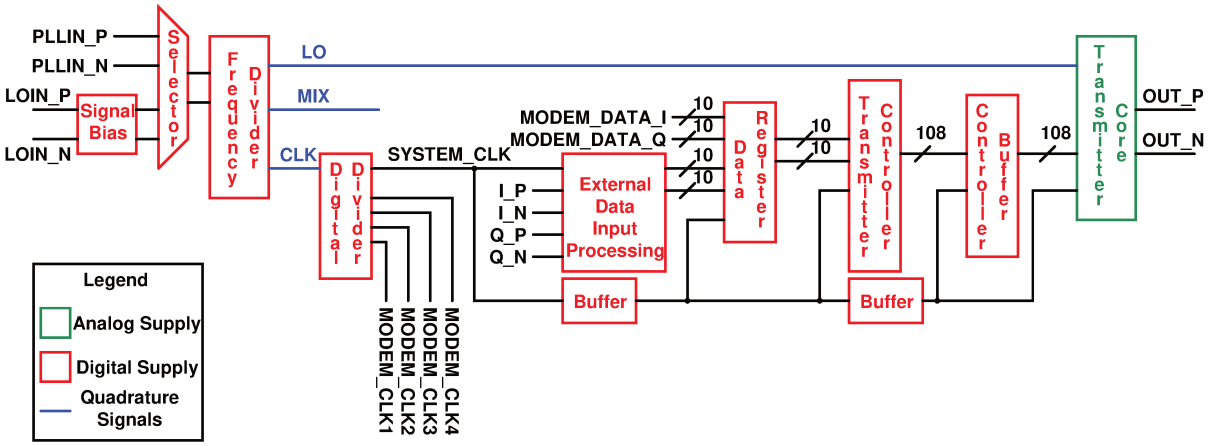


Figure 3.3 – Simplified transmitter block diagram.

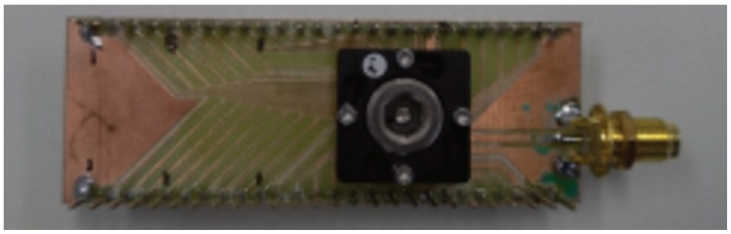


Figure 3.4 – First PCB for communication and biasing tests.

digital circuitry core and the I/O (input/Output) interface that in turn connects to the QFN package. Since the digital I/O cells could be configured to either behave as input only or output only, through a configuration bit from the register bank, the first suspicion was that one of the pins presented an incorrect configuration. Investigating the default register bank configuration showed that there were indeed two pins that were incorrect configured and thus rendering impossible to access the register bank, TOP_CLK, and I2C_SCL, which are respectively the digital system reference input clock and the I2C protocol clock signal. To circumvent the problem the viability of a procedure using a Focused Ion Beam (FIB) to cut the incorrect connections is analyzed.

3.2 Focused Ion Beam Intervention

A FIB is an equipment that is commonly used in the microelectronics industry when the need to manipulate fabricated chips arises. This equipment is capable of removing material from the sample with tenths of nanometres of precision, and also can be used for imaging, similar as in a Scanning Electron Microscope (SEM), and material deposition. The process of interest needed to rework the fabricated chip is both materials removing and deposition to cut and reconnect the misconfigured I/O, more detail on how the FIB process takes place can be readily found in literature such as [22].

The technology used to fabricate the chip consists of nine metal layers for routing plus a top aluminum layer for power supply redistribution. The connections that need to be reworked are in the lower metal layers thus creating a challenge in the process of cutting and reconnecting since, as required by the foundry, dummy metal structures should be present in the chip to fill empty spaces and thus meeting a minimum metal density requirement to guarantee fabrication reliability.

In Figure 3.5, it is shown only layer of the metal trace of interest for the sake of clarity, the metal trace that needs to be cut, denominated as "B", and the surrounding signal connections. The traces that represent power supply connections are also indicated since after cutting the trace "B" it needs to be connected to VDD so that the I/O circuitry operates as desired. In Figure 3.6a, all routing metal layers are presented, and in Figure 3.6b, the dummy filling is included. It is clear the complexity of the operation since there is a high concentration of signal lines in the region and the cut is to be done on top of active digital circuitry, and thus, any misalignment or failure to stop the cutting process at the correct depth may render the circuit inoperable.

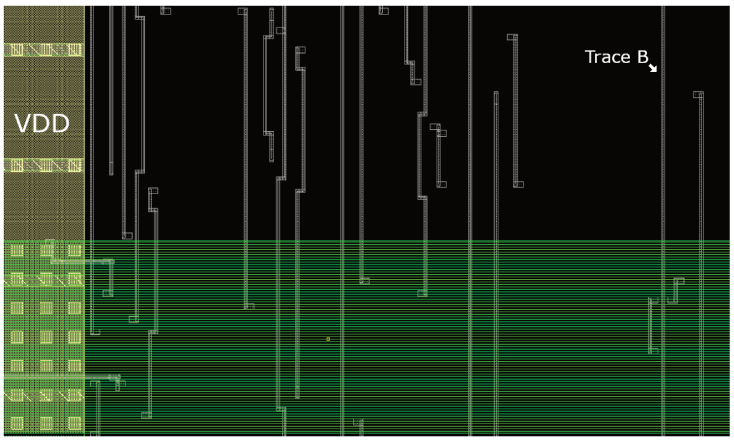
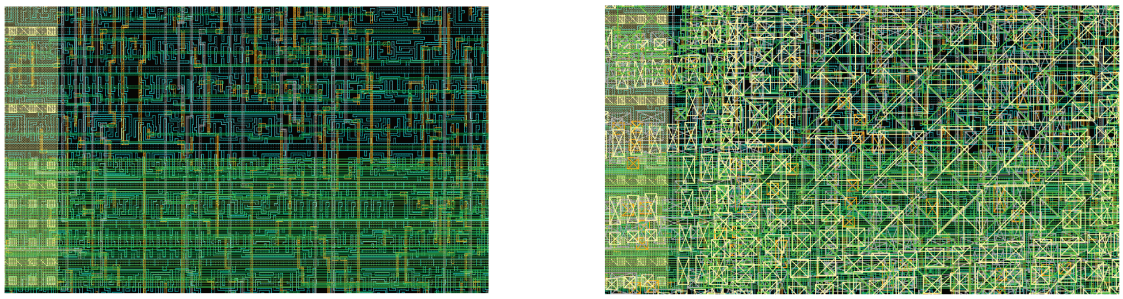


Figure 3.5 – Intervention area showing only the metal layer to be cut.

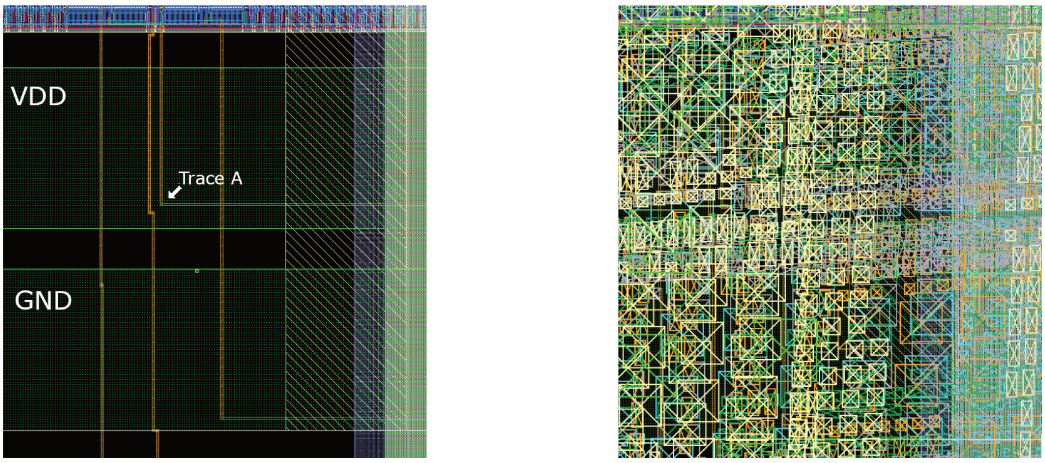


(a) Intervention area showing only the routed signals. (b) Intervention area showing all metal layers.

Figure 3.6 – I2C signal intervention area

Similarly, Figure 3.7a presents the metal trace that needs to be cut, named as "A", and 3.7b shows all metals in the region. As for trace "B", trace "A" also needs to be

connected to a VDD trace after being cut. The operation in this signal is more lenient since there is no active circuit under the trace to be cut. The layer color map identification is presented in Figure 3.8.



(a) Intervention area showing only the routing metal layers.

(b) Intervention area showing all metal layers.

Figure 3.7 – CLK signal intervention area

Figure 3.8 – Layer map identification for both routing and dummy metals.

The FIB process was initially carried out at Centro de Componentes Semicondutores e Nanotecnologias (CCSNano) at UNICAMP but due to the high density of metals, some problems were encountered. Since copper (Cu) has a slightly higher removal rate than silicon oxide (SiO_2), the several dummy patterns that are present above the desired line to be reworked lead to uneven material removal. Figure 3.9 shows the result of a tentative processing of the I2C signal region. Once the removal of metal was faster than the SiO_2, some caving is observed in the lower layers and thus the cutting process was not reliable.

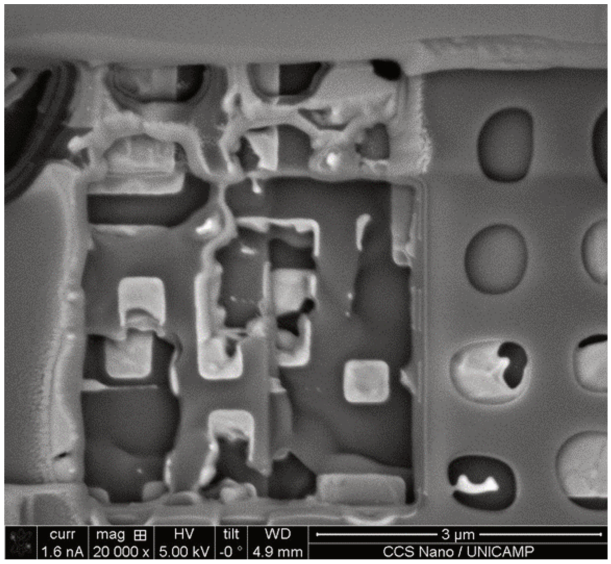


Figure 3.9 – Results from FIB processing realized at CCSNano

A possible way to circumvent this problem is to have a higher removal rate for SiO_2 than for Cu, and this can be achieved in a FIB equipment through the use of an assisting source of Xenon difluoride (XeF_2) that increases the removal rate of SiO_2 while keeping the removal of metal the same [23]. This process was not possible to be realized at CCS since there was no XeF_2 source available for the equipment. A new die processing was realized at CEITEC, which have a FIB equipped with a XeF_2, and the results for the same I2C signal is presented in Figure 3.10. Figure 3.11 shows the result after processing for the TOP_CLK signal and it is clear from this two images that the higher selectivity between Silicon and metal is achieved and thus making it possible to precisely cut the desired connection and later, by process of metal deposition, connect to the correct power supply line.

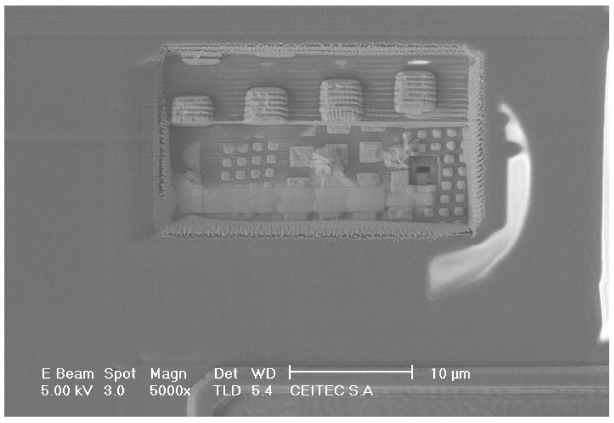


Figure 3.10 – Results from FIB processing realized at CEITEC for I2C

This process was carried out in just four bare die samples to ensure the reliability of the correction, and for testing, a simple bondwire scheme connecting just the minimum

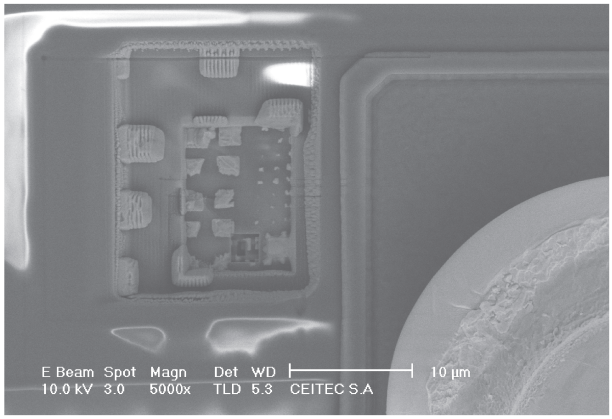


Figure 3.11 – Results from FIB processing realized at CEITECfor CLK

necessary signals besides the corrected ones was done. Figure 3.12 shows the substrate where the die was attached and bonded to metal traces that allow an external connection. Subsequent testing by simply writing a value to a register bank position and reading it back successfully in all samples proved that the correction procedure is reliable and could be done in other samples.

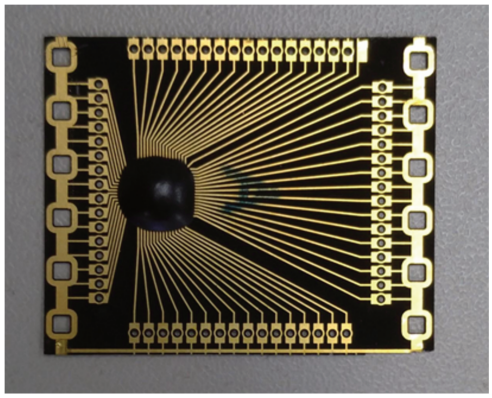


Figure 3.12 – Board to validate FIB processing.

3.3 Measurement Setup and Equipment

Having now complete functional samples, the measurement process can be resumed. In Figure 3.13 it is shown a simplified block diagram of the required key components to power up and allow connection to equipment. This diagram contemplates only the connections needed for the transmitter. The complete diagram and bill of materials (BOM) is presented on Appendix B. Table 3.1 lists the utilized components referenced in Figure 3.13.

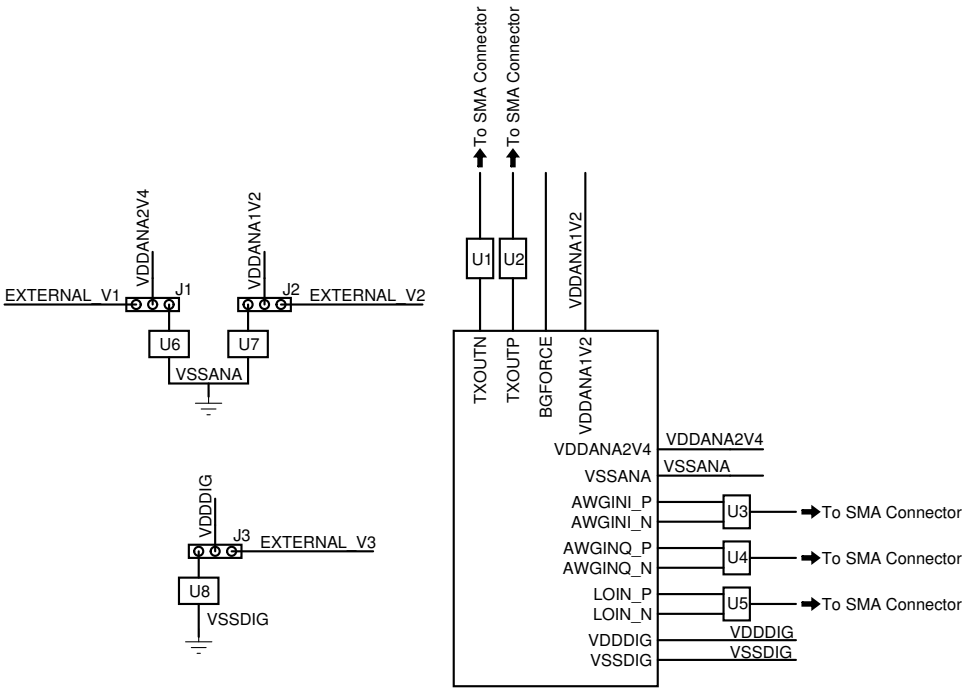


Figure 3.13 – Simplified Block Diagram for the transmitter part of the test board.

Table 3.1 – Simplified bill of materials for test board.

Component	Part-number	Description	Quantity
U1,U2	SMST1804NA005	Impedance matching from 4Ω to 50Ω	2
U3,U4,U5	1720BL15B0200E	50Ω : 200Ω Balun	3
U6	RP132S241B-E2-FE	2.4V voltage regulator	1
U7	MIC5309YD6	Adjustable voltage regulator	1
U8	LP5912-1.2DRVR	Low noise 1.2V voltage regulator	1
J1,J2,J3	CON-SMA-EDGE-S	Straight single row connector	3

The complete PCB layout is designed using Cadence® Allegro® PCB Designer and is shown in Figure 3.14. The measurement setup required to fully characterize the frequency divider is presented in Figure 3.15.

The signal generator is responsible to provide the reference signal to be divided, the utilized equipment is a Keysight EXG N5172B Vector Signal Generator. This equipment provides a stable sinusoidal RF output however having a phase noise characteristic, as shown in Figure 3.16, higher than the simulated results previously presented in Figure 2.14 and Table 2.8, and thus, setting the limit for the minimum achievable phase noise.

The Spectrum analyzer is connected to one of the transmitter outputs and is used to analyze both the signal spectrum and phase noise. The utilized equipment is a Keysight EXA N9010B Signal Analyzer which, when measuring phase noise, provides the capability of measuring the equipment Displayed Average Noise Level (DANL).

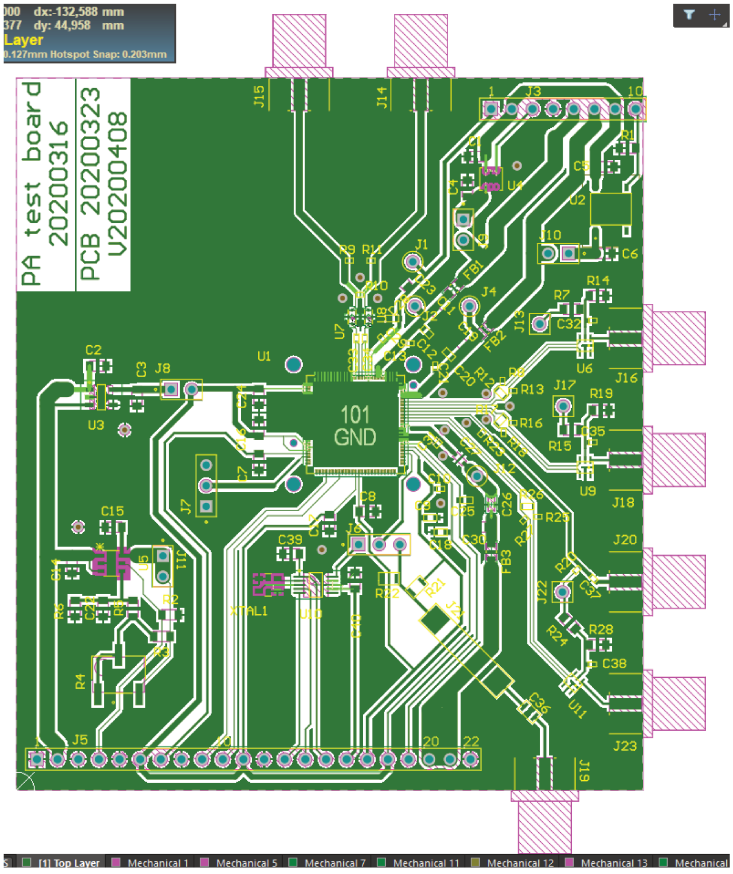


Figure 3.14 – PCB Layout used in the testbench.

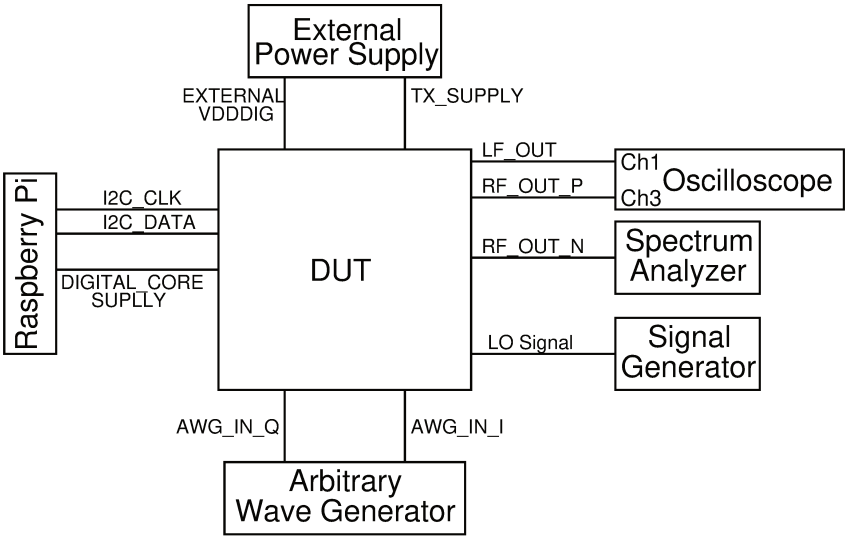


Figure 3.15 – Measurement testbench block diagram.

The DANL represents the smallest signal level that the equipment is able to measure due to its internal noise [25]. A DSA-X91604A oscilloscope is used to measure the low-frequency signal, which has a ratio of 1/16 of the reference input signal and also the transmitter output signal which can be analyzed and have its EVM derived.

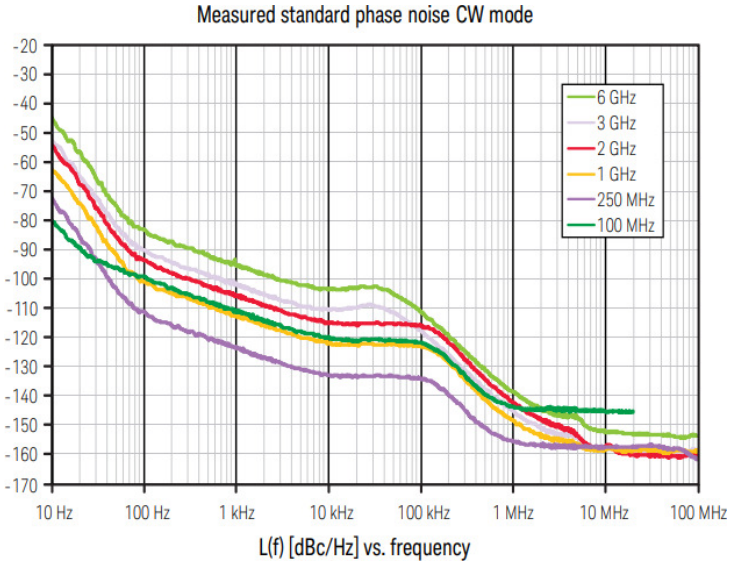


Figure 3.16 – EXG N5172B Phase noise characteristic[24]

A Raspberry Pi is utilized control to the register bank through I2C communication and also provides power to the voltage regulator responsible for powering digital circuitry core. An external power supply, Keysight N6705C DC power analyzer, is utilized to provide power to the voltage regulators of the transmitter and also to directly supply the containing the frequency divider, transmitter control logic and external data input processing circuits which all share the VDDDIG pin shown in Figure 3.13. Once there are other circuits powered by this same supply besides the frequency divider, a direct measurement of the circuit consumption is not possible, but a rough estimate is plausible.

Lastly, an M8190A Arbitrary Waveform Generator (AWG) is utilized to create external input signals to be provided as data to the transmitter. Although this generator is capable of providing both in-phase and quadrature signals deferentially, it was chosen by simplicity to use just single end signals and use onboard baluns to create the differential signal and thus reducing the number of cables needed to be attached to the PCB.

In Figure 3.17, a flowchart presenting the steps to do output frequency, current consumption, phase noise, and EVM measurements is presented. The EVM measurement is not a direct performance parameter of the frequency divider but a representative of the divider output signal duty-cycle as previously presented in chapter 2. It needs to be also taken into consideration that the transmitter itself may degrade the output signal EVM and thus the inferred duty-cycle will be an upper boundary for the circuit actual performance.

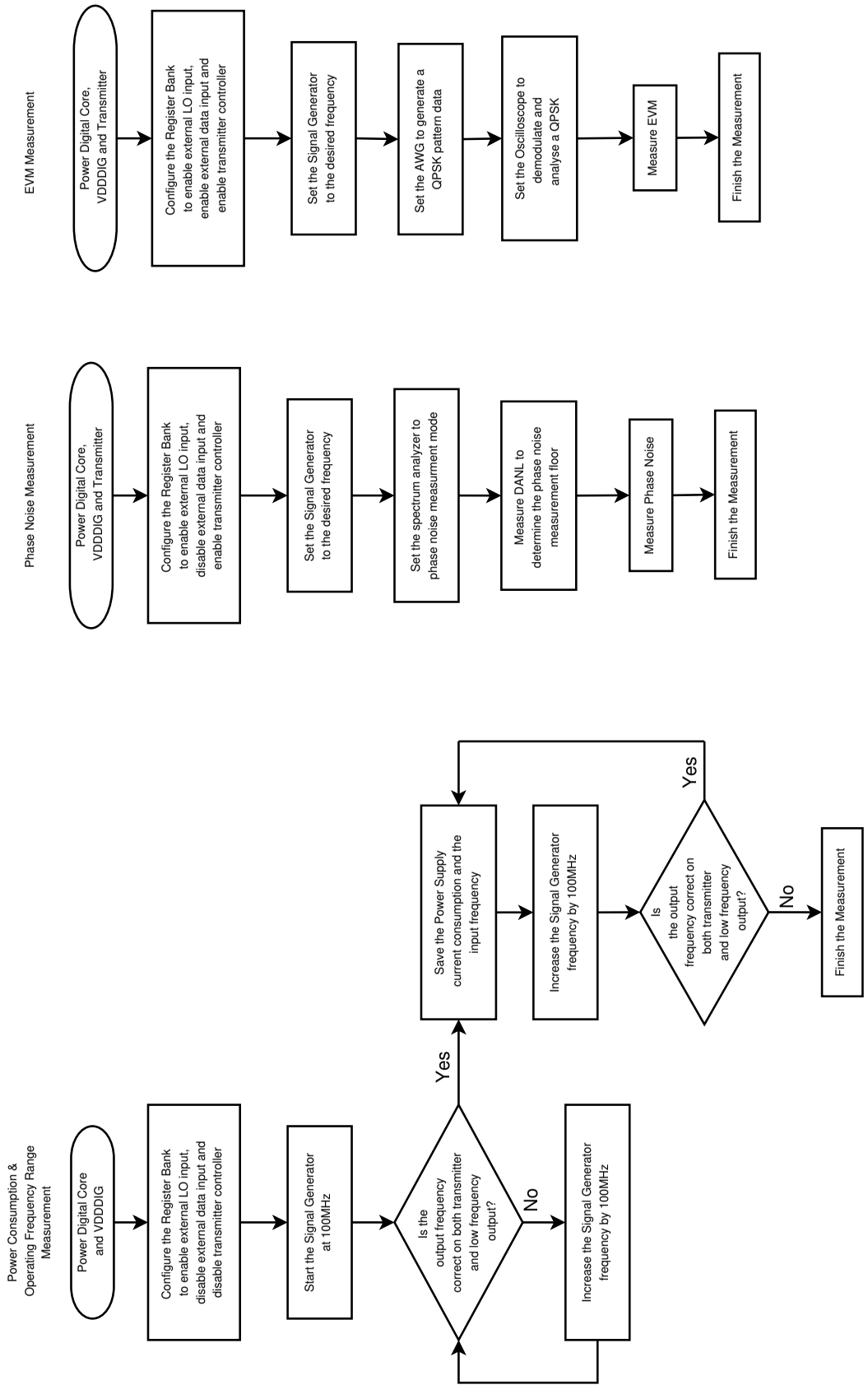
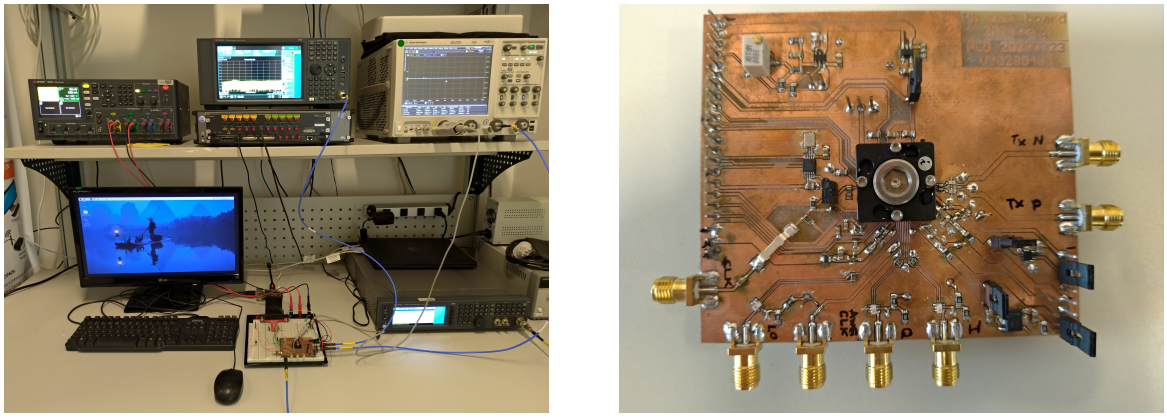


Figure 3.17 – Measurement Flowchart

Since it is already known, through previously extracted circuit simulations, that the circuit has problems when operating at nominal power supply voltage, the first measurement flow, designated as "Power Consumption & Operating Frequency Range Measurement" in Figure 3.17, is executed three times: one at 1.2 V (nominal voltage), one at 1.32 V (10% over nominal voltage) and finally one 1.4 V, that was the observed needed power supply voltage during extracted simulation to achieve correct operation at 1.8 GHz. Phase noise and EVM measurements are done only at 1.4 V supply since the operating frequency of interest to do this measure is at 1.8 GHz input frequency.

The testbench setup in the laboratory is shown in Figure 3.18a. The equipment M8190A in this setup is not connected since it is not used in the current measurement setup; the assembled PCB is shown in detail in 3.18b.



(a) Assembled testbench setup

(b) Fabricated printed circuit board.

Figure 3.18 – Testbench Assembly

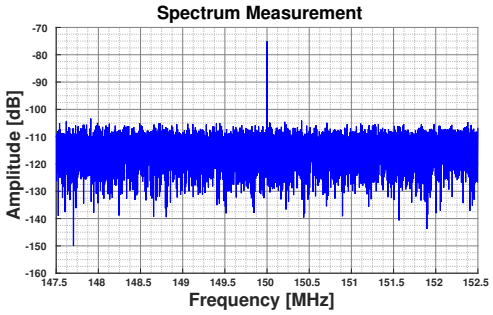
3.4 Measurements Results

Following the procedures presented in Figure 3.17, the obtained measurements are presented in the next sections. The two samples are identified as "A" and "B" throughout the presented results.

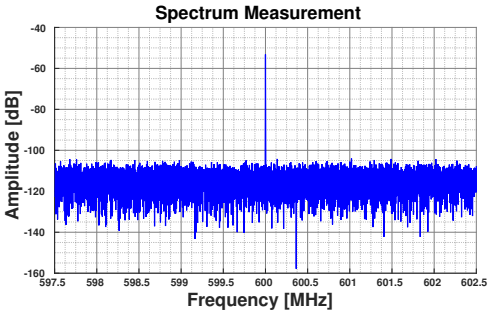
3.4.1 Input Frequency Range and Current Consumption Measurement

Figure 3.19 presents four different measured frequency spectrum for the boundaries regarding the input frequency range for sample A. These represent the measured signal spectrum at the transmitter output using a 5 MHz observation span, with a resolution bandwidth of 560 Hz. From (a) to (d), the measurements are as follows: divided minimum input frequency measured at 1.2 V and which is the same for all utilized voltages; divided

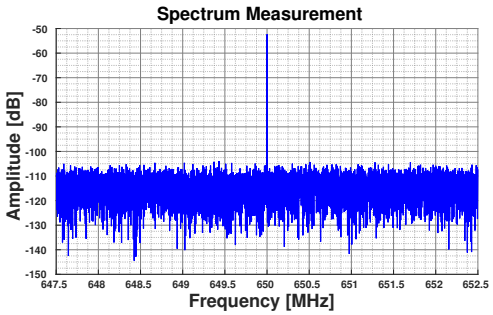
maximum input frequency at 1.2 V, 1.32 V and 1.4 V. As expected, the measured signal strength is quite low since goes to the output just through capacitive coupling.



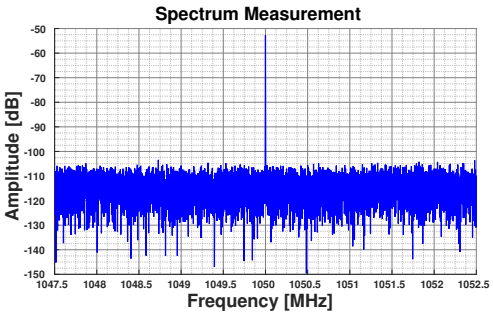
(a) 300MHz Input at 1.2V.



(b) 1200MHz Input at 1.2V.



(c) 1300MHz Input at 1.32V.



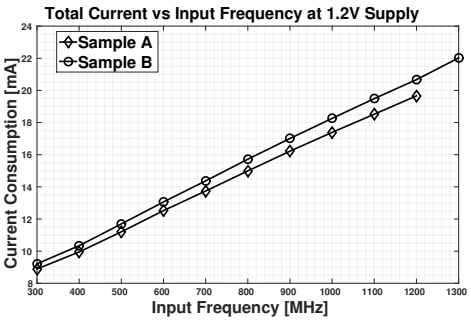
(d) 2100MHz Input at 1.4V.

Figure 3.19 – Observed output spectrum for frequency range boundary.

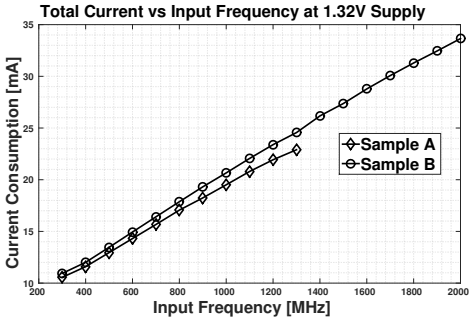
For each successful frequency measurement, the total measured current is also taken note. In Figure 3.20 is presented the complete current curve for each supply voltage for the complete operating range. In this case, the consumption of all other active blocks is also present.

Since the divider is a dynamic logic circuit, if the leakage current is not taken into consideration, the circuit should present a current consumption of 0 mA. This property can be exploited to obtain a better estimate of the divider power by doing a linear extrapolation ($y = mx + b$) of the measured data in Figure 3.20 and subtracting the y-intercept point (b), which represents the static DC current being drawn from the power supply. Figure 3.21 shows the results after this operation.

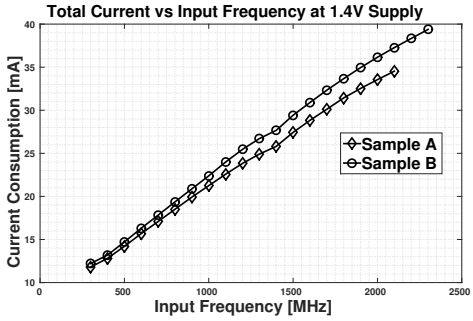
It can be noted from the measurements that the values are considerable higher than the obtained from the extracted simulation. A higher current is expected in the measurement since there are three other blocks, "Signal Bias", "Selector", and "Digital Divider" as shown in Figure 3.3, which are operating during the measurement process. Schematic level simulation using wields a current of 18.42 mA, and thus, the measurements represents an increase of around 30%. This increase in current is most probably due to capacitance greater than the expected for all other blocks, which also needs to be on, as occurred in the frequency divider.



(a) Total current at 1.2V

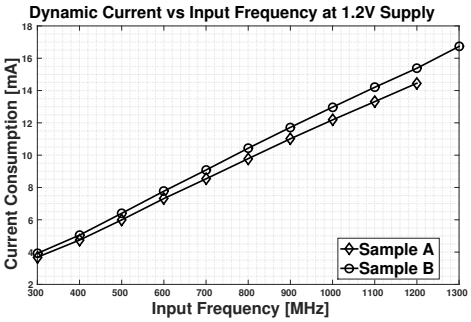


(b) Total current at 1.32V

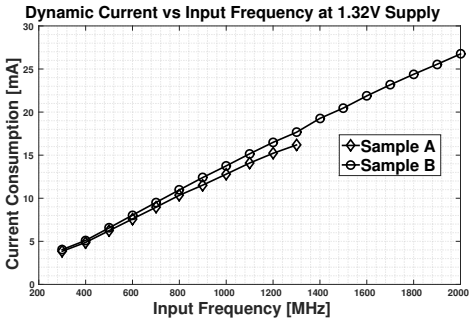


(c) Total current at 1.4V

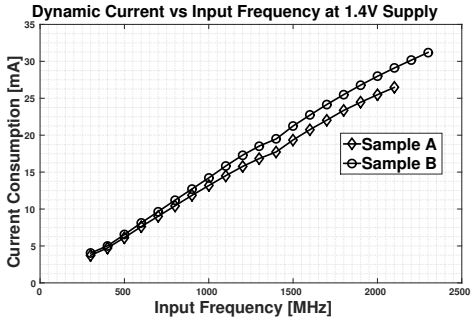
Figure 3.20 – Total current measured for each supply voltage.



(a) Dynamic current at 1.2V



(b) Dynamic current at 1.32V



(c) Dynamic current at 1.4V

Figure 3.21 – Total dynamic current measured for each supply voltage.

It is observed in sample B, when using a 1.32 V supply, a considerable higher input frequency range when compared to sample A. This behavior was not expected and cannot be readily explained since there is no more samples available to determine if sample

A presents a less than average input frequency range or if sample B is an exception. Process variation as a mechanism to explain this discrepancy is not believed to be the case, since this behavior is observed for just one supply value.

3.4.2 Phase Noise Measurement

The phase noise measurement is carried out using a fixed data to ensure a stable operation at the transmitter output and thus allowing a reliable phase noise measurement. Figure 3.22 presents the measured signal spectrum at the transmitter output. The signal generator source is set to output a waveform at 1.8 Ghz, while the measurement equipment configuration is a 50 kHz span with a 51 Hz resolution bandwidth. Now that the transmitter is powered on and the input signal for the controller is fixed and different than zero, the output signal observed is effectively a amplified sinusoid at a frequency equal to $f_{in}/2$. The measured peak is at 899.996 MHz, which is within the tolerance of the signal generator source.

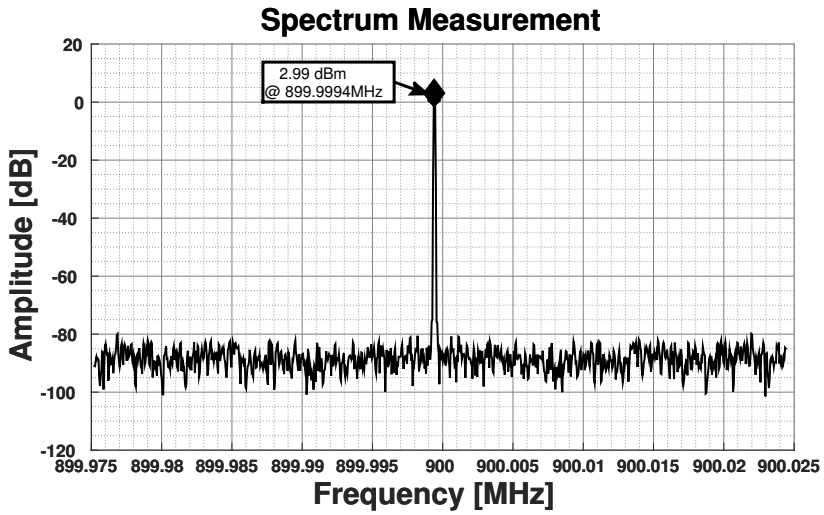


Figure 3.22 – Measured signal output spectrum used for phase noise measurements.

Switching the equipment measuring mode to observe the signal phase noise, now the setup is configured to observe an offset frequency from the fundamental. Thus, the center frequency is set to the previously measured frequency of 899.996 MHz and an the offset frequency range is set from 10 Hz to 40 MHz. Using this setup, both the equipment DANL and the signal phase noise are measured presented in Figure 3.23, together with the simulated phase noise of the divider. Comparing this measurement with the result from Figure 2.14, it is immediately clear that the measure phase noise is much higher than expected through simulation but this happens due to two factors. For offset frequencies higher than 1 MHz the measurement is bound by the measuring equipment DANL and thus is not possible to measure a phase noise better than approximately -135 dBc/Hz.

On the other hand, when measuring offsets below 1 MHz the phase noise is bound by the generator signal source as previously presented in Figure 3.16.

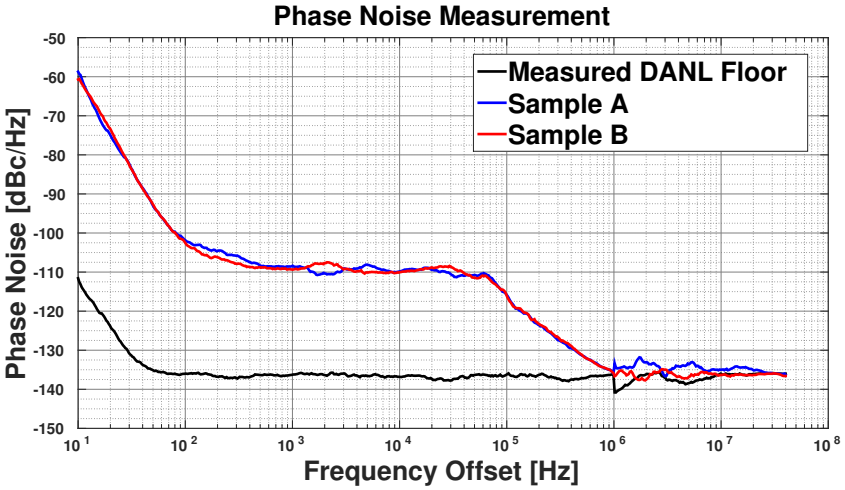


Figure 3.23 – Measured divider phase noise and equipment DANL.

Another measurement that can be obtained from the phase noise is the equivalent jitter. The spectrum analyzer utilized provides this functionality and returns the value in degrees, then utilizing equation 3.1 the corresponding jitter can be calculated. The obtained result are 553 fs and 537 fs for sample A and B respectively.

$$RMS_{JITTER} = \frac{RMS_{PHASE}}{360 f_c} \tag{3.1}$$

3.4.3 EVM Measurement

To proceed with EVM measurements, an external complex modulated (I-Q) baseband signal needs to be inject in the transmitter. The signal is generated using MATLAB® with a 225 MHz sample rate and a 10-bit resolution. The bits are then serialized into a 2.25 Gb/s. Inside the transmitter this signal is deserialized by the block identified as "External Data Input Processing" in Figure 3.3. Due to the high speed switching present in this block some problems were observed when running this test. When inputting an static data the expected signal single tone amplitude at the transmitter output is observed, but when feeding a signal with the required 225 MHz sample rate the deserializer was not able to correctly output the data and thus rending the test impossible.

3.5 Measurements Final Considerations

Although not being directly measured due to the non availability of the circuit direct outputs, the circuit performance seems to reasonably match the expected results from simulation regarding the input frequency range and current consumption. Regarding

phase noise, it is not possible to do a direct comparison to simulations since the equipment available to make the measurements cannot either generate or sense the simulated phase-noise levels. Though it is reasonably to assume that the circuit can achieve the simulated performance since the measured results can be viewed as an upper boundary for performance. Comparison between the proposed divider with others presented in literature is not possible since several problems were encountered after fabrication that heavily impairs the circuit performance.

Conclusion

This work presented a frequency divider aimed to a IEEE802.15.4g transceiver. The design process, from theory to measurements, is shown and discussed. Chapter 1 discussed the motivation and need of a frequency divider in communication systems as well the possible topologies that can be used to implement one. Comparison between them were drawn to devise the most appropriate one to fit into the purpose of the project.

In Chapter 2, the performance specifications are drawn and the impact of each one in the overall system is explained. Section 2.3 details the working principle and the design process of the chosen topology. Simulation results, from schematic to layout extracted circuits, were shown and performance limitations of the fabricated circuit that could not be addressed due to design tools unavailability are explained.

Chapter 3 presents issues encountered during the measurement process and how they were addressed, then follows with the measurement process and results. As far as it was possible to compare the simulated and the measured values an agreement between them is observed regarding power and input frequency range. Although phase noise measurements are limited by the available equipment to run the tests, the measurements are in accordance in the offset range that presents similar conditions to the simulation environment.

Future work comprises the redesign of the circuit. It aims to correct the operation problems observed in this work and also make the measurement process more direct. The main change to the circuit design is to, instead of sizing the divider last stage to drive the output load, add a dedicated buffering circuit. This approach allows for smaller transistor sizes for the frequency divider overall. Since the divider's last stage sizing is reduced to drive only the buffer input capacitance, the transistor intrinsic capacitance is smaller. Therefore, the size of the transistors from the previous stages can be reduced. The main goal of adopting this approach is to obtain a potentially higher operating frequency for the circuit core due to the reduced capacitance. The separation of the divider and buffers is also important once it allows different power supplies in each block. This separation makes it possible to measure only the divider core power consumption, which is the metric usually observed in published works.

The new version of the frequency divider is to be fabricated as a standalone block with direct access to all the inputs and outputs, allowing the direct measurement of all needed performance parameters. Also, since the frequency divider will not be part of a complete system, there will be no other external influence, such as observed in the measurements obtained in this work.

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Annex

ANNEX A – EVM equations for a 25% and 50% Duty-Cycle

As presented in [3], it is shown below how to compute an IQ signal EVM when considering different duty-cycle conditions. The LO signals are considered to be perfect rectangular waves but since the wave at the transmitter output is filtered by a matching network only the fundamental component of the square wave is considered in the equations. The EVM definition is presented in Equation A.1 where V_{ideal} is the fundamental component of the square wave in a case where there is no error in the duty-cycle.

$$EVM = \frac{1}{V_{ideal}}\sqrt{\frac{1}{N}\sum_{i=1}^{N} e_i^2} \tag{A.1}$$

A.1 25% Duty-Cycle Case.

The fundamental components for each LO phase in a 25% duty-cycle square wave are described as:

$$\vec{U}_{1,0} = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t\right) \tag{A.2}$$

$$\vec{U}_{0,1} = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t + \frac{\pi}{2}\right) = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\sin\left(\omega t\right) \tag{A.3}$$

$$\vec{U}_{-1,0} = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t + \pi\right) = -\frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t\right) \tag{A.4}$$

$$\vec{U}_{0,-1} = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t + \frac{3\pi}{2}\right) = -\frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\sin\left(\omega t\right) \tag{A.5}$$

An error Δt_1 in the wave's duty-cycle is now considered for all LO phases. Also assuming the vector $1,0$ as the reference, a phase error of Δt_2 can be inserted in the equations. The vectors can be rewritten now as:

$$\vec{U}'_{1,0} = \frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos\left(\omega t\right) \tag{A.6}$$

$$\vec{U}'_{0,1} = \frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos\left(\omega t + \frac{\pi}{2}\right) = \frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\sin\left(\omega t + \omega\Delta t_2\right) \tag{A.7}$$

$$\vec{U}'_{-1,0} = \frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos\left(\omega t + \pi\right) = -\frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\cos\left(\omega t + \omega\Delta t_2\right) \tag{A.8}$$

$$\vec{U}'_{0,-1} = \frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos\left(\omega t + \frac{3\pi}{2}\right) = -\frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\sin\left(\omega t + \omega\Delta t_2\right) \tag{A.9}$$

Computing then the error vector for each phase:

$$\vec{e}_{1,0} = \frac{2}{\pi}\left[\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right) - \sin\left(\frac{\pi}{4}\right)\right]\cos\left(\omega t\right) \tag{A.10}$$

$$\begin{aligned}\vec{e}_{0,1} = \frac{2}{\pi}&\left[\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos\left(\omega\Delta t_2\right) - \sin\left(\frac{\pi}{4}\right)\right]\sin(\omega t) \\ &+\frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\sin(\omega\Delta t_2)\cos(\omega t)\end{aligned} \tag{A.11}$$

$$\begin{aligned}\vec{e}_{-1,0} = \frac{2}{\pi}&\left[\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos(\omega\Delta t_2) - \sin\left(\frac{\pi}{4}\right)\right]\cos(\omega t) \\ &+\frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\sin(\omega\Delta t_2)\sin(\omega t)\end{aligned} \tag{A.12}$$

$$\begin{aligned}\vec{e}_{0,-1} = \frac{2}{\pi}&\left[\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\cos(\omega\Delta t_2) - \sin\left(\frac{\pi}{4}\right)\right]\cos(\omega t) \\ &-\frac{2}{\pi}\sin\left(\frac{\pi}{4} + \pi\frac{\Delta t_1}{T}\right)\sin(\omega\Delta t_2)\cos(\omega t)\end{aligned} \tag{A.13}$$

A.2 50% Duty-Cycle Case.

In a similar manner as of the 25% deduction, the fundamental components for a 50% duty-cycle LO waves are described as:

$$\vec{U}_{1,1} = \frac{2}{\pi}\sin\left(\frac{\pi}{2}\right)\frac{1}{\sqrt{2}}\left[\cos\left(\omega t\right) + \sin(\omega t)\right] \tag{A.14}$$

$$\vec{U}_{-1,1} = \frac{2}{\pi}\sin\left(\frac{\pi}{2}\right)\frac{1}{\sqrt{2}}\left[-\cos\left(\omega t\right) + \sin(\omega t)\right] \tag{A.15}$$

$$\vec{U}_{-1,-1} = \frac{2}{\pi}\sin\left(\frac{\pi}{2}\right)\frac{1}{\sqrt{2}}\left[-\cos\left(\omega t\right) - \sin(\omega t)\right] \tag{A.16}$$

$$\vec{U}_{1,-1} = \frac{2}{\pi}\sin\left(\frac{\pi}{2}\right)\frac{1}{\sqrt{2}}\left[\cos\left(\omega t\right) - \sin(\omega t)\right][5pt] \tag{A.17}$$

Considering that the duty-cycle error is now represented as Δt_3 and the phase error as Δt_4 the error vectors are written as:

$$\begin{aligned}\vec{e}_{1,1} = &\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[\cos(\omega\Delta t_4)+\sin(\omega\Delta t_4)] - \sin(\frac{\pi}{2})\cos(\omega t)\\ &+\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[\cos(\omega\Delta t_4)-\sin(\omega\Delta t_4)] - \sin(\frac{\pi}{2})\sin(\omega t)\end{aligned} \tag{A.18}$$

$$\begin{aligned}\vec{e}_{-1,1} = &\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[-\cos(\omega\Delta t_4)+\sin(\omega\Delta t_4)] + \sin(\frac{\pi}{2})\cos(\omega t)\\ &+\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[\cos(\omega\Delta t_4)+\sin(\omega\Delta t_4)] - \sin(\frac{\pi}{2})\sin(\omega t)\end{aligned} \tag{A.19}$$

$$\begin{aligned}\vec{e}_{-1,-1} = &\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[-\cos(\omega\Delta t_4)-\sin(\omega\Delta t_4)] + \sin(\frac{\pi}{2})\cos(\omega t)\\ &+\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[\cos(-\omega\Delta t_4)+\sin(\omega\Delta t_4)] + \sin(\frac{\pi}{2})\sin(\omega t)\end{aligned} \tag{A.20}$$

$$\begin{aligned}\vec{e}_{1,-1} = &\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[\cos(\omega\Delta t_4)-\sin(\omega\Delta t_4)] - \sin(\frac{\pi}{2})\cos(\omega t)\\ &+\frac{\sqrt{2}}{\pi}\sin(\frac{\pi}{2}+\pi\frac{\Delta t_3}{T})[-\cos(\omega\Delta t_4)-\sin(\omega\Delta t_4)] + \sin(\frac{\pi}{2})\sin(\omega t)\end{aligned} \tag{A.21}$$

A general expression for the error vector in both cases can be written as follows:

$$\vec{e}_{i,j} = a_{i,j}\cos(\omega t)+\sin(\omega t), \quad i,j \in (-1,0,1), b_{1,0}=0 \tag{A.22}$$

Thus a general EVM expression can be finally written as presented in Equation A.23.

$$EVM = \frac{\sqrt{a_{i,j}^2+b_{i,j}^2}}{\frac{\sqrt{2}}{\pi}} \tag{A.23}$$

To plot the curves presented in Figure 2.4 the phase errors Δt_2 and Δt_4 are considered to be 0 since this is not the desired variable to be analyzed. The signal period (T) and the duty-cycle error Δt_1 and Δt_3 corresponds to a $900MHz$ square wave and a $\pm 1\%$ variation.

ANNEX B – Complete Test board schematics and Bill of materials

The following section presents the bill of materials needed to assembly the PCB used for testing and appendix B.2 presents the correspondent schematics.

B.1 Bill of Materials

Table B.1 – Bill of materials for test board.

Component	Description	Designator	Quantity
2.2uF (0805)	CAP ceramic 2.2 uF 6V ± 10%	C1, C2, C3, C4, C5,C6, C14, C15, C39, C4	10
100nF (0805)	Generic non-polar capacitor	C7, C8, C16, C17, C24	5
100nF (0603)	Generic non-polar capacitor	C9, C12, C18, C20, C25	5
100pF (0402)	Generic non-polar capacitor CAP 100pF 10V ± 10% 0402	C10, C13, C21, C29, C31, C37	6
10uF (0805)	Generic non-polar capacitor	C11, C19, C30	3
10nF (0805)	CAP ceramic 10nF 6V ± 10%	C22	1
1uF (0805)	Generic non-polar capacitor	C23	1
NFM18PS105 D0J3D	Chip EMIFIL(R) Chip 3-Terminal Capacitor High Insertion Loss Type for Large Current,1 uF, +/-20%, 6.3 V	C26	1

To be continued

Table B.1 (continued)

Component	Description	Designator	Quantity
NFM18PC104 R1C3D	100nF Feed Through Capacitor 16V 2A 30mOhm 0603, 3 PC Pad	C27	1
1nF (0603)	Generic non-polar capacitor	C28	
68pF (0402)	RF bypass ceramic capacitor	C32, C35, C38	3
68pF (0402)	RF bypass ceramic capacitor	C33, C34	2
100nF (0805)	CAP 100nF 10V ± 10%	C36	1
MPZ2012S601A	Chip Bead for Power Line, 600 Ohm, +/- 25%, 2 A, -55 to 125 degC, 2-Pin SMD (0805)	FB1, FB2, FB3	3
Test point	Test point, TH	J1, J2, J4, J12	4
TSW-150-16-T-S 1x8, 2.54 mm, 20mm length	THT Vertical Pin Header, Pitch 2.54 mm, Single Row, 8 pins. Based on Wurth 1x32 header CMP-1502-01118-1, 61303211121.	J3	1
TSW-150-16-T-S 1x22, 2.54 mm, 20mm length	THT Vertical Pin Header WR-PHD, Pitch 2.54 mm, Single Row, 22 pins. Based on Wurth 1x32 header CMP-1502-01118-1, 61303211121	J5	1
Header 1x3	Male Header, Pitch 2.54 mm, 1 x 3 Position, Height 8.38 mm, Tail Length 3.18 mm	J6, J7	2
Jumper NC.	Header 1 row 2 positions	J8, J9, J10	3
Header 1x2	Header 1 row 2 positions	J11	1
Header 1x1	THT Vertical Pin Header WR-PHD, Pitch 2.54 mm, Single Row, 1 pins	J13, J17, J22	3

To be continued

Table B.1 (continued)

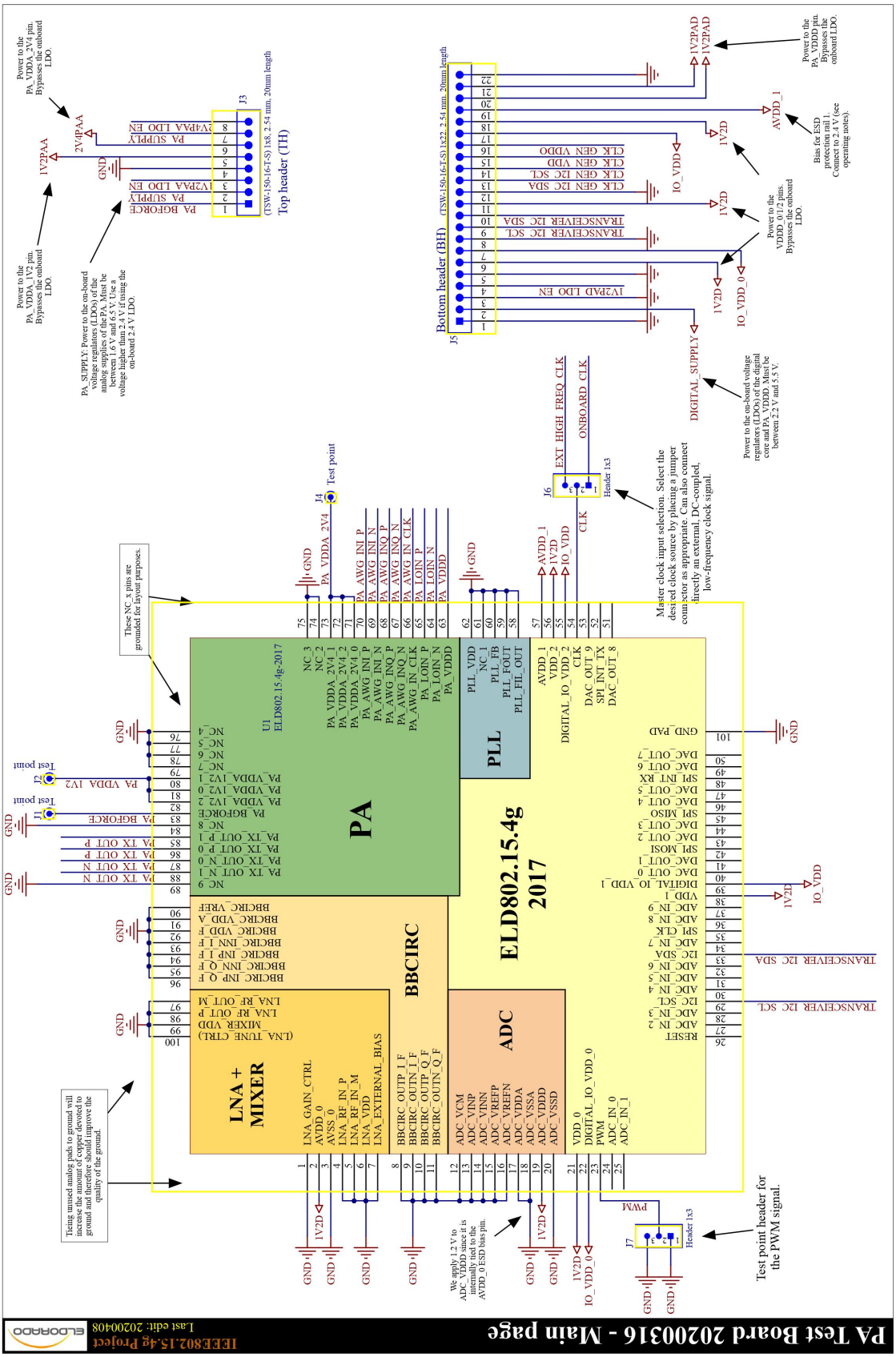
Component	Description	Designator	Quantity
CON-SMA EDGE-S	RF Solutions SMA female edge mount jack for 0.060" thick boards	J14, J15, J16, J18, J19, J20, J23	7
Air jumper	Keystone 5104: miniature SMT air jumper (12.3mm)	J21	1
10kOhm (0805)		R1, R2, R3, R6	4
84WR10KLFTR	TT Electronics 84WR10KLFTR multi-turn trimmer potentiometer model 84, 10 kOhm, 1/4 W, 12 turns, 10%	R4	1
4.7kOhm (0805)		R5	1
1kOhm (0805)		R7, R14, R15, R19, R24,R28	6
220Ohm (0603)	RF termination resistor. Susumu RG1608P-221-D-T5, RES SMD 220 OHM 0.5% 1/10W 0603	R12, R17, R26	3
100Ohm (0402)	RF termination resistor. Yageo RC0402JR-07100RL, RES SMD 100 OHM 5% 1/16W 0402	R20, R23	2
100Ohm (0805)		R21, R22	2
ELD802.15.4g v2017	IEEE802.15.4g radio transceiver. Version 2017	U1	1
RP132S241B E2-FE	Ricoh RP132S241B-E2-FE 2.4V Low Voltage 1A Voltage Regulator (LDO Regulator)	U2	1

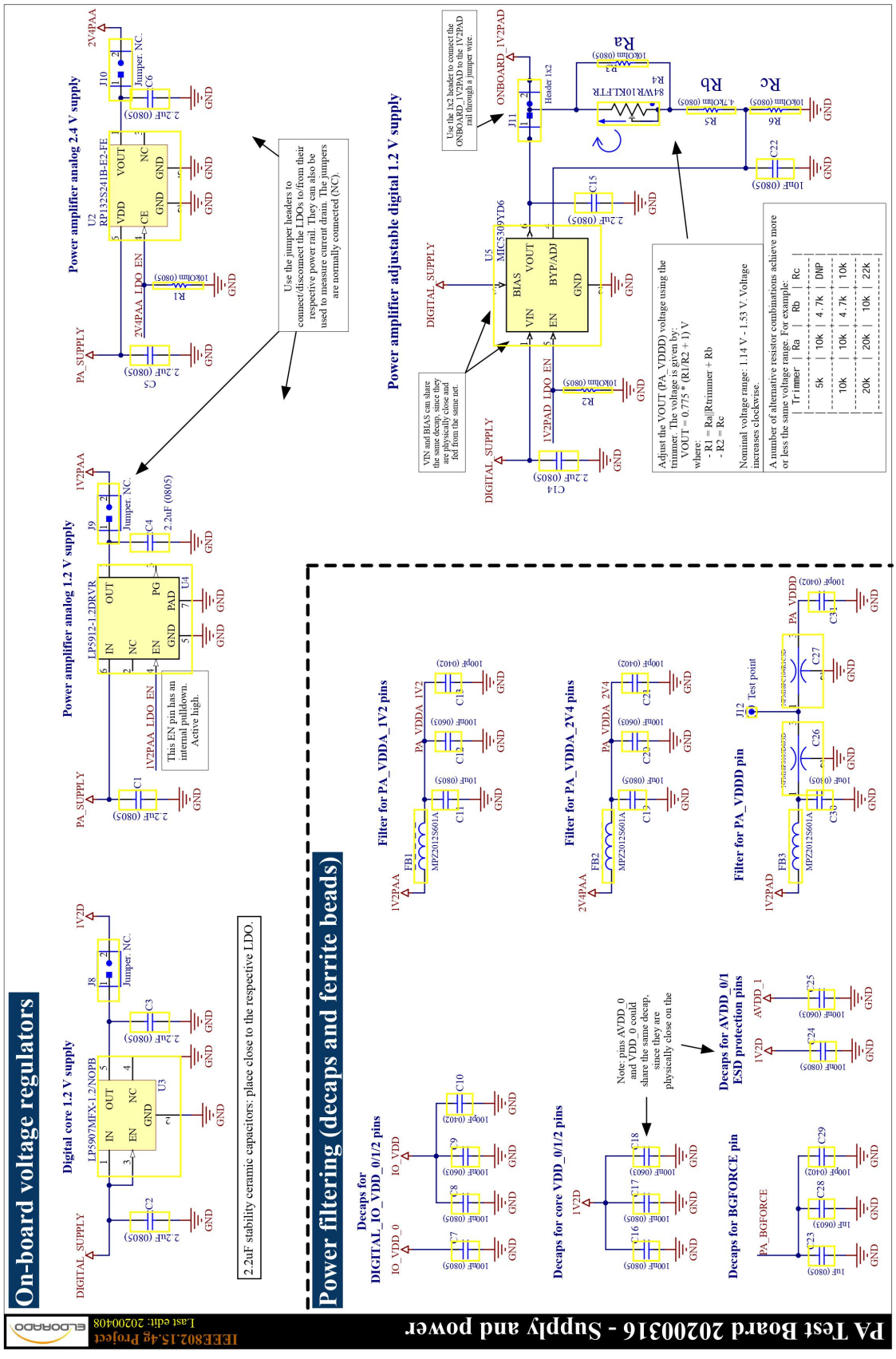
To be continued

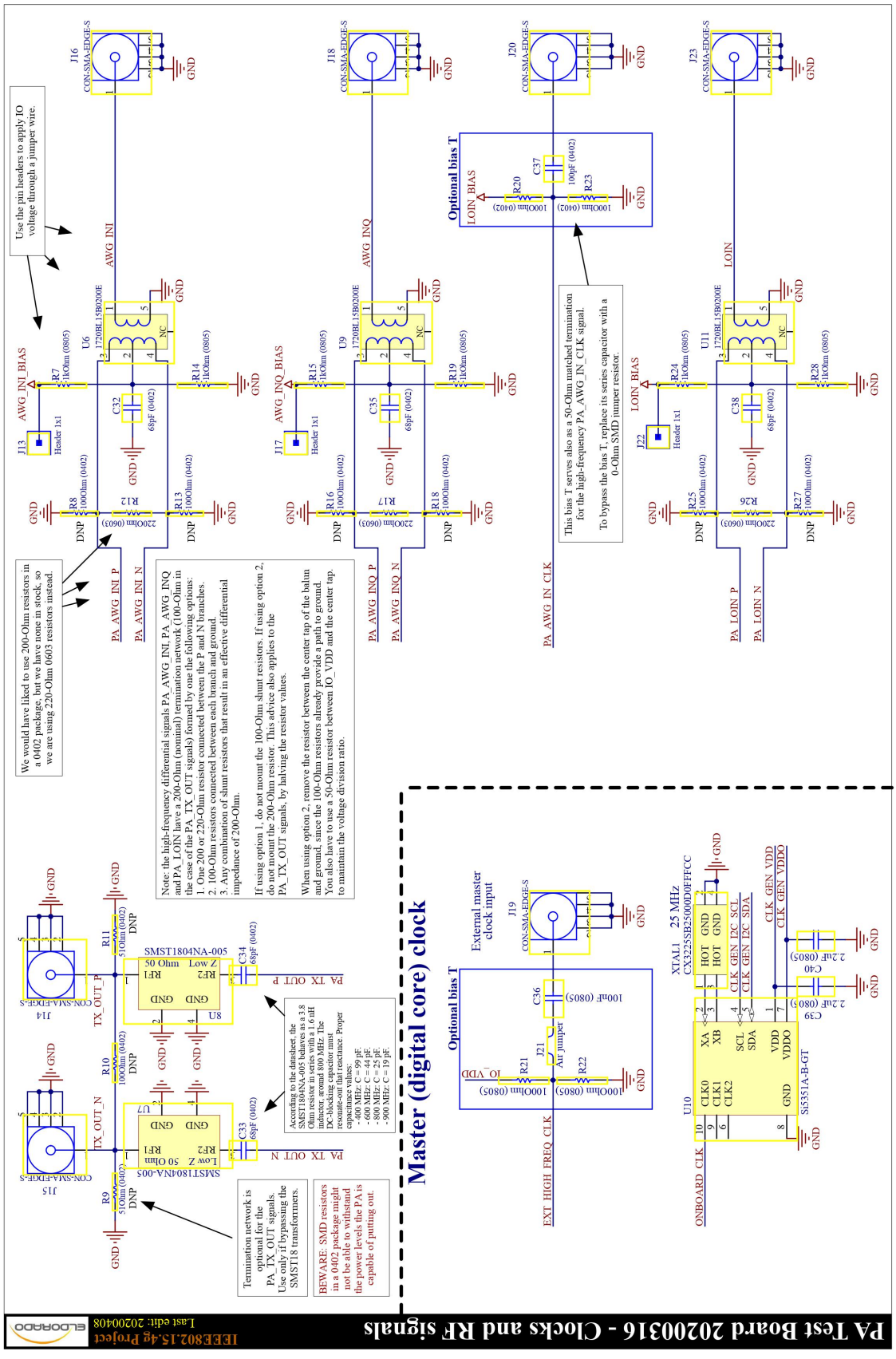
Table B.1 (continued)

Component	Description	Designator	Quantity
LP5907MFX-1.2/NOPB	Ultra-Low-Noise, Low-IQ LDO, 0.25 A, Fixed 1.2V Output, 2.2 to 5.5 V Input, -40 to 125 degC, 5-Pin SOT-23	U3	1
LP5912 1.2DRVR	Texas Instruments LP5912 500-mA Low-Noise,Low-IQ LDO. 1.2 V	U4	1
MIC5309YD6	Microchip MIC5309YD6 low Vin/Vout 300 mA high PSRR ULDO with ultra-low IQ	U5	1
1720BL15B0200E	Johanson Technology 625 - 2815 MHz wideband balun,1:4 impedance ratio (50 Ohm : 200 Ohm)	U6, U9, U11	3
SMST1804NA-005	Murata SMST18XX series RF transformer. 4-Ohm on low-Z side to 50 Ohm @ 800 MHz	U7, U8	2
Si5351A-B-GT	I2C-Programmable Any-Frequency CMOS Clock Generator + VCXO, 2.5 / 3.3 V, 0.008 to 160 MHz Output, -40 to 85 degC, 10-pin SOP	U10	1
CX3225SB25000D0FFFCC	Kyocera CX3225SB SMD quartz crystal; 25 MHz, 8 pF	XTAL1	1

B.2 Board Schematics


PA Test Board 20200316 - Main page
IEEE802.15.4g Project
Last edit: 20200408
ELDORADO
ELD802.15.4g
2017
PA
PLL
BBCIRC
ADC
LNA + MIXER
U1
ELD802.15.4g-2017
Top header (TH)
(TSW-150-16-T-S) 1x8, 2.54 mm, 20mm length
Bottom header (BH)
(TSW-150-16-T-S) 1x22, 2.54 mm, 20mm length
Test point
Header 1x3
Power to the PA_VDDA_2V4 pin. Bypasses the onboard LDO.
PA_SUPPLY: Power to the on-board voltage regulators (LDOs) of the analog supplies of the PA. Must be between 1.6 V and 6.5 V. Use a voltage higher than 2.4 V if using the on-board 2.4 V LDO.
Power to the PA_VDDA_1V2 pin. Bypasses the onboard LDO.
Power to the VDDD_1V2 pins. Bypasses the onboard LDO.
Bias for ESD protection rail. Connect to 1.1 V (see operating notes).
DIGITAL_SUPPLY: Power to the on-board voltage regulators (LDOs) of the digital core and PA_VDDD. Must be between 2.2 V and 5.5 V.
Master clock input selection. Select the desired clock source by placing a jumper connector as appropriate. Can also connect directly an external, DC-coupled, low-frequency clock signal.
These NC_x pins are grounded for layout purposes.
Tieing unused analog pads to ground will increase the amount of copper devoted to ground and therefore should improve the quality of the ground.
We apply 1.2 V to ADC_VDDD since it is internally tied to the AVDD_0 ESD bias pin.
Test point header for the PWM signal.


PA Test Board 20200316 - Supply and power
IEEE802.15.4g Project
Last edit: 20200408
On-board voltage regulators
Power filtering (decaps and ferrite beads)
Digital core 1.2 V supply
LP5907MFX-1.2/NOPB
Power amplifier analog 2.4 V supply
RP132S241B-E2-FE
Power amplifier analog 1.2 V supply
LP5912-1.2DRVR
Power amplifier adjustable digital 1.2 V supply
MIC5309YTD6
Use the jumper headers to connect/disconnect the LDOs to/from their respective power rail. They can also be used to measure current drain. The jumpers are normally connected (NC).
2.2uF stability ceramic capacitors; place close to the respective LDO.
This EN pin has an internal pulldown. Active high.
VIN and BIAS can share the same decap, since they are physically close and fed from the same net.
Use the 1x2 header to connect the ONBOARD_1V2PAD to the 1V2PAD rail through a jumper wire.
Adjust the VOUT (PA_VDDD) voltage using the trimmer. The voltage is given by:
VOUT = 0.775 * (R1/R2 + 1) V
where:
- R1 = Ra||Rtrimmer + Rb
- R2 = Rc
Nominal voltage range: 1.14 V - 1.53 V. Voltage increases clockwise.
A number of alternative resistor combinations achieve more or less the same voltage range. For example:
Trimmer | Ra | Rb | Rc
5k | 10k | 4.7k | DNP
10k | 10k | 4.7k | 10k
20k | 20k | 10k | 22k
Filter for PA_VDDA_1V2 pins
Filter for PA_VDDA_2V4 pins
Filter for PA_VDDD pin
Decaps for DIGITAL_IO_VDD_0/1/2 pins
Decaps for core VDD_0/1/2 pins
Note: pins AVDD_0 and VDD_0 could share the same decap, since they are physically close on the
Decaps for AVDD_0/1 ESD protection pins
Decaps for BGFORCE pin

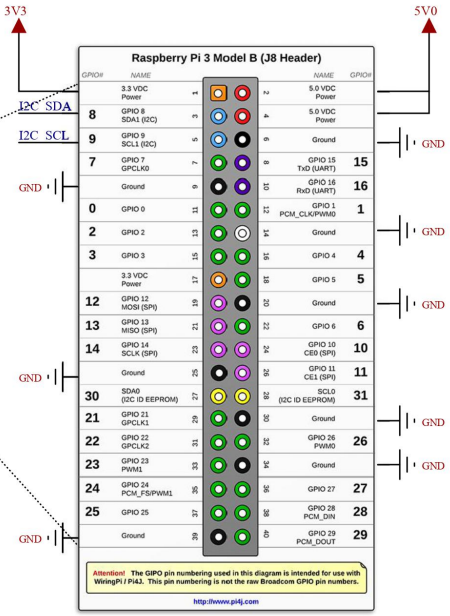

PA Test Board 20200316 - Clocks and RF signals
IEEE802.15.4g Project
Last edit: 20200408
Master (digital core) clock
External master clock input
Optional bias T
Optional bias T
Use the pin headers to apply IO voltage through a jumper wire.
We would have liked to use 200-Ohm resistors in a 0402 package, but we have none in stock, so we are using 220-Ohm 0603 resistors instead.
Note: the high-frequency differential signals PA_AWG_INI, PA_AWG_INQ and PA_LOIN have a 200-Ohm (nominal) termination network (100-Ohm in the case of the PA_TX_OUT signals) formed by one the following options:
1. One 200 or 220-Ohm resistor connected between the P and N branches.
2. 100-Ohm resistors connected between each branch and ground.
3. Any combination of shunt resistors that result in an effective differential impedance of 200-Ohm.
If using option 1, do not mount the 100-Ohm shunt resistors. If using option 2, do not mount the 200-Ohm resistor. This advice also applies to the PA_TX_OUT signals, by halving the resistor values.
When using option 2, remove the resistor between the center tap of the balun and ground, since the 100-Ohm resistors already provide a path to ground. You also have to use a 50-Ohm resistor between IO_VDD and the center tap, to maintain the voltage division ratio.
This bias T serves also as a 50-Ohm matched termination for the high-frequency PA_AWG_IN_CLK signal.
To bypass the bias T, replace its series capacitor with a 0-Ohm SMD jumper resistor.
According to the datasheet, the SMST1804NA-005 behaves as a 3.8 Ohm resistor in series with a 1.6 nH inductor around 900 MHz. The DC-blocking capacitor must resonate-out that reactance. Proper capacitance values:
- 400 MHz: C = 99 pF.
- 600 MHz: C = 44 pF.
- 800 MHz: C = 25 pF.
- 900 MHz: C = 19 pF.
Termination network is optional for the PA_TX_OUT signals. Use only if bypassing the SMST18 transformers.
BEWARE: SMD resistors in a 0402 package might not be able to withstand the power levels the PA is capable of putting out.
J16
J18
J20
J23
J13
J17
J22
J19
J21
J14
J15
U6
U9
U11
U7
U8
U10
AWG_INI
AWG_INQ
LOIN
AWG_INI_BIAS
AWG_INQ_BIAS
LOIN_BIAS
LOIN_BIAS
PA_AWG_INI_P
PA_AWG_INI_N
PA_AWG_INQ_P
PA_AWG_INQ_N
PA_AWG_IN_CLK
PA_LOIN_P
PA_LOIN_N
PA_TX_OUT_P
PA_TX_OUT_N
TX_OUT_P
TX_OUT_N
EXT_HIGH_FREQ_CLK
ONBOARD_CLK
IO_VDD
CLK_GEN_VDD
CLK_GEN_VDDO
CLK_GEN_I2C_SCL
CLK_GEN_I2C_SDA
XTAL1 25 MHz
CX3225SB25000D0FEFCC
Si5351A-B-GT
SMST1804NA-005
CON-SMA-EDGE-S
Header 1x1
1720BL15B0200E
GND
DNP
NC

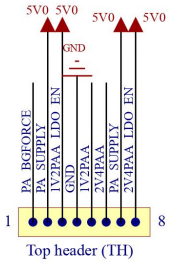
Setup and usage example

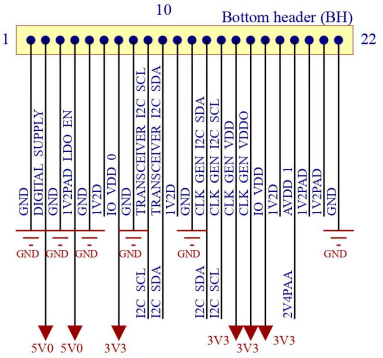
This power amplifier test board was designed to be used in conjunction with a Raspberry Pi 3 single-board computer (tough other supporting hardware can be used). The diagrams below show a usage example for the typical configuration:

- The ELD802.15.4g-2017 IC under test is powered from the on-board voltage regulators (LDOs).
- The supply for the on-board LDOs comes from the Raspberry Pi 3 board.
- I/O voltage coming from the Raspberry Pi 3 board (3.3 V).
- Digital core clocked from the on-board programmable clock (which must be configured via I2C on power-on).

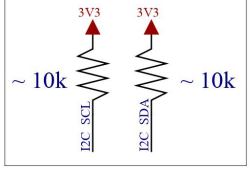
Raspberry Pi 3 Model B+







Pull-up resistors might be needed on the I2C lines, if using a different I2C master or custom pins for I2C communication. Resistor values around 10 kOhm should work fine here.



ANNEX C – WCAS 2017 Paper

Paper submitted and accepted for oral presentation on the 7^{th} Workshop on Circuits and System Design (WCAS 2017) at Fortaleza, Ceará. The paper also received the Best Paper Award.

Low Phase-Error Differential Frequency Divider for Quadrature LO Generation

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ABSTRACT

The Local Oscillator (LO) generation block is a key component in a transceiver architecture. Besides phase noise, LO impairments such as duty-cycle reduction and phase imbalance produced by the LO divider can severely degrade the spectral performance. In this paper, an alternative LO frequency divider implementation is proposed, providing reduced phase error between complementary and quadrature LO phases with a reduced power consumption given by a True Single Phase Clock (TSPC) based implementation. Using a CMOS 65nm technology, Monte Carlo circuit simulations show a worst-case phase error of less than 1°, with an output noise better than -163 dBc/Hz (at 40 MHz) and power consumption of 0.218 mW/GHz.

KEYWORDS

Local Oscillator, Frequency Divider, Low Noise, Low Phase-Error, RF

1 INTRODUCTION

With the current outlook of billions of new devices being incorporated into the network over the coming years, it is evident that the Internet of Things – and its foreseen tremendous number of applications – will have a huge impact on both economy and society. Though battery lifetime has always been an important aspect of mobile communication devices, in particular to IoT and Wireless Sensor Networks (WSN) the power consumption should be on par with the expected device's lifetime, otherwise the impact in communication reliability and the excessive battery replacement costs would simply become prohibitive to most applications.

Since the power budget in wireless communication devices is typically dominated by the radio frontend, a drastic reduction of the transceiver impact has been a major goal in the past decade. However, especially regarding transceiver frontends, the clear trade-off between power consumption and performance metrics (e.g. radiated output power, linearity, sensitivity) places difficult challenges to further reduce the radio contribution.

The Local Oscillator (LO) generation blocks have always been among the top contributors in power consumption, typically due to stringent phase noise specifications. Moreover, besides phase noise, other impairments such as duty-cycle reduction and/or phase imbalance between the different LO phases can also severely degrade the spectral performance in cartesian architectures. As a result, register-based divider implementations are not completely suitable for LO generation, since the inverter delay at the complementary output produces phase deviation between complementary LO phases. By extension, other power efficient single-ended topologies (such as [3]) fall short for the same reason.

In this paper, an alternative LO divider topology is proposed, which combines the True Single Phase Clock (TSPC) topology in a differential LO divider, providing reduced LO phase deviation and improved output noise performance with minimized power consumption.

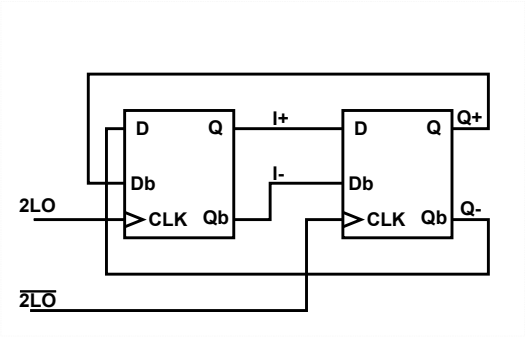

Figure 1: LO Generator top-level schematic.

2 DESCRIPTION

2.1 LO frequency divider

With a simple and compact implementation, TSPC dividers are well known for their significantly lower power consumption when compared to their current-mode logic (CML) counterparts. Though their application was first limited to relatively low frequencies, the speed improvements provided with the constant CMOS downscaling allowed for TSPC logic gates to start replacing CML logic even in high-frequency applications [2] although not providing true differential outputs. To solve this problem a new version of TSPC divider was proposed in [1] with a resistive coupling between stages to generate the complementary outputs.

The top-level LO divider schematic is shown in Figure 1. A combination of two divider blocks in negative feedback are used to implement the quadrature frequency divider. The input signal for

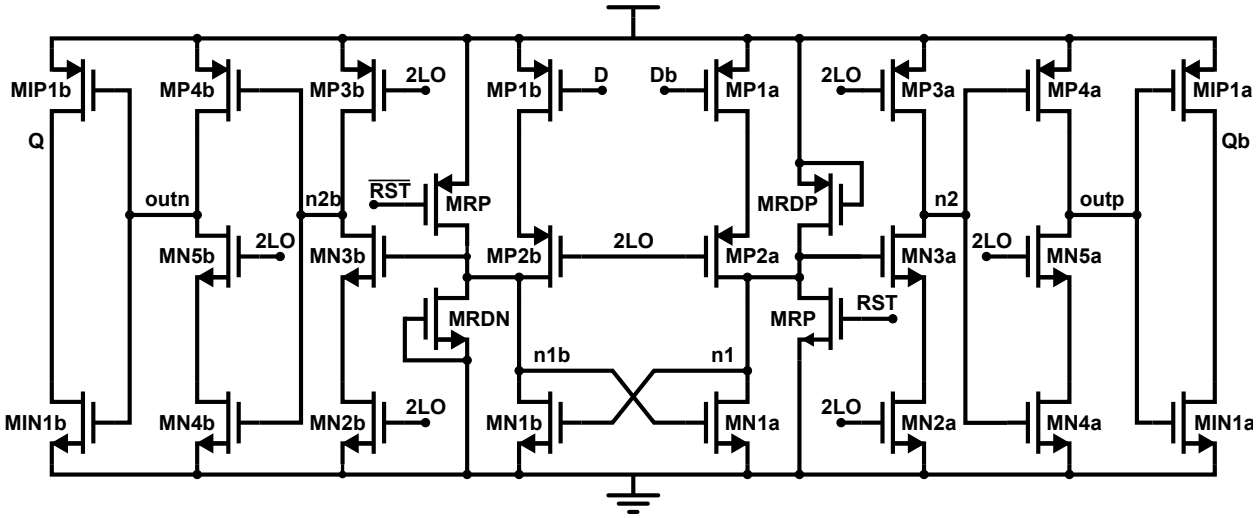

Figure 2: Divide-by-two cell schematic.

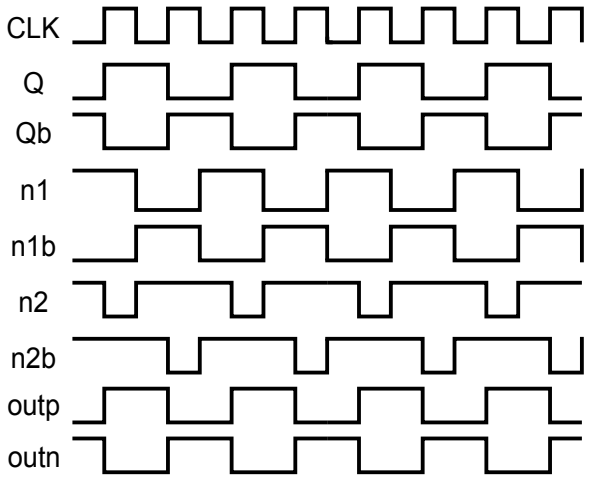

Figure 3: Timing diagram.

the dividers are complementary clock signals, which are typically provided with a balun at the input (potentially incurring phase error).

2.2 TSPC-based differential LO divider

The circuit uses a topology that combines the traditional TSPC basic blocks as first described in [6] and a cross-coupled structure for the input stage as shown in Figure 2, comprising a total of 18 transistors in the core circuit. The use of a cross-coupled pair in the input stage natively creates differential signals without the need of inverters as commonly used in other topologies. The signal is further combined with the clock signal in the two next stages creating the desired divided-by-two outputs in the nodes **outp** and **outn**. As in TSPC topologies, there is no static power consumption.

The inverter is added at the output to provide drive capability even when the output nodes **outp** and **outn** are at high-impedance state (Phase III-Figure 4). It is also necessary to implement the reset capability by adding two more transistors, to ensure that the circuit will be correctly initialized. For the sake of circuit symmetry, dummy transistors are added to make the capacitance on both nodes approximately the same, totalizing 26 transistors.

The timing diagram for the proposed divider is shown in Figure 3 and the logical transitions in the circuit for a divide-by-two operation presented in Figure 4. The input stage is active in the low level of the clock signal, creating a 50% duty-cycle signal in the node **n1** and a delayed version by one clock cycle in the node **n1b**. These signals are used as a mask for the clock input signal in the second stage creating 75% duty-cycle signals in nodes **n2** and **n2b**. As an additional feature, these signals can be used to derive 25% duty-cycle LO signal, as commonly applied in recent transceiver topologies such as [4]. In combination with the clock signal in the third stage, the output duty-cycle is brought to 50%.

The proposed implementation is designed for a targeted output noise density lower than -163 dBc/Hz with minimal phase error between LO phases and minimum power consumption. It is important to note that in closed-loop (as shown in Figure 1), due to setup-time violation, the clock-to-Q delay is a very important limiting factor defining the maximum operating frequency.

3 SIMULATION RESULTS

The proposed LO divider is implemented using a CMOS 65 nm technology and integrates a full RF transmitter frontend designed for low-power (IoT) applications operating at ISM 900MHz band. Area consumption after full-custom layout implementation is 31 μm x 43 μm.

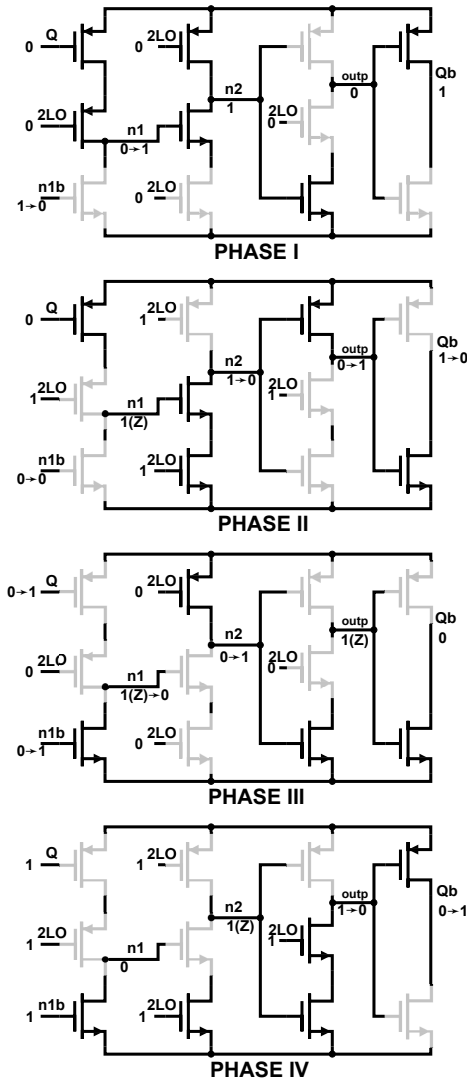

Figure 4: Four phases of a divide-by-two operation.

Figure 5 shows the simulation testbench used for performance assessment. Both transient and periodic steady-state (PSS) simulations were performed to evaluate the respective phase error and phase noise on every output. Worst-case performance was also assessed with circuit simulations considering every corner provided by technology.

Monte Carlo simulations (thousand runs) were performed to evaluate performance robustness regarding phase error between complementary outputs (as defined in Equation 1) and quadrature outputs (as in Equation 2). As demonstrated in Figure 6 the proposed differential architecture keeps the phase error smaller than 1° across the whole input frequency range.

$$\text{Complementary Phase Error} = |\phi(I^+/Q^+) - \phi(I^-/Q^-) - 180| \quad (1)$$

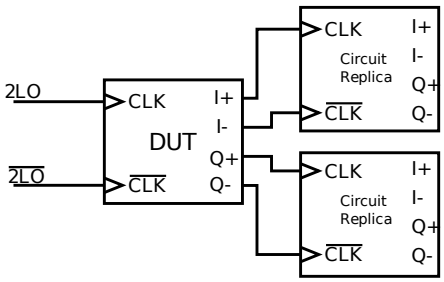

Figure 5: Testbench configuration

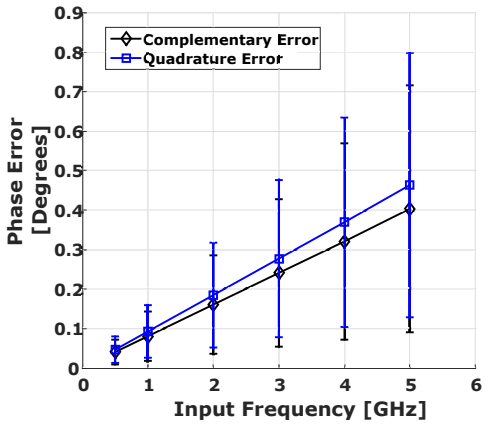

Figure 6: Phase Error (Monte Carlo) showing max. deviation.

$$\text{Quadrature Phase Error} = |\phi(I/Q) - \phi(Q/I) - 90| \quad (2)$$

Designed for a maximum output noise density of -163 dBc/Hz, Figure 7 indicates a nominal power consumption of 0.218 mW/GHz (worst-case 0.2366 mW/GHz in FF corner). For all input frequencies, sensitivity simulations (Figure 8) demonstrates that the required input swing is well below the technology's supply voltage (1.2 V). All performance requirements are met from 0.6 to 5 GHz (4 GHz in SS corner).

Finally, Table 1 summarizes the LO divider performance characteristics in comparison with similar examples from literature. Overall, it should be noted that simulation results indicates an improved performance comparable to more complex topologies (e.g. [5]) while keeping a small area and reduced power consumption. Even though the presented results are derived from simulations, it is believed that even a large degradation due to unpredicted parasitics would place the obtained phase error performance among best.

4 CONCLUSION

In this paper, a differential TSPC-based LO divider topology is demonstrated. Implemented with CMOS 65 nm technology, Monte Carlo simulations indicate a phase error smaller than 1° (including

Table 1: Performance Summary with other state-of-the-art examples

Reference	Tech	Topology	Frequency Range (GHz)	Power (mW)	Phase Error (Degree)	Output Noise (dBc/Hz)	Area
[1] (measured)	0.18 um CMOS	TSPC Divider	0.6 - 5	12@3 GHz	<1.7	N/A	160 μm x 160 μm
[5] (measured)	40 nm CMOS	Quad Dividers	0.56 - 2.92	16.5@1.97 GHz (VCO + I/Q Gen.)	<1	-132.4 @ 1 MHz (1.97 GHz)	0.15 mm2 (VCO + I/Q Gen.)
This Work (simulated)	65 nm CMOS	Differential TSPC-based	0.5 - 5	0.392@1.8 GHz	<1	<-163 @ 40 MHz	31 μm x 43 μm

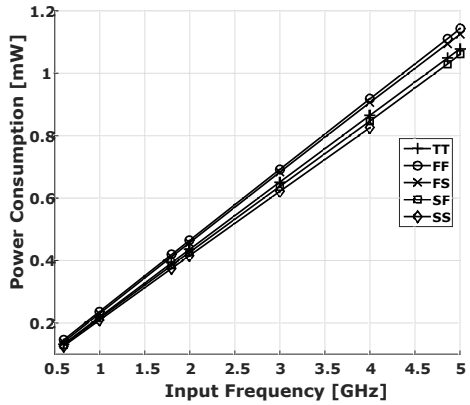

Figure 7: Simulated power consumption across corners.

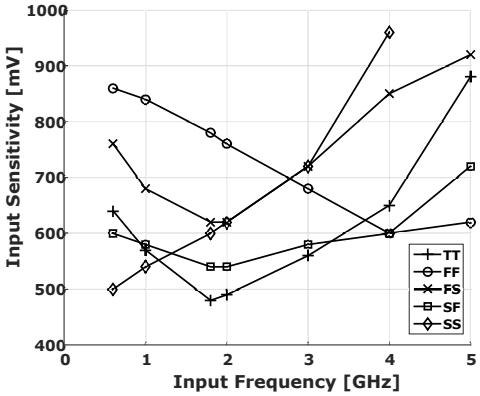

Figure 8: Simulated input sensitivity across corners

corners). With a power consumption of 0.392 mW at 1.8 GHz, the LO divider provides a better than -163 dBc/Hz output noise (at 40 MHz offset), proving to be a viable solution to LO generation in advanced wireless-communication frontend implementations.

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LOW PHASE-ERROR DIFFERENTIAL FREQUENCY DIVIDER FOR QUADRATURE LO GENERATION

Fortaleza - Ceara – Brazil, August 28th to September 1st, 2017

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